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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18868
Number of Logic Elements/Cells	50000
Total RAM Bits	2862080
Number of I/O	240
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cgxfc4c6f23c6n



Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

Related Information

[Cyclone V Device Handbook: Known Issues](#)

Lists the planned updates to the Cyclone V Device Handbook chapters.

Key Advantages of Cyclone V Devices

Table 1. Key Advantages of the Cyclone V Device Family

Advantage	Supporting Feature
Lower power consumption	<ul style="list-style-type: none"> Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks Up to 40% lower power consumption than the previous generation device
Improved logic integration and differentiation capabilities	<ul style="list-style-type: none"> 8-input adaptive logic module (ALM) Up to 13.59 megabits (Mb) of embedded memory Variable-precision digital signal processing (DSP) blocks
Increased bandwidth capacity	<ul style="list-style-type: none"> 3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers Hard memory controllers
Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor	<ul style="list-style-type: none"> Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC) Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Lowest system cost	<ul style="list-style-type: none"> Requires only two core voltages to operate Available in low-cost wirebond packaging Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration

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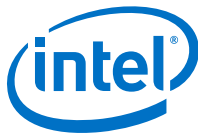
Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

Feature	Description	
Technology	<ul style="list-style-type: none"> TSMC's 28-nm low-power (28LP) process technology 1.1 V core voltage 	
Packaging	<ul style="list-style-type: none"> Wirebond low-halogen packages Multiple device densities with compatible package footprints for seamless migration between different device densities RoHS-compliant and leaded⁽¹⁾ options 	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	<ul style="list-style-type: none"> M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory 	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none"> Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block 64-bit accumulator and cascade Embedded internal coefficient memory Padder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	<ul style="list-style-type: none"> Up to 550 MHz global clock network Global, quadrant, and peripheral clock networks Clock networks that are not used can be powered down to reduce dynamic power 	
Phase-locked loops (PLLs)	<ul style="list-style-type: none"> Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) Integer mode and fractional mode 	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter 400 MHz/800 Mbps external memory interface On-chip termination (OCT) 3.3 V support with up to 16 mA drive strength 	
Low-power high-speed serial interface	<ul style="list-style-type: none"> 614 Mbps to 6.144 Gbps integrated transceiver speed Transmit pre-emphasis and receiver equalization Dynamic partial reconfiguration of individual channels 	
HPS (Cyclone V SE, SX, and ST devices only)	<ul style="list-style-type: none"> Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-Go (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I²C interface, and up to 85 HPS GPIO interfaces System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers On-chip RAM and boot ROM 	

continued...

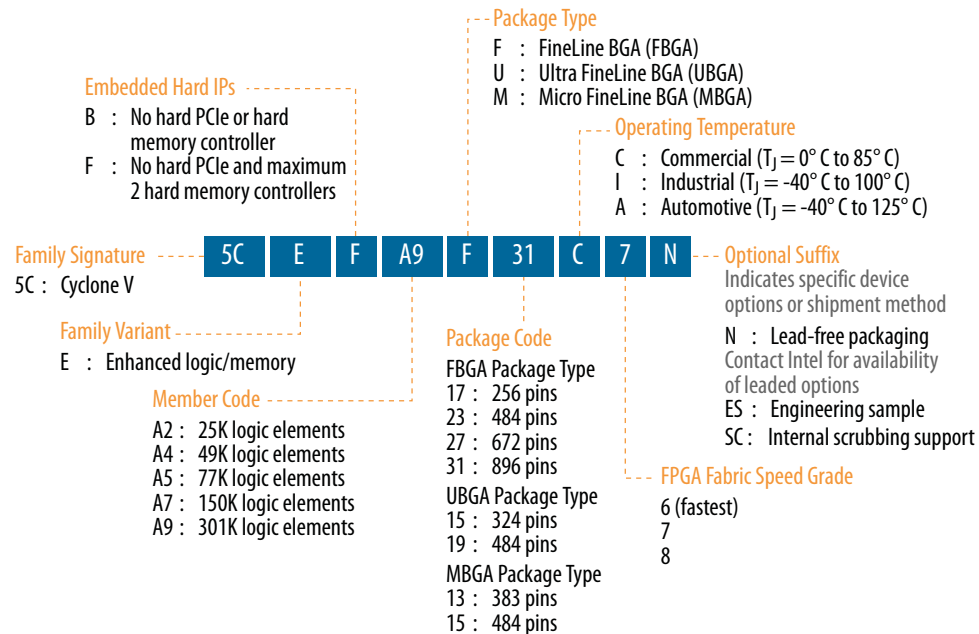
⁽¹⁾ Contact Intel for availability.



Available Options

Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

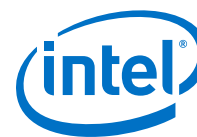
The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 4. Maximum Resource Counts for Cyclone V E Devices

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	150	301
ALM		9,430	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO		224	224	240	480	480
LVDS	Transmitter	56	56	60	120	120
	Receiver	56	56	60	120	120
Hard Memory Controller		1	1	2	2	2



Resource		Member Code				
		C3	C4	C5	C7	C9
LVDS	Transmitter	52	84	84	120	140
	Receiver	52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 7. Package Plan for Cyclone V GX Devices

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	—	—	—	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	—	—	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	208	3	—	—	—	—	—	—
C4	240	6	336	6	—	—	—	—
C5	240	6	336	6	—	—	—	—
C7	240	6	336	9	480	9	—	—
C9	224	6	336	9	480	12	560	12

Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

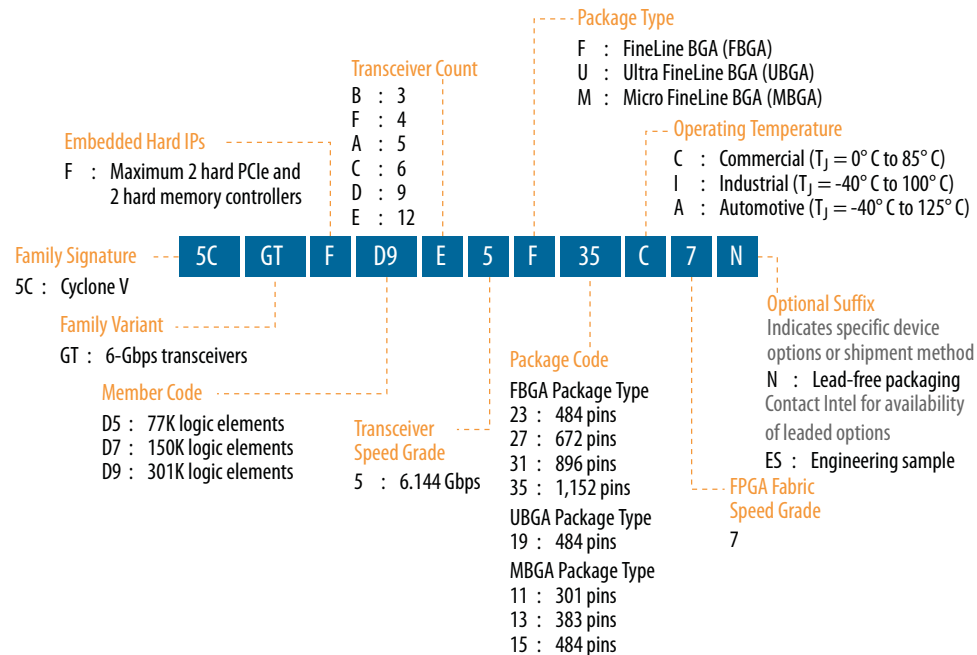
[Product Selector Guide](#)

Provides the latest information about Intel products.



Available Options

Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices



Maximum Resources

Table 8. Maximum Resource Counts for Cyclone V GT Devices

Resource		Member Code		
		D5	D7	D9
Logic Elements (LE) (K)		77	150	301
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DSP Block		150	156	342
18 x 18 Multiplier		300	312	684
PLL		6	7	8
6 Gbps Transceiver		6	9	12
GPIO ⁽⁵⁾		336	480	560
LVDS	Transmitter	84	120	140

continued...

⁽⁵⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 12. Maximum Resource Counts for Cyclone V SX Devices

Resource		Member Code			
		C2	C4	C5	C6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6

continued...



Resource		Member Code			
		C2	C4	C5	C6
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO ⁽⁸⁾		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 ⁽⁹⁾	2 ⁽⁹⁾
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

Package Plan

Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ 1 PCIe Hard IP Block in U672 package.



Resource		Member Code	
		D5	D6
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤ 5 Gbps. 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 ⁽¹¹⁾
D6	288	181	9 ⁽¹¹⁾

Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

⁽¹¹⁾ If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

I/O Vertical Migration for Cyclone V Devices

Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package										
		M301	M383	M484	F256	U324	U484	F484	U672	F672	F896	F1152
Cyclone V E	A2		↕↕↕		↕↕	↕↕	↕↕	↕↕				
	A4		↕↕		↕↕	↕↕	↕↕	↕↕				
	A5		↕↕↕				↕↕	↕↕				
	A7						↕↕	↕↕		↕↕	↕↕	
	A9						↕↕	↕↕		↕↕	↕↕	
Cyclone V GX	C3						↕↕	↕↕		↕↕	↕↕	
	C4	↕↕	↕↕				↕↕	↕↕		↕↕		
	C5	↕↕	↕↕				↕↕	↕↕		↕↕		
	C7						↕↕	↕↕			↕↕	
	C9						↕↕	↕↕		↕↕	↕↕	
Cyclone V GT	D5						↕↕	↕↕		↕↕	↕↕	
	D7						↕↕	↕↕		↕↕	↕↕	
	D9						↕↕	↕↕		↕↕	↕↕	
Cyclone V SE	A2						↕↕		↕↕↕	↕↕↕		
	A4						↕↕		↕↕↕	↕↕↕		
	A5								↕↕↕	↕↕↕	↕↕	
	A6						↕↕		↕↕↕	↕↕↕	↕↕	
Cyclone V SX	C2								↕↕↕	↕↕↕		
	C4								↕↕↕	↕↕↕		
	C5								↕↕↕	↕↕↕	↕↕	
	C6								↕↕↕	↕↕↕	↕↕	
Cyclone V ST	D5										↕↕	
	D6										↕↕	

You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters and general DSP usage	Two 18 x 18 with accumulate	1
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
Cyclone V E	A2	25	75	50	25	25	25
	A4	66	198	132	66	66	66
	A5	150	450	300	150	150	150
	A7	156	468	312	156	156	156
	A9	342	1,026	684	342	342	342
Cyclone V GX	C3	57	171	114	57	57	57
	C4	70	210	140	70	70	70
	C5	150	450	300	150	150	150
	C7	156	468	312	156	156	156
	C9	342	1,026	684	342	342	342
Cyclone V GT	D5	150	450	300	150	150	150
	D7	156	468	312	156	156	156
	D9	342	1,026	684	342	342	342
Cyclone V SE	A2	36	108	72	36	36	36
	A4	84	252	168	84	84	84
	A5	87	261	174	87	87	87
	A6	112	336	224	112	112	112
Cyclone V SX	C2	36	108	72	36	36	36
	C4	84	252	168	84	84	84
	C5	87	261	174	87	87	87
continued...							



External Memory Performance

Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.



PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23. Transceiver PCS Features for Cyclone V Devices

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
3-Gbps and 6-Gbps Basic	0.614 to 6.144	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Transmitter bit-slip 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate-match FIFO 8B/10B decoder Byte deserializer Byte ordering Receiver phase compensation FIFO
PCIe Gen1 (x1, x2, x4)	2.5 and 5.0	<ul style="list-style-type: none"> Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic 	<ul style="list-style-type: none"> Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic
PCIe Gen2 (x1, x2, x4) ⁽¹²⁾			
GbE	1.25	<ul style="list-style-type: none"> Custom PHY IP core with preset feature GbE transmitter synchronization state machine 	<ul style="list-style-type: none"> Custom PHY IP core with preset feature GbE receiver synchronization state machine
XAUI ⁽¹³⁾	3.125	<ul style="list-style-type: none"> Dedicated XAUI PHY IP core XAUI synchronization state machine for bonding four channels 	<ul style="list-style-type: none"> Dedicated XAUI PHY IP core XAUI synchronization state machine for realigning four channels
HiGig	3.75		
SRIO 1.3 and 2.1	1.25 to 3.125	<ul style="list-style-type: none"> Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 channel bonding 	<ul style="list-style-type: none"> Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 deskew state machine
SDI, SD/HD, and 3G-SDI	0.27 ⁽¹⁴⁾ , 1.485, and 2.97	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature
JESD204A	0.3125 ⁽¹⁵⁾ to 3.125		

continued...

⁽¹²⁾ PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

⁽¹³⁾ XAUI is supported through the soft PCS.

⁽¹⁴⁾ The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁵⁾ The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.



PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Serial ATA Gen1 and Gen2	1.5 and 3.0	<ul style="list-style-type: none">Custom PHY IP core with preset featureElectrical idle	<ul style="list-style-type: none">Custom PHY IP core with preset featureSignal detectWider spread of asynchronous SSC
CPRI 4.1 ⁽¹⁶⁾	0.6144 to 6.144	<ul style="list-style-type: none">Dedicated deterministic latency PHY IP coreTransmitter (TX) manual bit-slip mode	<ul style="list-style-type: none">Dedicated deterministic latency PHY IP coreReceiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072		
V-by-One HS	Up to 3.75	Custom PHY IP core	<ul style="list-style-type: none">Custom PHY IP coreWider spread of asynchronous SSC
DisplayPort 1.2 ⁽¹⁷⁾	1.62 and 2.7		

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

⁽¹⁶⁾ High-voltage output mode (1000-BASE-CX) is not supported.

⁽¹⁷⁾ Pending characterization.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 400 MHz (800 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.



Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

[Cyclone V Device Family Pin Connection Guidelines](#)

Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

[International Altera Sales Support Offices](#)

Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial Reconfiguration

Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

Table 24. Configuration Schemes and Features Supported by Cyclone V Devices

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration ⁽¹⁸⁾	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	
CvP (PCIe)	x1, x2, and x4 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Related Information

[Configuration via Protocol \(CvP\) Implementation in Intel FPGAs User Guide](#)

Provides more information about CvP.

⁽¹⁸⁾ The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Date	Version	Changes
		<ul style="list-style-type: none">Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<ul style="list-style-type: none">Cyclone V GX C3: Updated from 181 to 182Cyclone V GX C4: Updated from 295 to 424Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<ul style="list-style-type: none">Cyclone V GX C3: Updated from 1,531 to 1,532Cyclone V GX C4: Updated from 2,795 to 2,924Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<ul style="list-style-type: none">Cyclone V GX C4: Updated from 472 to 678Cyclone V GX C5: Updated from 679 to 678
March 2015	2015.03.31	<ul style="list-style-type: none">Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table.Added optional suffix "SC: Internal scrubbing support" to the following diagrams:<ul style="list-style-type: none">Sample Ordering Code and Available Options for Cyclone V E DevicesSample Ordering Code and Available Options for Cyclone V GX DevicesSample Ordering Code and Available Options for Cyclone V SE DevicesSample Ordering Code and Available Options for Cyclone V SX Devices
January 2015	2015.01.23	<ul style="list-style-type: none">Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and -7 speed grade.<ul style="list-style-type: none">Operating Temperature: Removed C and A temperature gradesFPGA Fabric Speed Grade: Removed -6 and -8 speed gradesUpdated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps:<ul style="list-style-type: none">Device Variants for the Cyclone V Device Family tableSample Ordering Code and Available Options for Cyclone V ST Devices figureMaximum Resource Counts for Cyclone V ST DevicesUpdated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices.<ul style="list-style-type: none">Logic elements (LE) (K): Updated from 35.7 to 35.5Variable-precision DSP block: Updated from 51 to 5718 x 18 multiplier: Updated from 102 to 114Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices.<ul style="list-style-type: none">Variableprecision DSP Block: Updated from 51 to 579 x 9 Multiplier: Updated from 153 to 17118 x 18 Multiplier: Updated from 102 to 11427 x 27 Multiplier: Updated from 51 to 5718 x 18 Multiplier Adder Mode: Updated from 51 to 5718 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices.<ul style="list-style-type: none">M10K block: Updated from 119 to 135M10K RAM bit (Kb): Updated from 1,190 to 1,350MLAB block: Updated from 255 to 291MLAB RAM bit (Kb): Updated from 159 to 181Total RAM bit (Kb): Updated from 1,349 to 1,531
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.
continued...		



Date	Version	Changes
July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	<ul style="list-style-type: none"> Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. Added link to Altera Product Selector for each device variant. Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120. Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84. Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168. Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252. Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37. Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5. Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. Added decompression support for the CvP configuration mode.
May 2013	2013.05.06	<ul style="list-style-type: none"> Added link to the known document issues in the Knowledge Base. Moved all links to the Related Information section of respective topics for easy reference. Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. Updated the package plan with M383 for the Cyclone V E device. Removed the M301 and M383 packages from the Cyclone V GX C4 device. Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. Updated 5 Gbps to '6.144 Gbps' for Cyclone V GT device.

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Date	Version	Changes
		<ul style="list-style-type: none"> Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6. Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices. Removed '36 x 36' from the Variable-Precision DSP Block. Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device. Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices. Updated Figure 7 which shows the I/O vertical migration table. Updated Table 17 for Cyclone V SX C4 device. Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. Removed 'Counter reconfiguration' from the PLL Features. Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps. Removed 'Distributed Memory' symbol. Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'. Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps. Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'. Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'. Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'. Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.
December 2012	2012.12.28	<ul style="list-style-type: none"> Updated the pin counts for the MBGA packages. Updated the GPIO and transceiver counts for the MBGA packages. Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices. Updated the vertical migration table for vertical migration of the U484 packages. Updated the MLAB supported programmable widths at 32 bits depth.
November 2012	2012.11.19	<ul style="list-style-type: none"> Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT. Added ordering code for five-transceiver devices for Cyclone V GT and ST. Updated the vertical migration table to add MBGA packages. Added performance information for HPS memory controller. Removed DDR3U support. Updated Cyclone V ST speed grade information. Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance. Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software. Updated template.
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	<ul style="list-style-type: none"> Restructured the document. Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. Added Table 1, Table 3, Table 16, Table 19, and Table 20. Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.
continued...		



Date	Version	Changes
		<ul style="list-style-type: none"> Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. Text edits throughout the document.
February 2012	1.2	<ul style="list-style-type: none"> Updated Table 1-2, Table 1-3, and Table 1-6. Updated "Cyclone V Family Plan" on page 1-4 and "Clock Networks and PLL Clock Sources" on page 1-15. Updated Figure 1-1 and Figure 1-6.
November 2011	1.1	<ul style="list-style-type: none"> Updated Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-5, and Table 1-6. Updated Figure 1-4, Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8. Updated "System Peripherals" on page 1-18, "HPS-FPGA AXI Bridges" on page 1-19, "HPS SDRAM Controller Subsystem" on page 1-19, "FPGA Configuration and Processor Booting" on page 1-19, and "Hardware and Software Development" on page 1-20. Minor text edits.
October 2011	1.0	Initial release.