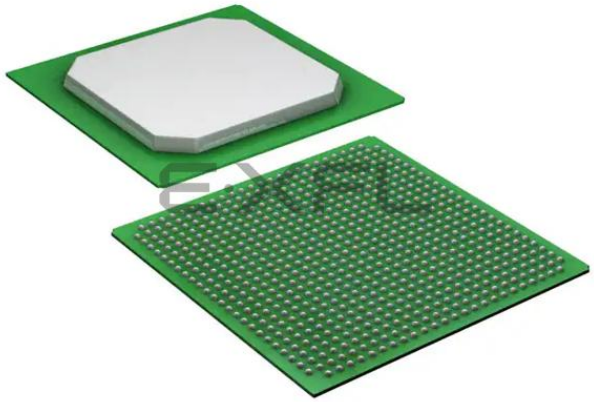

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18868
Number of Logic Elements/Cells	50000
Total RAM Bits	2862080
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cgxfc4c6f27c7n

Contents

Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

Feature	Description	
Technology	• TSMC's 28-nm low-power (28LP) process technology • 1.1 V core voltage	
Packaging	• Wirebond low-halogen packages • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS-compliant and leaded(1) options	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) • Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory	
Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block • 64-bit accumulator and cascade • Embedded internal coefficient memory • Preadder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	• Up to 550 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode	
FPGA General-purpose I/Os (GPIOs)	• 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter • 400 MHz/800 Mbps external memory interface • On-chip termination (OCT) • 3.3 V support with up to 16 mA drive strength	
Low-power high-speed serial interface	• 614 Mbps to 6.144 Gbps integrated transceiver speed • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels	
HPS (Cyclone V SE, SX, and ST devices only)	• Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I^2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM	

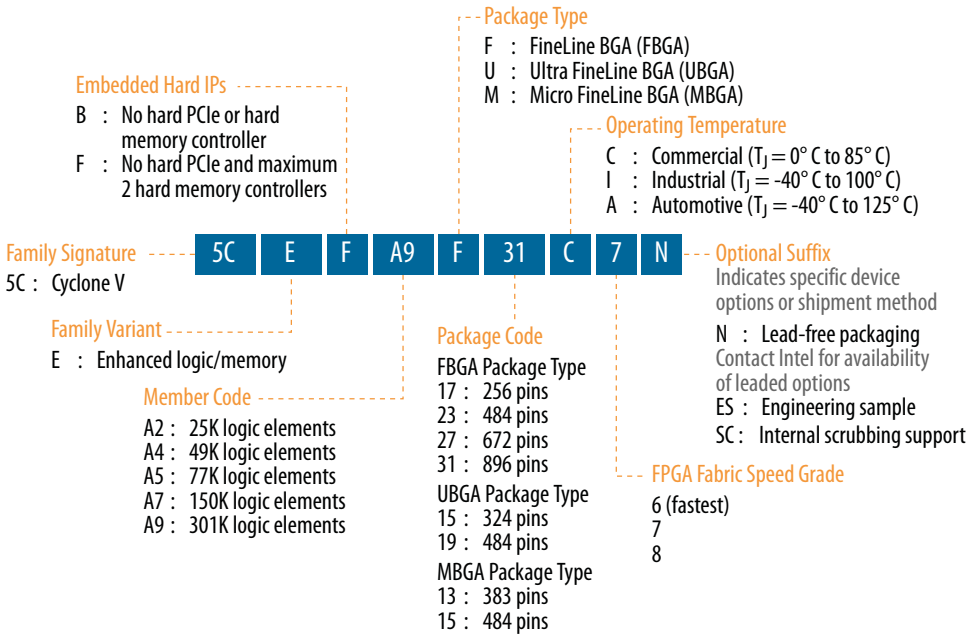
continued...

(1) Contact Intel for availability.

Available Options

Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 4. Maximum Resource Counts for Cyclone V E Devices

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	150	301
ALM		9,430	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO		224	224	240	480	480
LVDS	Transmitter	56	56	60	120	120
	Receiver	56	56	60	120	120
Hard Memory Controller		1	1	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 5. Package Plan for Cyclone V E Devices

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	223	—	176	128	224	224	—	—
A4	223	—	176	128	224	224	—	—
A5	175	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Resource		Member Code				
		C3	C4	C5	C7	C9
LVDS	Transmitter	52	84	84	120	140
	Receiver	52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 7. Package Plan for Cyclone V GX Devices

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	—	—	—	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	—	—	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	208	3	—	—	—	—	—	—
C4	240	6	336	6	—	—	—	—
C5	240	6	336	6	—	—	—	—
C7	240	6	336	9	480	9	—	—
C9	224	6	336	9	480	12	560	12

Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

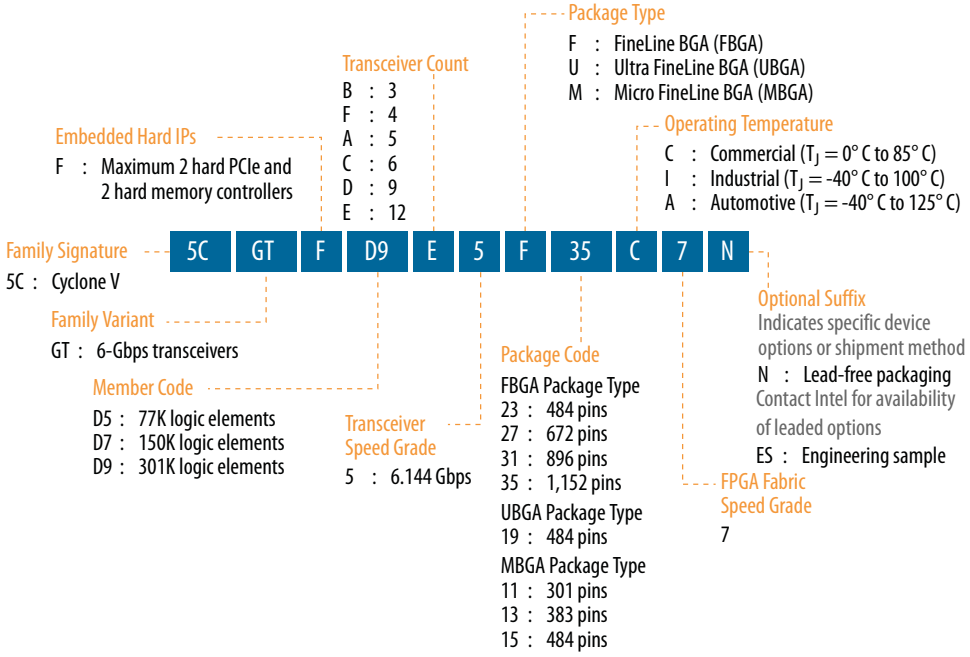
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices



Maximum Resources

Table 8. Maximum Resource Counts for Cyclone V GT Devices

Resource		Member Code		
		D5	D7	D9
Logic Elements (LE) (K)		77	150	301
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DSP Block		150	156	342
18 x 18 Multiplier		300	312	684
PLL		6	7	8
6 Gbps Transceiver		6	9	12
GPIO(5)		336	480	560
LVDS	Transmitter	84	120	140

continued...

(5) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code		
		D5	D7	D9
	Receiver	84	120	140
PCIe Hard IP Block		2	2	2
Hard Memory Controller		2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 9. Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	129	4	175	6	—	—	224	6
D7	—	—	—	—	240	3	240	6
D9	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	240	6	336	6	—	—	—	—
D7	240	6	336	9 (6)	480	9 (6)	—	—
D9	224	6	336	9 (6)	480	12 (7)	560	12 (7)

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(6) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

(7) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Resource		Member Code			
		C2	C4	C5	C6
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO (8)		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 (9)	2 (9)
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

(8) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

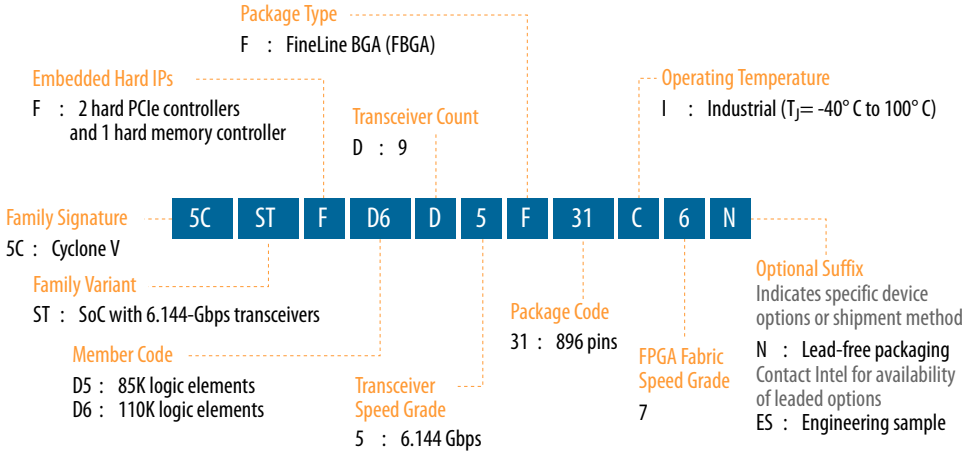
(9) 1 PCIe Hard IP Block in U672 package.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices



Maximum Resources

Table 14. Maximum Resource Counts for Cyclone V ST Devices

Resource		Member Code	
		D5	D6
Logic Elements (LE) (K)		85	110
ALM		32,070	41,910
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,570
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL		6	6
HPS PLL		3	3
6.144 Gbps Transceiver		9	9
FPGA GPIO(10)		288	288
HPS I/O		181	181
LVDS	Transmitter	72	72

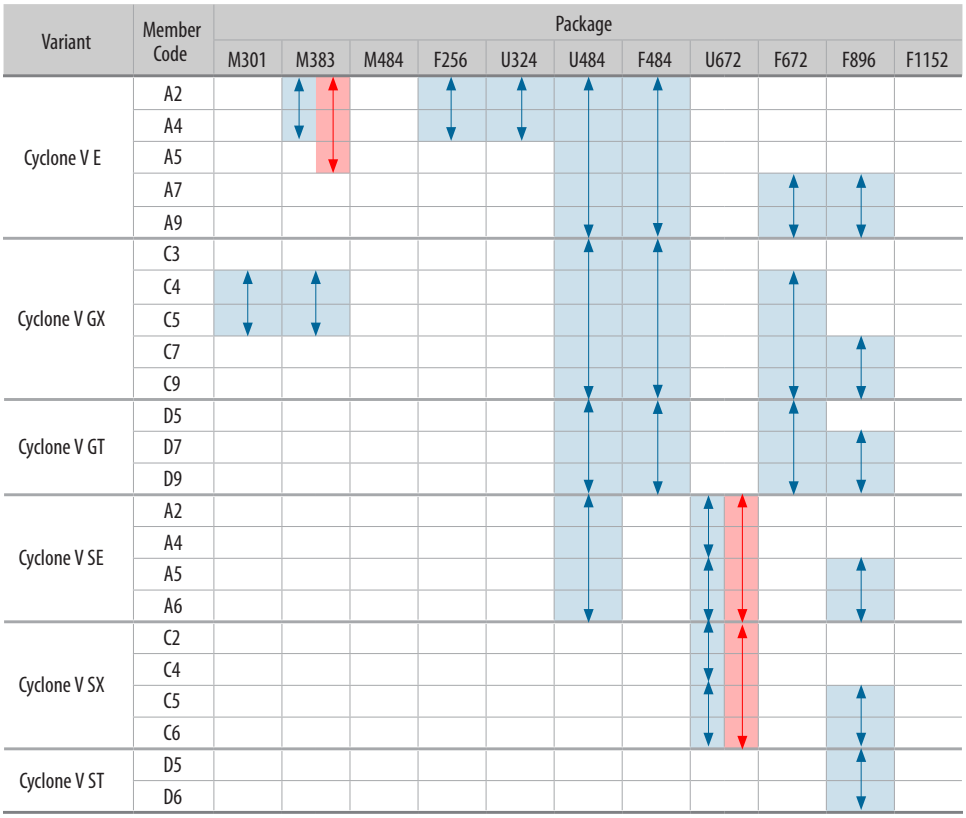
continued...

(10) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

I/O Vertical Migration for Cyclone V Devices

Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.



You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

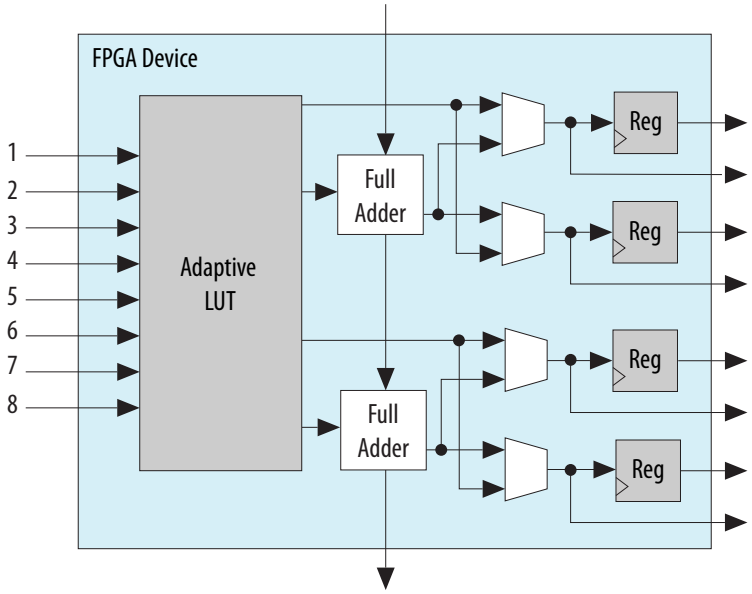
Note: To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Figure 8. ALM for Cyclone V Devices



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21
Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

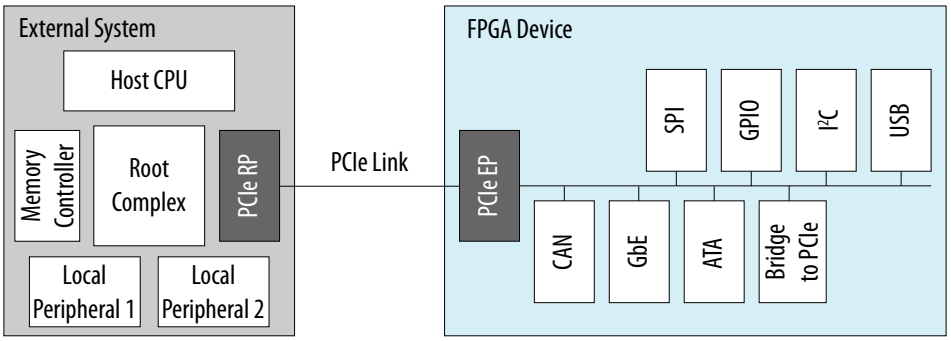
PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 9. PCIe Multifunction for Cyclone V Devices



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.

External Memory Performance

Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Cyclone V devices deliver the industry’s lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23. Transceiver PCS Features for Cyclone V Devices

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
3-Gbps and 6-Gbps Basic	0.614 to 6.144	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Transmitter bit-slip	• Word aligner • Deskew FIFO • Rate-match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • Receiver phase compensation FIFO
PCIe Gen1 (x1, x2, x4)	2.5 and 5.0	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic
PCIe Gen2 (x1, x2, x4)(12)			
GbE	1.25	• Custom PHY IP core with preset feature • GbE transmitter synchronization state machine	• Custom PHY IP core with preset feature • GbE receiver synchronization state machine
XAUI (13)	3.125	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for bonding four channels	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for realigning four channels
HiGig	3.75		
SRIO 1.3 and 2.1	1.25 to 3.125	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 channel bonding	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 deskew state machine
SDI, SD/HD, and 3G-SDI	0.27(14), 1.485, and 2.97	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature
JESD204A	0.3125(15) to 3.125		

continued...

(12) PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

(13) XAUI is supported through the soft PCS.

(14) The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

(15) The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Serial ATA Gen1 and Gen2	1.5 and 3.0	• Custom PHY IP core with preset feature • Electrical idle	• Custom PHY IP core with preset feature • Signal detect • Wider spread of asynchronous SSC
CPRI 4.1(16)	0.6144 to 6.144	• Dedicated deterministic latency PHY IP core • Transmitter (TX) manual bit-slip mode	• Dedicated deterministic latency PHY IP core • Receiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072		
V-by-One HS	Up to 3.75	Custom PHY IP core	• Custom PHY IP core • Wider spread of asynchronous SSC
DisplayPort 1.2(17)	1.62 and 2.7		

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

(16) High-voltage output mode (1000-BASE-CX) is not supported.

(17) Pending characterization.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the *Sample Ordering Code and Available Options* diagrams. • Rebranded as Intel.

Date	Version	Changes
December 2017	2017.12.18	• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.
June 2016	2016.06.10	Updated Cyclone V GT speed grade to –7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	• Added descriptions to package plan tables for Cyclone V GT and ST devices. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives. • Updated logic elements (LE) (K) for the following devices: — Cyclone V E A7: Updated from 149.5 to 150 — Cyclone V GX C3: Updated from 35.5 to 36 — Cyclone V GX C7: Updated from 149.7 to 150 — Cyclone V GT D7: Updated from 149.5 to 150 • Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows: — Cyclone V GX C3: Updated from 291 to 182 — Cyclone V GX C4: Updated from 678 to 424 — Cyclone V GX C5: Updated from 678 to 424 — Cyclone V GX C7: Updated from 1,338 to 836 — Cyclone V GX C9: Updated from 2,748 to 1,717

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Date	Version	Changes
July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	• Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. • Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. • Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. • Added link to Altera Product Selector for each device variant. • Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. • Added leaded package options. • Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. • Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60. • Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120. • Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84. • Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168. • Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252. • Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. • Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37. • Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5. • Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V. • Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. • Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. • Added decompression support for the CvP configuration mode.
May 2013	2013.05.06	• Added link to the known document issues in the Knowledge Base. • Moved all links to the Related Information section of respective topics for easy reference. • Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. • Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. • Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. • Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. • Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. • Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. • Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. • Updated the package plan with M383 for the Cyclone V E device. • Removed the M301 and M383 packages from the Cyclone V GX C4 device. • Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. • Updated 5 Gbps to '6.144 Gbps' forCyclone V GT device.

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Date	Version	Changes
		• Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6. • Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. • Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices. • Removed '36 x 36' from the Variable-Precision DSP Block. • Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device. • Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices. • Updated Figure 7 which shows the I/O vertical migration table. • Updated Table 17 for Cyclone V SX C4 device. • Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. • Removed 'Counter reconfiguration' from the PLL Features. • Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps. • Removed 'Distributed Memory' symbol. • Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'. • Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps. • Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'. • Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'. • Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'. • Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.
December 2012	2012.12.28	• Updated the pin counts for the MBGA packages. • Updated the GPIO and transceiver counts for the MBGA packages. • Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices. • Updated the vertical migration table for vertical migration of the U484 packages. • Updated the MLAB supported programmable widths at 32 bits depth.
November 2012	2012.11.19	• Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT. • Added ordering code for five-transceiver devices for Cyclone V GT and ST. • Updated the vertical migration table to add MBGA packages. • Added performance information for HPS memory controller. • Removed DDR3U support. • Updated Cyclone V ST speed grade information. • Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance. • Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software. • Updated template.
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	• Restructured the document. • Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. • Added Table 1, Table 3, Table 16, Table 19, and Table 20. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.

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Date	Version	Changes
		• Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. • Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. • Text edits throughout the document.
February 2012	1.2	• Updated Table 1–2, Table 1–3, and Table 1–6. • Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15. • Updated Figure 1–1 and Figure 1–6.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. • Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8. • Updated "System Peripherals" on page 1–18, "HPS–FPGA AXI Bridges" on page 1–19, "HPS SDRAM Controller Subsystem" on page 1–19, "FPGA Configuration and Processor Booting" on page 1–19, and "Hardware and Software Development" on page 1–20. • Minor text edits.
October 2011	1.0	Initial release.