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Understanding [Embedded - FPGAs (Field Programmable Gate Array)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	29080
Number of Logic Elements/Cells	77000
Total RAM Bits	5001216
Number of I/O	175
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	383-TFBGA
Supplier Device Package	383-MBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cgxfc5c7m13c8n

Contents

Summary of Cyclone V Features

Table 2.   Summary of Features for Cyclone V Devices

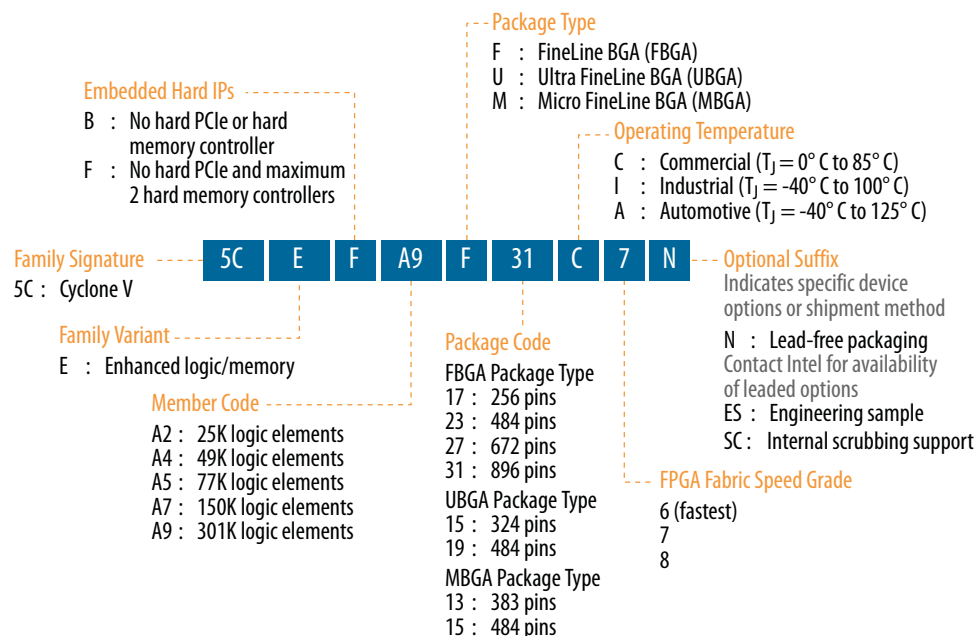| Feature	Description	
Technology	• TSMC's 28-nm low-power (28LP) process technology • 1.1 V core voltage	
Packaging	• Wirebond low-halogen packages • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS-compliant and leaded[1]options	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) • Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory	
Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block • 64-bit accumulator and cascade • Embedded internal coefficient memory • Preadder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	• Up to 550 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode	
FPGA General-purpose I/Os (GPIOs)	• 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter • 400 MHz/800 Mbps external memory interface • On-chip termination (OCT) • 3.3 V support with up to 16 mA drive strength	
Low-power high-speed serial interface	• 614 Mbps to 6.144 Gbps integrated transceiver speed • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels	
HPS (Cyclone V SE, SX, and ST devices only)	• Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I^2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM	

continued...

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[1] Contact Intel for availability.

Available Options

Figure 1. **Sample Ordering Code and Available Options for Cyclone V E Devices**

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Package Type
F : FineLine BGA (FBGA)
U : Ultra FineLine BGA (UBGA)
M : Micro FineLine BGA (MBGA)

Embedded Hard IPs
B : No hard PCIe or hard memory controller
F : No hard PCIe and maximum 2 hard memory controllers

Operating Temperature
C : Commercial ($T_J = 0°$ C to $85°$ C)
I : Industrial ($T_J = -40°$ C to $100°$ C)
A : Automotive ($T_J = -40°$ C to $125°$ C)

Family Signature
5C : Cyclone V

| 5C | E | F | A9 | F | 31 | C | 7 | N |

Optional Suffix
Indicates specific device options or shipment method
N : Lead-free packaging
Contact Intel for availability of leaded options
ES : Engineering sample
SC : Internal scrubbing support

Family Variant
E : Enhanced logic/memory

Member Code
A2 : 25K logic elements
A4 : 49K logic elements
A5 : 77K logic elements
A7 : 150K logic elements
A9 : 301K logic elements

Package Code
FBGA Package Type
17 : 256 pins
23 : 484 pins
27 : 672 pins
31 : 896 pins
UBGA Package Type
15 : 324 pins
19 : 484 pins
MBGA Package Type
13 : 383 pins
15 : 484 pins

FPGA Fabric Speed Grade
6 (fastest)
7
8

Maximum Resources

Table 4. **Maximum Resource Counts for Cyclone V E Devices**

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	150	301
ALM		9,430	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO		224	224	240	480	480
LVDS	Transmitter	56	56	60	120	120
	Receiver	56	56	60	120	120
Hard Memory Controller		1	1	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 5. **Package Plan for Cyclone V E Devices**

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	223	—	176	128	224	224	—	—
A4	223	—	176	128	224	224	—	—
A5	175	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
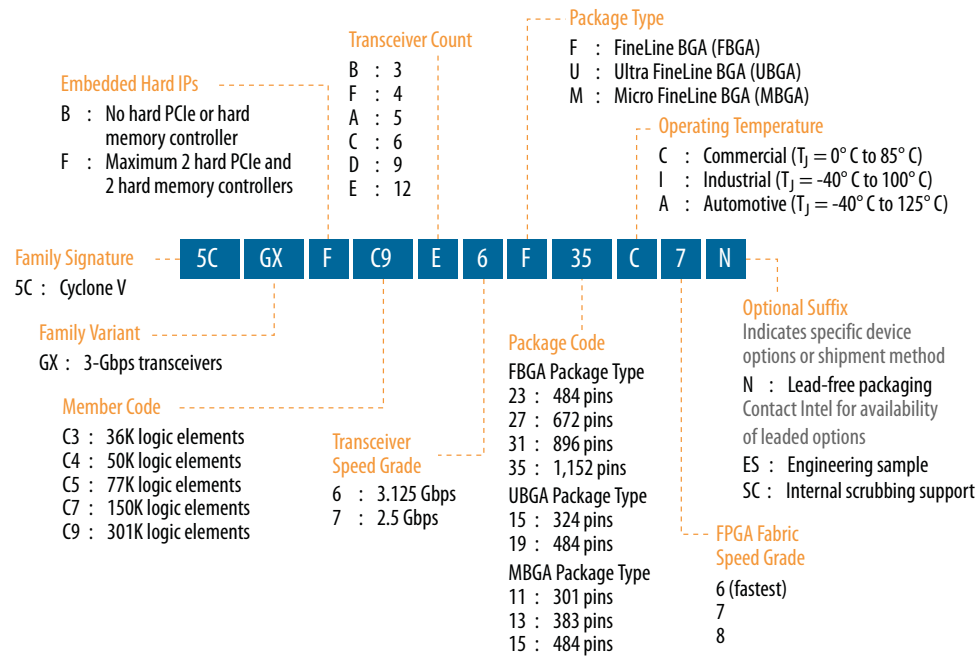Provides the latest information about Intel products.

Available Options

Figure 2.   Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Transceiver Count
B : 3
F : 4
A : 5
C : 6
D : 9
E : 12

Embedded Hard IPs
B : No hard PCIe or hard
     memory controller
F : Maximum 2 hard PCIe and
     2 hard memory controllers

Package Type
F : FineLine BGA (FBGA)
U : Ultra FineLine BGA (UBGA)
M : Micro FineLine BGA (MBGA)

Operating Temperature
C : Commercial (T_J = 0° C to 85° C)
I : Industrial (T_J = -40° C to 100° C)
A : Automotive (T_J = -40° C to 125° C)

| 5C | GX | F | C9 | E | 6 | F | 35 | C | 7 | N |

Family Signature
5C : Cyclone V

Family Variant
GX : 3-Gbps transceivers

Member Code
C3 : 36K logic elements
C4 : 50K logic elements
C5 : 77K logic elements
C7 : 150K logic elements
C9 : 301K logic elements

Transceiver Speed Grade
6 :   3.125 Gbps
7 :   2.5 Gbps

Package Code
FBGA Package Type
23 : 484 pins
27 : 672 pins
31 : 896 pins
35 : 1,152 pins
UBGA Package Type
15 : 324 pins
19 : 484 pins
MBGA Package Type
11 : 301 pins
13 : 383 pins
15 : 484 pins

Optional Suffix
Indicates specific device options or shipment method
N :   Lead-free packaging
Contact Intel for availability of leaded options
ES : Engineering sample
SC : Internal scrubbing support

FPGA Fabric Speed Grade
6 (fastest)
7
8

Maximum Resources

Table 6.   Maximum Resource Counts for Cyclone V GX Devices

Resource		Member Code				
		C3	**C4**	**C5**	**C7**	**C9**
Logic Elements (LE) (K)		36	50	77	150	301
ALM		13,460	18,860	29,080	56,480	113,560
Register		53,840	75,440	116,320	225,920	454,240
Memory (Kb)	M10K	1,350	2,500	4,460	6,860	12,200
	MLAB	182	424	424	836	1,717
Variable-precision DSP Block		57	70	150	156	342
18 x 18 Multiplier		114	140	300	312	684
PLL		4	6	6	7	8
3 Gbps Transceiver		3	6	6	9	12
GPIO[4]		208	336	336	480	560
continued...						

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[4] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code				
		C3	**C4**	**C5**	**C7**	**C9**
LVDS	Transmitter	52	84	84	120	140
	Receiver	52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 7.   Package Plan for Cyclone V GX Devices

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	—	—	—	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	—	—	—	—	—	—	—	—	240	5

| Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**
C3	208	3	—	—	—	—	—	—
C4	240	6	336	6	—	—	—	—
C5	240	6	336	6	—	—	—	—
C7	240	6	336	9	480	9	—	—
C9	224	6	336	9	480	12	560	12

Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
Provides the latest information about Intel products.
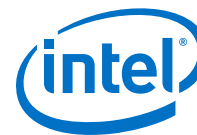
Resource		Member Code			
		C2	**C4**	**C5**	**C6**
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO [8]		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 [9]	2 [9]
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 13.   Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	**HPS I/O**	**XCVR**	**FPGA GPIO**	**HPS I/O**	**XCVR**
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

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[8] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

[9] 1 PCIe Hard IP Block in U672 package.
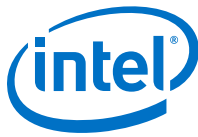
Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 6.   Sample Ordering Code and Available Options for Cyclone V ST Devices
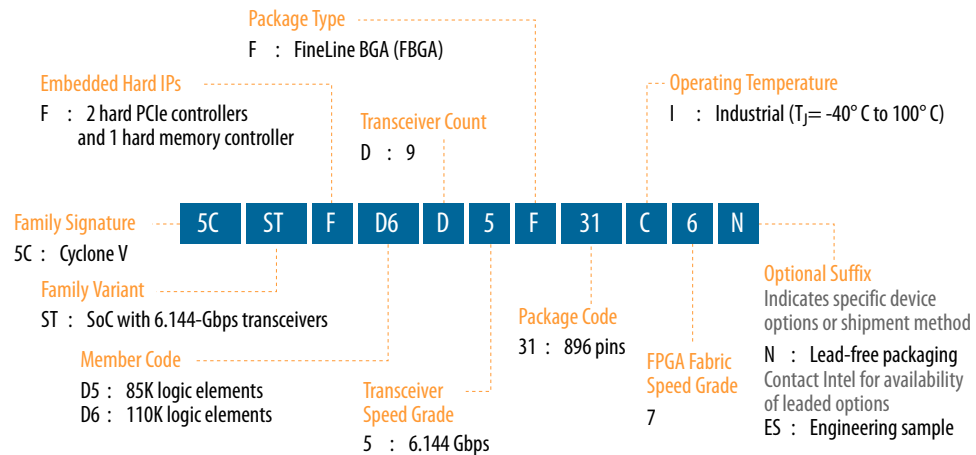
Maximum Resources

Table 14.   Maximum Resource Counts for Cyclone V ST Devices

Resource		Member Code	
		D5	**D6**
Logic Elements (LE) (K)		85	110
ALM		32,070	41,910
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,570
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL		6	6
HPS PLL		3	3
6.144 Gbps Transceiver		9	9
FPGA GPIO[10]		288	288
HPS I/O		181	181
LVDS	Transmitter	72	72
			continued...

---

[10] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code	
		D5	**D6**
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 15.   Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	**HPS I/O**	**XCVR**
D5	288	181	9 [11]
D6	288	181	9 [11]

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

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[11] If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

I/O Vertical Migration for Cyclone V Devices

Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package										
		M301	M383	M484	F256	U324	U484	F484	U672	F672	F896	F1152
Cyclone V E	A2		↑↕		↕	↕		↑				
	A4		↓		↓	↓						
	A5		↓				■					
	A7						■			↑	↑	
	A9						↓	↓		↓	↓	
Cyclone V GX	C3						↑	↑				
	C4	↑	↑							↑		
	C5	↓	↓									
	C7										↑	
	C9						↓	↓			↓	
Cyclone V GT	D5						↑	↑			↑	
	D7						■	■			■	
	D9						↓	↓		↓	↓	
Cyclone V SE	A2						↑		↑			
	A4						■		↓			
	A5						■		■		↑	
	A6						↓		↕			
Cyclone V SX	C2								↑			
	C4								↓			
	C5								■		↑	
	C6								↓		↓	
Cyclone V ST	D5										↑	
	D6										↓	

You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Figure 8.   ALM for Cyclone V Devices
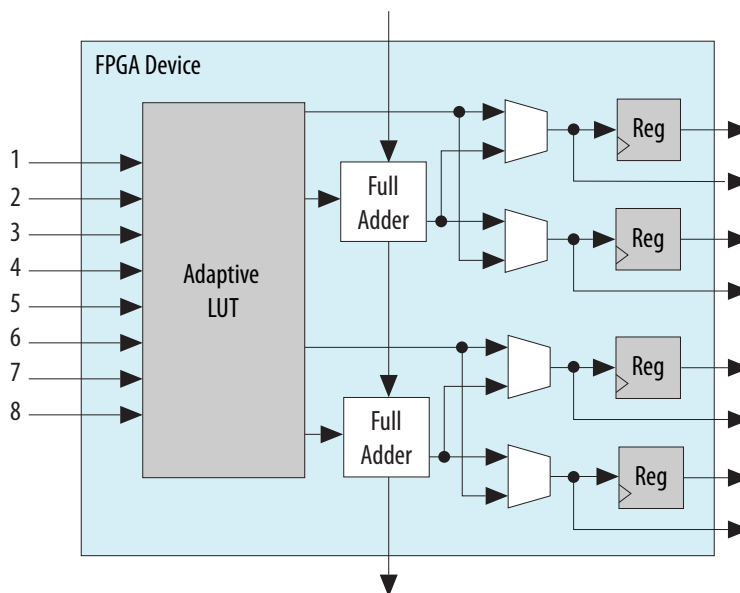
You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21
    Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively

- A 64-bit accumulator

- A hard preadder that is available in both 18- and 27-bit modes

- Cascaded output adders for efficient systolic finite impulse response (FIR) filters

- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode

- Fully independent multiplier operation

- A second accumulator feedback register to accommodate complex multiply-accumulate functions

- Fully independent Efficient support for single-precision floating point arithmetic

- The inferability of all modes by the Intel Quartus Prime design software
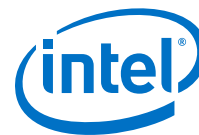
PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

Figure 10.   Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.
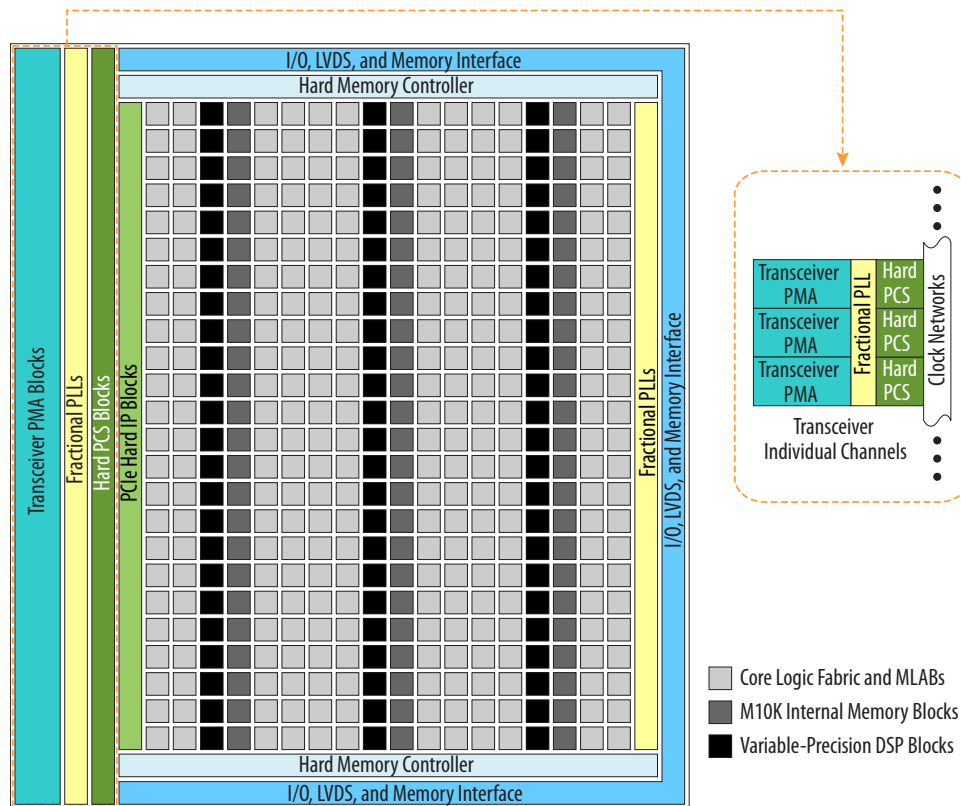
PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 22.   PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	• Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization • No decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23.   Transceiver PCS Features for Cyclone V Devices

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
3-Gbps and 6-Gbps Basic	0.614 to 6.144	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Transmitter bit-slip	• Word aligner • Deskew FIFO • Rate-match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • Receiver phase compensation FIFO
PCIe Gen1 (x1, x2, x4) PCIe Gen2 (x1, x2, x4)[12]	2.5 and 5.0	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic
GbE	1.25	• Custom PHY IP core with preset feature • GbE transmitter synchronization state machine	• Custom PHY IP core with preset feature • GbE receiver synchronization state machine
XAUI [13] HiGig	3.125 3.75	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for bonding four channels	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for realigning four channels
SRIO 1.3 and 2.1	1.25 to 3.125	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 channel bonding	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 deskew state machine
SDI, SD/HD, and 3G-SDI JESD204A	0.27[14], 1.485, and 2.97 0.3125[15] to 3.125	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature

continued...

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[12] PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

[13] XAUI is supported through the soft PCS.

[14] The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

[15] The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Serial ATA Gen1 and Gen2	1.5 and 3.0	• Custom PHY IP core with preset feature • Electrical idle	• Custom PHY IP core with preset feature • Signal detect • Wider spread of asynchronous SSC
CPRI 4.1[16]	0.6144 to 6.144	• Dedicated deterministic latency PHY IP core • Transmitter (TX) manual bit-slip mode	• Dedicated deterministic latency PHY IP core • Receiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072		
V-by-One HS	Up to 3.75	Custom PHY IP core	• Custom PHY IP core • Wider spread of asynchronous SSC
DisplayPort 1.2[17]	1.62 and 2.7		

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor

- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard

- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

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[16] High-voltage output mode (1000-BASE-CX) is not supported.

[17] Pending characterization.

Figure 11.   HPS with Dual-Core Arm Cortex-A9 MPCore Processor
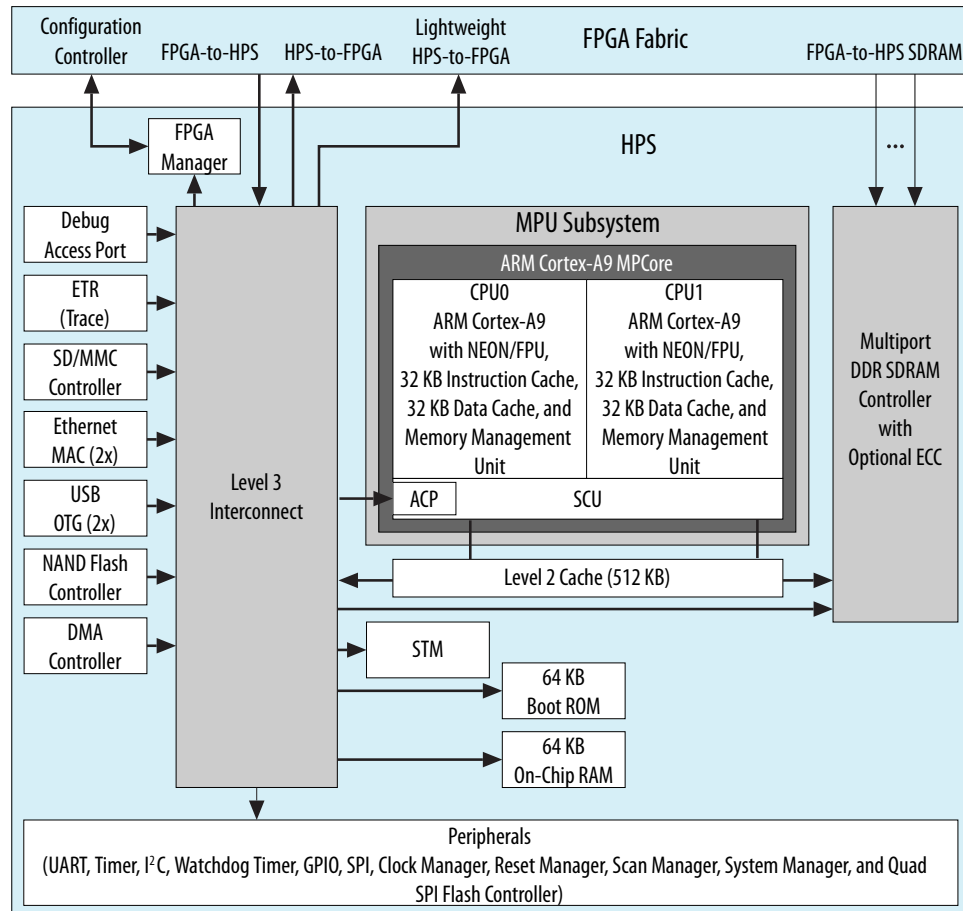
System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.
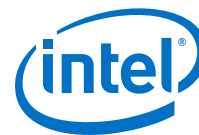
Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

Cyclone V Device Family Pin Connection Guidelines
Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

International Altera Sales Support Offices

Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial Reconfiguration

Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.

- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the *Sample Ordering Code and Available Options* diagrams. • Rebranded as Intel.

Date	Version	Changes
December 2017	2017.12.18	• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.
June 2016	2016.06.10	Updated Cyclone V GT speed grade to −7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	• Added descriptions to package plan tables for Cyclone V GT and ST devices. • Changed instances of *Quartus II* to *Quartus Prime*.

June 2015	2015.06.12	• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives.
		• Updated logic elements (LE) (K) for the following devices:
		  — Cyclone V E A7: Updated from 149.5 to 150
		  — Cyclone V GX C3: Updated from 35.5 to 36
		  — Cyclone V GX C7: Updated from 149.7 to 150
		  — Cyclone V GT D7: Updated from 149.5 to 150
		• Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows:
		  — Cyclone V GX C3: Updated from 291 to 182
		  — Cyclone V GX C4: Updated from 678 to 424
		  — Cyclone V GX C5: Updated from 678 to 424
		  — Cyclone V GX C7: Updated from 1,338 to 836
		  — Cyclone V GX C9: Updated from 2,748 to 1,717

Date	Version	Changes
		• Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C3: Updated from 181 to 182 — Cyclone V GX C4: Updated from 295 to 424 • Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C3: Updated from 1,531 to 1,532 — Cyclone V GX C4: Updated from 2,795 to 2,924 • Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C4: Updated from 472 to 678 — Cyclone V GX C5: Updated from 679 to 678
March 2015	2015.03.31	• Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table. • Added optional suffix "SC: Internal scrubbing support" to the following diagrams: — Sample Ordering Code and Available Options for Cyclone V E Devices — Sample Ordering Code and Available Options for Cyclone V GX Devices — Sample Ordering Code and Available Options for Cyclone V SE Devices — Sample Ordering Code and Available Options for Cyclone V SX Devices
January 2015	2015.01.23	• Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and −7 speed grade. — Operating Temperature: Removed C and A temperature grades — FPGA Fabric Speed Grade: Removed −6 and −8 speed grades • Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps: — Device Variants for the Cyclone V Device Family table — Sample Ordering Code and Available Options for Cyclone V ST Devices figure — Maximum Resource Counts for Cyclone V ST Devices • Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices. — Logic elements (LE) (K): Updated from 35.7 to 35.5 — Variable-precision DSP block: Updated from 51 to 57 — 18 x 18 multiplier: Updated from 102 to 114 • Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. — Variableprecision DSP Block: Updated from 51 to 57 — 9 x 9 Multiplier: Updated from 153 to 171 — 18 x 18 Multiplier: Updated from 102 to 114 — 27 x 27 Multiplier: Updated from 51 to 57 — 18 x 18 Multiplier Adder Mode: Updated from 51 to 57 — 18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57 • Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices. — M10K block: Updated from 119 to 135 — M10K RAM bit (Kb): Updated from 1,190 to 1,350 — MLAB block: Updated from 255 to 291 — MLAB RAM bit (Kb): Updated from 159 to 181 — Total RAM bit (Kb): Updated from 1,349 to 1,531
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.
		continued...

Date	Version	Changes
		• Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. • Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. • Text edits throughout the document.
February 2012	1.2	• Updated Table 1–2, Table 1–3, and Table 1–6. • Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15. • Updated Figure 1–1 and Figure 1–6.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. • Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8. • Updated "System Peripherals" on page 1–18, "HPS–FPGA AXI Bridges" on page 1–19, "HPS SDRAM Controller Subsystem" on page 1–19, "FPGA Configuration and Processor Booting" on page 1–19, and "Hardware and Software Development" on page 1–20. • Minor text edits.
October 2011	1.0	Initial release.