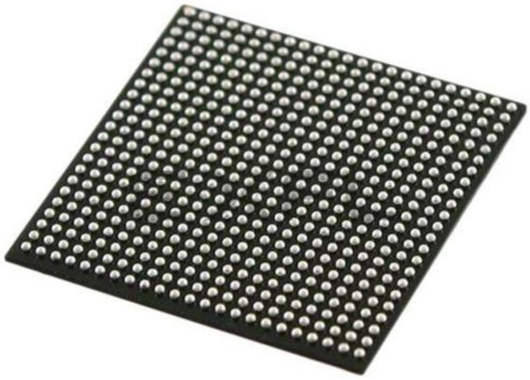
# Intel - 5CGXFC7C6U19I7N Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 56480 |
| Number of Logic Elements/Cells | 149500 |
| Total RAM Bits | 7880704 |
| Number of I/O | 240 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-FBGA |
| Supplier Device Package | 484-UBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5cgxfc7c6u19i7n |

# Contents

# Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

### Related Information

Cyclone V Device Handbook: Known Issues
Lists the planned updates to the Cyclone V Device Handbook chapters.

## Key Advantages of Cyclone V Devices

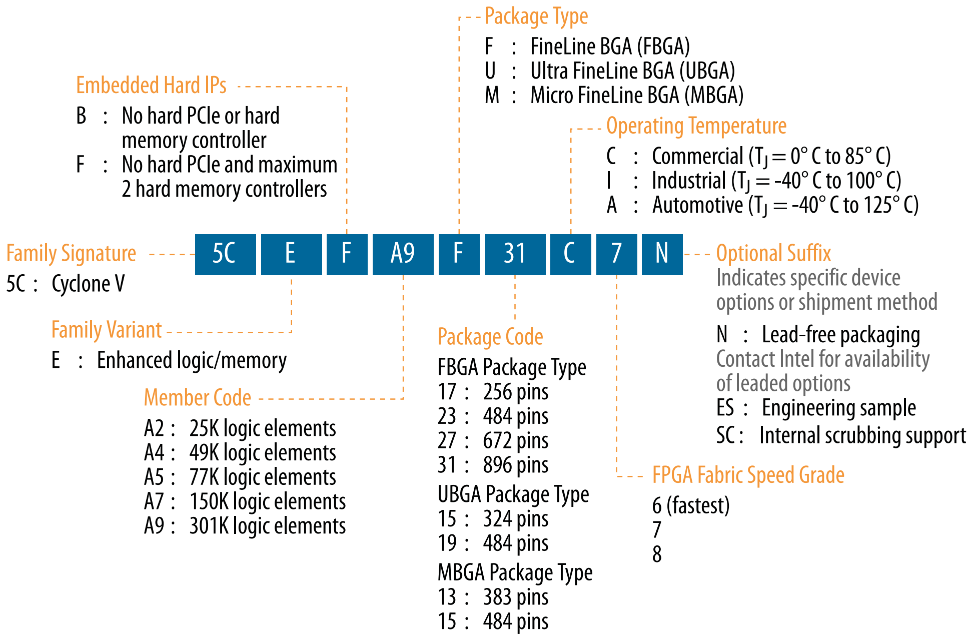
**Table 1. Key Advantages of the Cyclone V Device Family**

| Advantage | Supporting Feature |
|---|---|
| Lower power consumption | • Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks<br>• Up to 40% lower power consumption than the previous generation device |
| Improved logic integration and differentiation capabilities | • 8-input adaptive logic module (ALM)<br>• Up to 13.59 megabits (Mb) of embedded memory<br>• Variable-precision digital signal processing (DSP) blocks |
| Increased bandwidth capacity | • 3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers<br>• Hard memory controllers |
| Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor | • Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC)<br>• Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Lowest system cost | • Requires only two core voltages to operate<br>• Available in low-cost wirebond packaging<br>• Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration |

## Available Options

### Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Maximum Resources

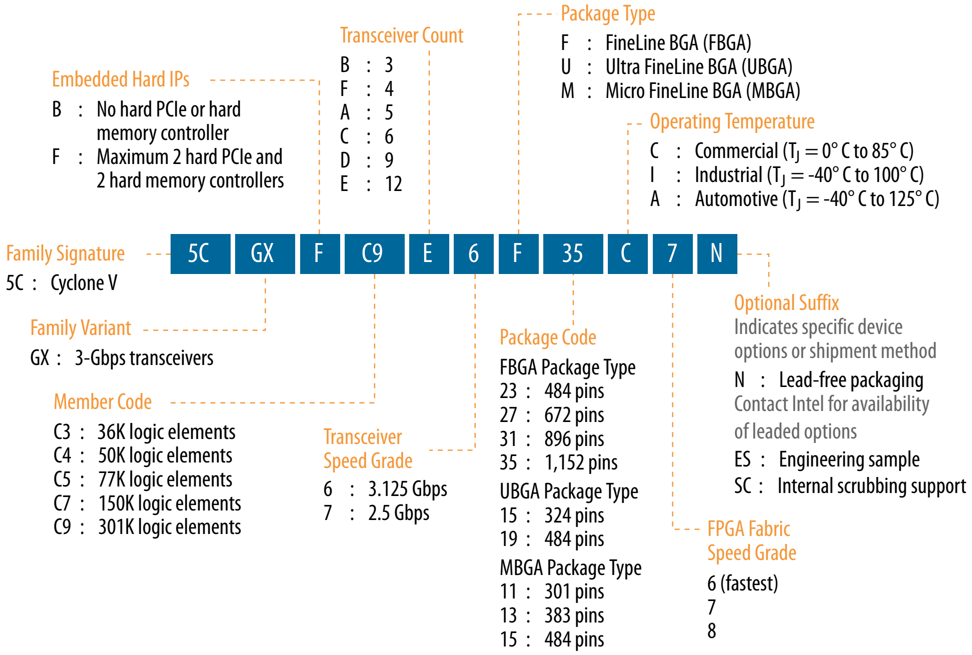
### Table 4. Maximum Resource Counts for Cyclone V E Devices

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | A2 | A4 | A5 | A7 | A9 |
| Logic Elements (LE) (K) | | 25 | 49 | 77 | 150 | 301 |
| ALM | | 9,430 | 18,480 | 29,080 | 56,480 | 113,560 |
| Register | | 37,736 | 73,920 | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 1,760 | 3,080 | 4,460 | 6,860 | 12,200 |
| | MLAB | 196 | 303 | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 25 | 66 | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 50 | 132 | 300 | 312 | 684 |
| PLL | | 4 | 4 | 6 | 7 | 8 |
| GPIO | | 224 | 224 | 240 | 480 | 480 |
| LVDS | Transmitter | 56 | 56 | 60 | 120 | 120 |
| | Receiver | 56 | 56 | 60 | 120 | 120 |
| Hard Memory Controller | | 1 | 1 | 2 | 2 | 2 |

## Available Options

### Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Maximum Resources

### Table 6. Maximum Resource Counts for Cyclone V GX Devices

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | C3 | C4 | C5 | C7 | C9 |
| Logic Elements (LE) (K) | | 36 | 50 | 77 | 150 | 301 |
| ALM | | 13,460 | 18,860 | 29,080 | 56,480 | 113,560 |
| Register | | 53,840 | 75,440 | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 1,350 | 2,500 | 4,460 | 6,860 | 12,200 |
| | MLAB | 182 | 424 | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 57 | 70 | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 114 | 140 | 300 | 312 | 684 |
| PLL | | 4 | 6 | 6 | 7 | 8 |
| 3 Gbps Transceiver | | 3 | 6 | 6 | 9 | 12 |
| GPIO(4) | | 208 | 336 | 336 | 480 | 560 |

*continued...*

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(4) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | C3 | C4 | C5 | C7 | C9 |
| LVDS | Transmitter | 52 | 84 | 84 | 120 | 140 |
| | Receiver | 52 | 84 | 84 | 120 | 140 |
| PCIe Hard IP Block | | 1 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 1 | 2 | 2 | 2 | 2 |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 7. Package Plan for Cyclone V GX Devices

| Member Code | M301 (11 mm) | | M383 (13 mm) | | M484 (15 mm) | | U324 (15 mm) | | U484 (19 mm) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| C3 | — | — | — | — | — | — | 144 | 3 | 208 | 3 |
| C4 | 129 | 4 | 175 | 6 | — | — | — | — | 224 | 6 |
| C5 | 129 | 4 | 175 | 6 | — | — | — | — | 224 | 6 |
| C7 | — | — | — | — | 240 | 3 | — | — | 240 | 6 |
| C9 | — | — | — | — | — | — | — | — | 240 | 5 |

| Member Code | F484 (23 mm) | | F672 (27 mm) | | F896 (31 mm) | | F1152 (35 mm) | |
|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| C3 | 208 | 3 | — | — | — | — | — | — |
| C4 | 240 | 6 | 336 | 6 | — | — | — | — |
| C5 | 240 | 6 | 336 | 6 | — | — | — | — |
| C7 | 240 | 6 | 336 | 9 | 480 | 9 | — | — |
| C9 | 224 | 6 | 336 | 9 | 480 | 12 | 560 | 12 |

# Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

Product Selector Guide
Provides the latest information about Intel products.

# Cyclone V SE

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

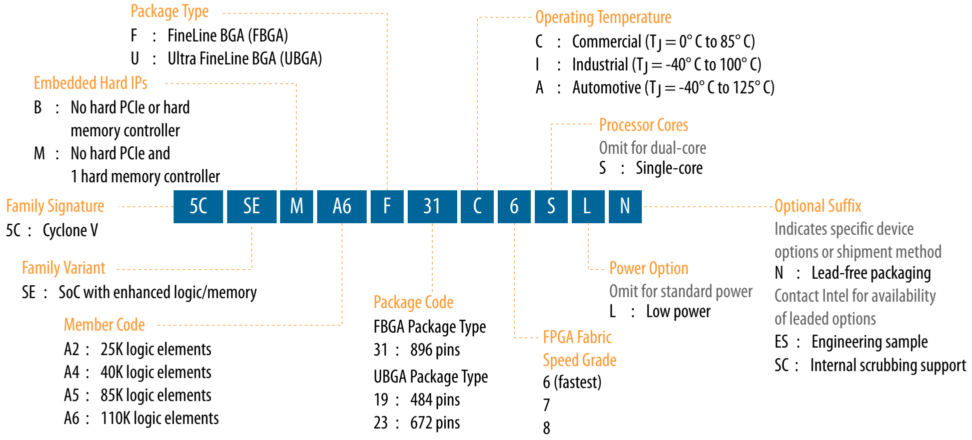
Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 4. Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



## Maximum Resources

### Table 10. Maximum Resource Counts for Cyclone V SE Devices

| Resource | | Member Code | | | |
|---|---|---|---|---|---|
| | | A2 | A4 | A5 | A6 |
| Logic Elements (LE) (K) | | 25 | 40 | 85 | 110 |
| ALM | | 9,430 | 15,880 | 32,070 | 41,910 |
| Register | | 37,736 | 60,376 | 128,300 | 166,036 |
| Memory (Kb) | M10K | 1,400 | 2,700 | 3,970 | 5,570 |
| | MLAB | 138 | 231 | 480 | 621 |
| Variable-precision DSP Block | | 36 | 84 | 87 | 112 |
| 18 x 18 Multiplier | | 72 | 168 | 174 | 224 |
| FPGA PLL | | 5 | 5 | 6 | 6 |
| HPS PLL | | 3 | 3 | 3 | 3 |
| FPGA GPIO | | 145 | 145 | 288 | 288 |
| HPS I/O | | 181 | 181 | 181 | 181 |
| LVDS | Transmitter | 32 | 32 | 72 | 72 |
| | Receiver | 37 | 37 | 72 | 72 |
| FPGA Hard Memory Controller | | 1 | 1 | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Single- or dual-core | Single- or dual-core | Single- or dual-core | Single- or dual-core |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 11. Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | U484 (19 mm) | | U672 (23 mm) | | F896 (31 mm) | |
|---|---|---|---|---|---|---|
| | FPGA GPIO | HPS I/O | FPGA GPIO | HPS I/O | FPGA GPIO | HPS I/O |
| A2 | 66 | 151 | 145 | 181 | — | — |
| A4 | 66 | 151 | 145 | 181 | — | — |
| A5 | 66 | 151 | 145 | 181 | 288 | 181 |
| A6 | 66 | 151 | 145 | 181 | 288 | 181 |

# Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

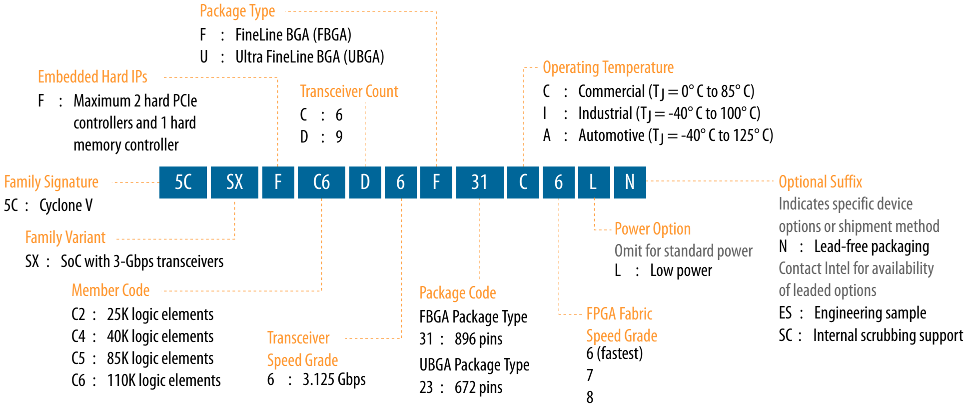
Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



## Maximum Resources

### Table 12. Maximum Resource Counts for Cyclone V SX Devices

| Resource | | Member Code | | | |
|---|---|---|---|---|---|
| | | C2 | C4 | C5 | C6 |
| Logic Elements (LE) (K) | | 25 | 40 | 85 | 110 |
| ALM | | 9,430 | 15,880 | 32,070 | 41,910 |
| Register | | 37,736 | 60,376 | 128,300 | 166,036 |
| Memory (Kb) | M10K | 1,400 | 2,700 | 3,970 | 5,570 |
| | MLAB | 138 | 231 | 480 | 621 |
| Variable-precision DSP Block | | 36 | 84 | 87 | 112 |
| 18 x 18 Multiplier | | 72 | 168 | 174 | 224 |
| FPGA PLL | | 5 | 5 | 6 | 6 |

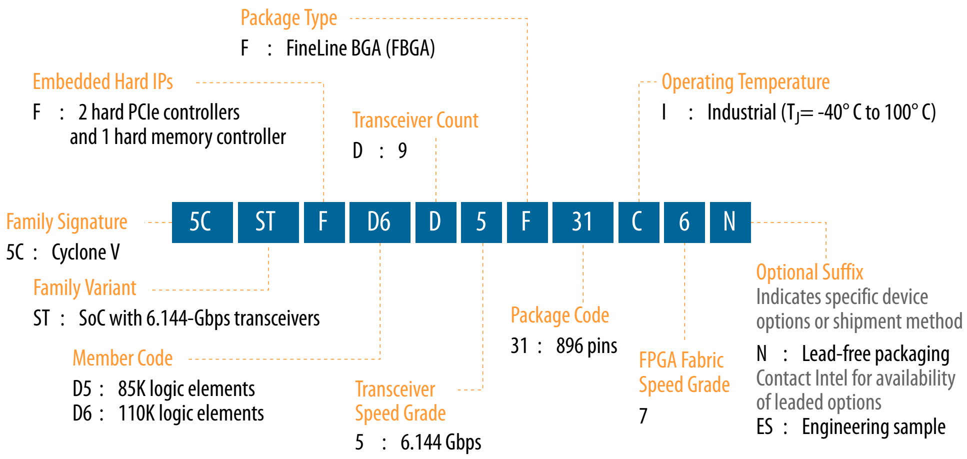
***continued...***

### Related Information

Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices



## Maximum Resources

### Table 14. Maximum Resource Counts for Cyclone V ST Devices

| Resource | | Member Code | |
|---|---|---|---|
| | | D5 | D6 |
| Logic Elements (LE) (K) | | 85 | 110 |
| ALM | | 32,070 | 41,910 |
| Register | | 128,300 | 166,036 |
| Memory (Kb) | M10K | 3,970 | 5,570 |
| | MLAB | 480 | 621 |
| Variable-precision DSP Block | | 87 | 112 |
| 18 x 18 Multiplier | | 174 | 224 |
| FPGA PLL | | 6 | 6 |
| HPS PLL | | 3 | 3 |
| 6.144 Gbps Transceiver | | 9 | 9 |
| FPGA GPIO(10) | | 288 | 288 |
| HPS I/O | | 181 | 181 |
| LVDS | Transmitter | 72 | 72 |

*continued...*

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(10) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

| Resource | | Member Code | |
|---|---|---|---|
| | | D5 | D6 |
| | Receiver | 72 | 72 |
| PCIe Hard IP Block | | 2 | 2 |
| FPGA Hard Memory Controller | | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Dual-core | Dual-core |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | F896 (31 mm) | | |
|---|---|---|---|
| | FPGA GPIO | HPS I/O | XCVR |
| D5 | 288 | 181 | 9 (11) |
| D6 | 288 | 181 | 9 (11) |

### Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

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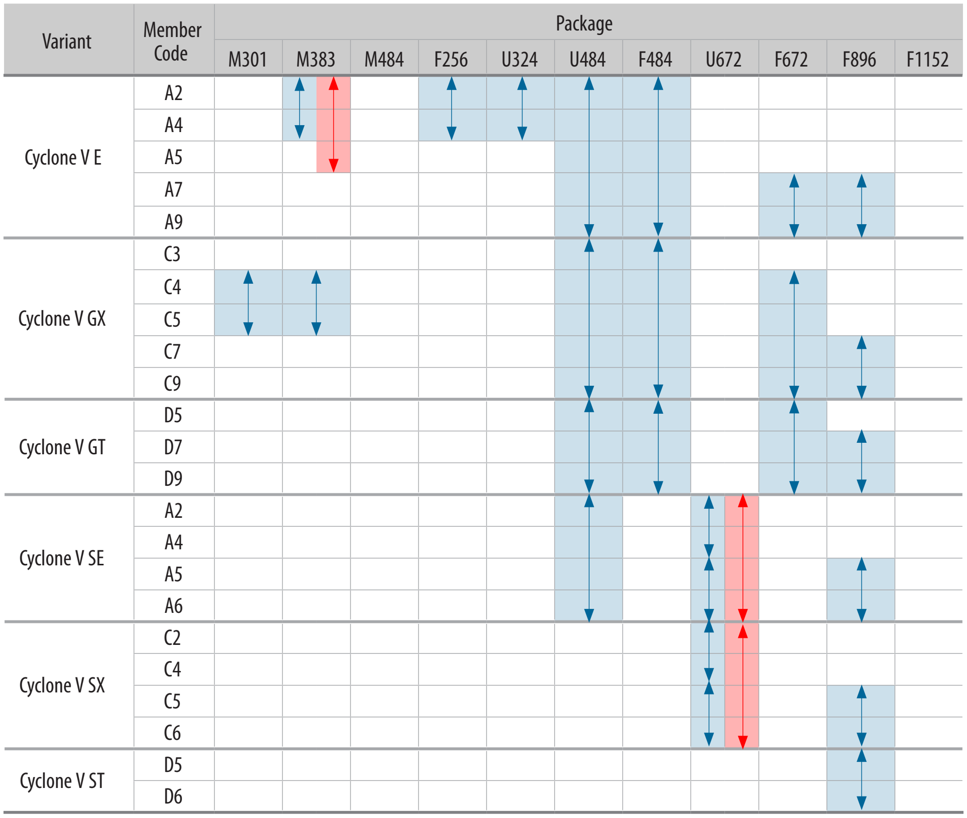
(11) If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

## I/O Vertical Migration for Cyclone V Devices

**Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities**

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.



| Variant | Member Code | Package | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | M301 | M383 | M484 | F256 | U324 | U484 | F484 | U672 | F672 | F896 | F1152 |
| Cyclone V E | A2 | | ▨ 🟥 | | ▨ | ▨ | ▨ | ▨ | | | | |
| | A4 | | ▨ 🟥 | | ▨ | ▨ | ▨ | ▨ | | | | |
| | A5 | | 🟥 | | | | ▨ | ▨ | | | | |
| | A7 | | | | | | ▨ | ▨ | | ▨ | ▨ | |
| | A9 | | | | | | ▨ | ▨ | | ▨ | ▨ | |
| Cyclone V GX | C3 | | | | | | ▨ | ▨ | | | | |
| | C4 | ▨ | ▨ | | | | ▨ | ▨ | | ▨ | | |
| | C5 | ▨ | ▨ | | | | ▨ | ▨ | | ▨ | | |
| | C7 | | | | | | ▨ | ▨ | | ▨ | ▨ | |
| | C9 | | | | | | ▨ | ▨ | | ▨ | ▨ | |
| Cyclone V GT | D5 | | | | | | ▨ | ▨ | | ▨ | | |
| | D7 | | | | | | ▨ | ▨ | | ▨ | ▨ | |
| | D9 | | | | | | ▨ | ▨ | | ▨ | ▨ | |
| Cyclone V SE | A2 | | | | | | ▨ | | ▨ 🟥 | | | |
| | A4 | | | | | | ▨ | | ▨ 🟥 | | | |
| | A5 | | | | | | ▨ | | ▨ 🟥 | | ▨ | |
| | A6 | | | | | | ▨ | | ▨ 🟥 | | ▨ | |
| Cyclone V SX | C2 | | | | | | | | ▨ 🟥 | | | |
| | C4 | | | | | | | | ▨ 🟥 | | | |
| | C5 | | | | | | | | ▨ 🟥 | | ▨ | |
| | C6 | | | | | | | | ▨ 🟥 | | ▨ | |
| Cyclone V ST | D5 | | | | | | | | | | ▨ | |
| | D6 | | | | | | | | | | ▨ | |

You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

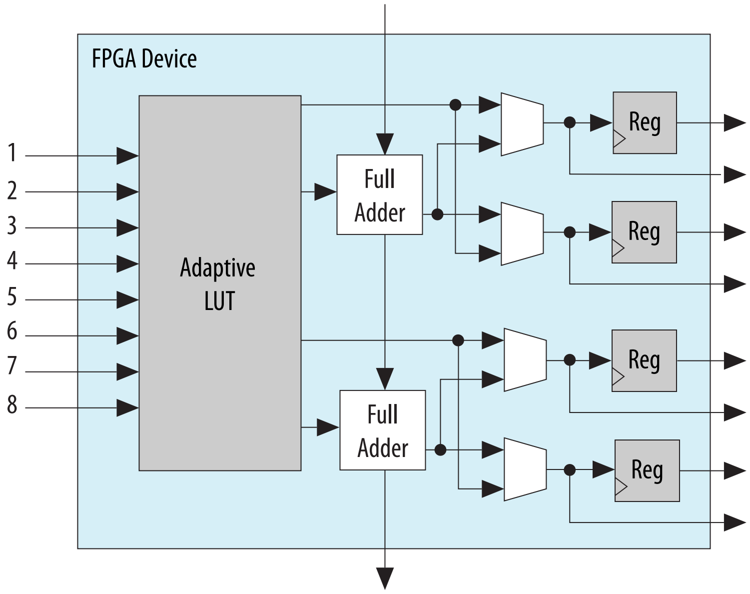
*Note:* To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

## Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

**Figure 8. ALM for Cyclone V Devices**



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

**Related Information**

Embedded Memory Capacity in Cyclone V Devices on page 21
Lists the embedded memory capacity for each device.

## Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

### Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

| Usage Example | Multiplier Size (Bit) | DSP Block Resource |
|---|---|---|
| Low precision fixed point for video applications | Three 9 x 9 | 1 |
| Medium precision fixed point in FIR filters | Two 18 x 18 | 1 |
| FIR filters and general DSP usage | Two 18 x 18 with accumulate | 1 |
| High precision fixed- or floating-point implementations | One 27 x 27 with accumulate | 1 |

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

### Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

| Variant | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---|---|---|---|---|---|---|---|
| | | | 9 x 9 Multiplier | 18 x 18 Multiplier | 27 x 27 Multiplier | | |
| Cyclone V E | A2 | 25 | 75 | 50 | 25 | 25 | 25 |
| | A4 | 66 | 198 | 132 | 66 | 66 | 66 |
| | A5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | A7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | A9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GX | C3 | 57 | 171 | 114 | 57 | 57 | 57 |
| | C4 | 70 | 210 | 140 | 70 | 70 | 70 |
| | C5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | C7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | C9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GT | D5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | D7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | D9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V SE | A2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | A4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | A5 | 87 | 261 | 174 | 87 | 87 | 87 |
| | A6 | 112 | 336 | 224 | 112 | 112 | 112 |
| Cyclone V SX | C2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | C4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | C5 | 87 | 261 | 174 | 87 | 87 | 87 |

*continued...*

| Variant | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---|---|---|---|---|---|---|---|
| | | | 9 x 9 Multiplier | 18 x 18 Multiplier | 27 x 27 Multiplier | | |
| | C6 | 112 | 336 | 224 | 112 | 112 | 112 |
| Cyclone V ST | D5 | 87 | 261 | 174 | 87 | 87 | 87 |
| | D6 | 112 | 336 | 224 | 112 | 112 | 112 |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Types of Embedded Memory

The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks—blocks of dedicated memory resources. The M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Cyclone V Devices

### Table 18. Embedded Memory Capacity and Distribution in Cyclone V Devices

| Variant | Member Code | M10K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Cyclone V E | A2 | 176 | 1,760 | 314 | 196 | 1,956 |
| | A4 | 308 | 3,080 | 485 | 303 | 3,383 |
| | A5 | 446 | 4,460 | 679 | 424 | 4,884 |
| | A7 | 686 | 6,860 | 1338 | 836 | 7,696 |
| | A9 | 1,220 | 12,200 | 2748 | 1,717 | 13,917 |
| Cyclone V GX | C3 | 135 | 1,350 | 291 | 182 | 1,532 |
| | C4 | 250 | 2,500 | 678 | 424 | 2,924 |
| | C5 | 446 | 4,460 | 678 | 424 | 4,884 |
| | C7 | 686 | 6,860 | 1338 | 836 | 7,696 |
| | C9 | 1,220 | 12,200 | 2748 | 1,717 | 13,917 |

*continued...*

| Variant | Member Code | M10K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Cyclone V GT | D5 | 446 | 4,460 | 679 | 424 | 4,884 |
| | D7 | 686 | 6,860 | 1338 | 836 | 7,696 |
| | D9 | 1,220 | 12,200 | 2748 | 1,717 | 13,917 |
| Cyclone V SE | A2 | 140 | 1,400 | 221 | 138 | 1,538 |
| | A4 | 270 | 2,700 | 370 | 231 | 2,460 |
| | A5 | 397 | 3,970 | 768 | 480 | 4,450 |
| | A6 | 553 | 5,530 | 994 | 621 | 6,151 |
| Cyclone V SX | C2 | 140 | 1,400 | 221 | 138 | 1,538 |
| | C4 | 270 | 2,700 | 370 | 231 | 2,460 |
| | C5 | 397 | 3,970 | 768 | 480 | 4,450 |
| | C6 | 553 | 5,530 | 994 | 621 | 6,151 |
| Cyclone V ST | D5 | 397 | 3,970 | 768 | 480 | 4,450 |
| | D6 | 553 | 5,530 | 994 | 621 | 6,151 |

## Embedded Memory Configurations

### Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|---|---|---|
| MLAB | 32 | x16, x18, or x20 |
| M10K | 256 | x40 or x32 |
| | 512 | x20 or x16 |
| | 1K | x10 or x8 |
| | 2K | x5 or x4 |
| | 4K | x2 |
| | 8K | x1 |

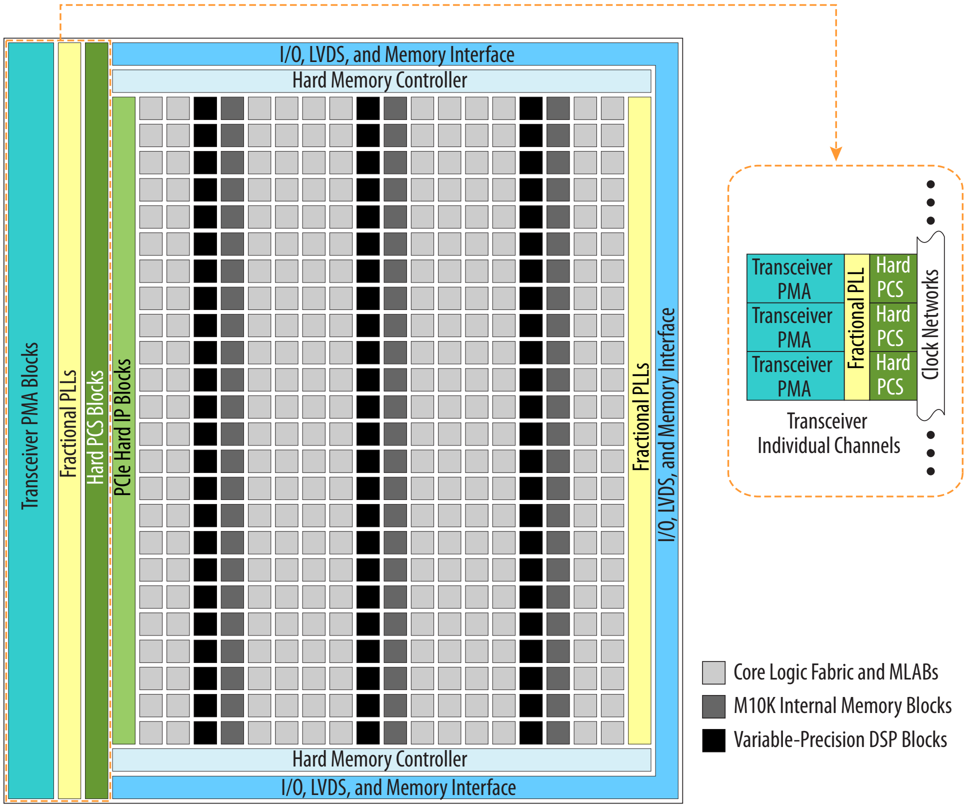
## Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

*Note:* To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

## Figure 10. Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



## PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

## Table 22. PMA Features of the Transceivers in Cyclone V Devices

| Features | Capability |
|---|---|
| Backplane support | Driving capability up to 6.144 Gbps |
| PLL-based clock recovery | Superior jitter tolerance |
| Programmable deserialization and word alignment | Flexible deserialization width and configurable word alignment pattern |
| Equalization and pre-emphasis | • Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization<br>• No decision feedback equalizer (DFE) |
| Ring oscillator transmit PLLs | 614 Mbps to 6.144 Gbps |
| Input reference clock range | 20 MHz to 400 MHz |
| Transceiver dynamic reconfiguration | Allows the reconfiguration of a single channel without affecting the operation of other channels |

| PCS Support | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|---|---|---|---|
| Serial ATA Gen1 and Gen2 | 1.5 and 3.0 | • Custom PHY IP core with preset feature<br>• Electrical idle | • Custom PHY IP core with preset feature<br>• Signal detect<br>• Wider spread of asynchronous SSC |
| CPRI 4.1(16) | 0.6144 to 6.144 | • Dedicated deterministic latency PHY IP core<br>• Transmitter (TX) manual bit-slip mode | • Dedicated deterministic latency PHY IP core<br>• Receiver (RX) deterministic latency state machine |
| OBSAI RP3 | 0.768 to 3.072 | | |
| V-by-One HS | Up to 3.75 | Custom PHY IP core | • Custom PHY IP core<br>• Wider spread of asynchronous SSC |
| DisplayPort 1.2(17) | 1.62 and 2.7 | | |

## SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

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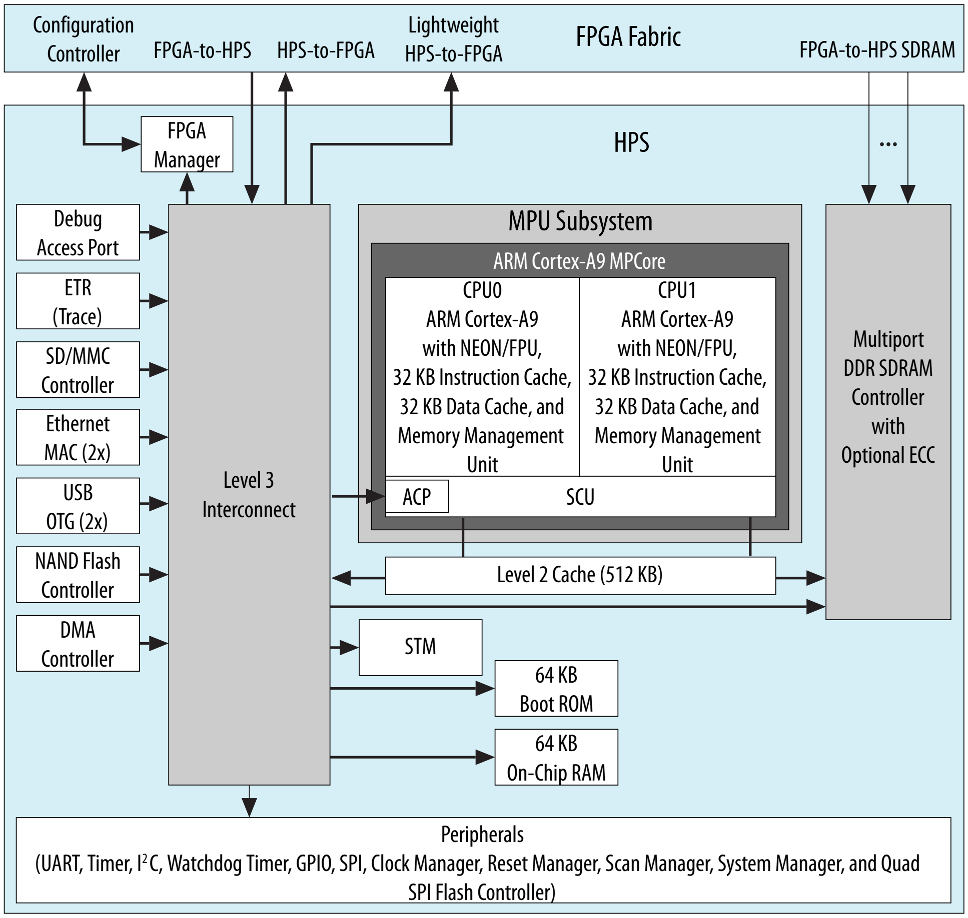
(16) High-voltage output mode (1000-BASE-CX) is not supported.

(17) Pending characterization.

**Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor**



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

## Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

**Table 24. Configuration Schemes and Features Supported by Cyclone V Devices**

| Mode | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) | Decompression | Design Security | Partial Reconfiguration[18] | Remote System Update |
|---|---|---|---|---|---|---|---|
| AS through the EPCS and EPCQ serial configuration device | 1 bit, 4 bits | 100 | — | Yes | Yes | — | Yes |
| PS through CPLD or external microcontroller | 1 bit | 125 | 125 | Yes | Yes | — | — |
| FPP | 8 bits | 125 | — | Yes | Yes | — | Parallel flash loader |
| | 16 bits | 125 | — | Yes | Yes | Yes | |
| CvP (PCIe) | x1, x2, and x4 lanes | — | — | Yes | Yes | Yes | — |
| JTAG | 1 bit | 33 | 33 | — | — | — | — |

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

### Related Information

Configuration via Protocol (CvP) Implementation in Intel FPGAs User Guide
Provides more information about CvP.

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(18) The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

| Date | Version | Changes |
|---|---|---|
| | | • Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<br>— Cyclone V GX C3: Updated from 181 to 182<br>— Cyclone V GX C4: Updated from 295 to 424<br>• Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<br>— Cyclone V GX C3: Updated from 1,531 to 1,532<br>— Cyclone V GX C4: Updated from 2,795 to 2,924<br>• Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<br>— Cyclone V GX C4: Updated from 472 to 678<br>— Cyclone V GX C5: Updated from 679 to 678 |
| March 2015 | 2015.03.31 | • Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table.<br>• Added optional suffix "SC: Internal scrubbing support" to the following diagrams:<br>— Sample Ordering Code and Available Options for Cyclone V E Devices<br>— Sample Ordering Code and Available Options for Cyclone V GX Devices<br>— Sample Ordering Code and Available Options for Cyclone V SE Devices<br>— Sample Ordering Code and Available Options for Cyclone V SX Devices |
| January 2015 | 2015.01.23 | • Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and –7 speed grade.<br>— Operating Temperature: Removed C and A temperature grades<br>— FPGA Fabric Speed Grade: Removed –6 and –8 speed grades<br>• Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps:<br>— Device Variants for the Cyclone V Device Family table<br>— Sample Ordering Code and Available Options for Cyclone V ST Devices figure<br>— Maximum Resource Counts for Cyclone V ST Devices<br>• Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices.<br>— Logic elements (LE) (K): Updated from 35.7 to 35.5<br>— Variable-precision DSP block: Updated from 51 to 57<br>— 18 x 18 multiplier: Updated from 102 to 114<br>• Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices.<br>— Variableprecision DSP Block: Updated from 51 to 57<br>— 9 x 9 Multiplier: Updated from 153 to 171<br>— 18 x 18 Multiplier: Updated from 102 to 114<br>— 27 x 27 Multiplier: Updated from 51 to 57<br>— 18 x 18 Multiplier Adder Mode: Updated from 51 to 57<br>— 18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57<br>• Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices.<br>— M10K block: Updated from 119 to 135<br>— M10K RAM bit (Kb): Updated from 1,190 to 1,350<br>— MLAB block: Updated from 255 to 291<br>— MLAB RAM bit (Kb): Updated from 159 to 181<br>— Total RAM bit (Kb): Updated from 1,349 to 1,531 |
| October 2014 | 2014.10.06 | Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices. |

***continued...***