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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 25K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba2u19i7n



Feature	Description
	<ul style="list-style-type: none"> HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller Arm CoreSight™ JTAG debug access port, trace port, and on-chip trace storage
Configuration	<ul style="list-style-type: none"> Tamper protection—comprehensive design protection to protect your valuable IP investments Enhanced advanced encryption standard (AES) design security features CvP Dynamic reconfiguration of the FPGA Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options Internal scrubbing ⁽²⁾ Partial reconfiguration ⁽³⁾

Cyclone V Device Variants and Packages

Table 3. Device Variants for the Cyclone V Device Family

Variant	Description
Cyclone V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone V SE	SoC with integrated Arm-based HPS
Cyclone V SX	SoC with integrated Arm-based HPS and 3.125 Gbps transceivers
Cyclone V ST	SoC with integrated Arm-based HPS and 6.144 Gbps transceivers

Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

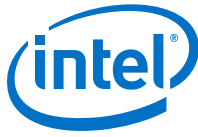
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

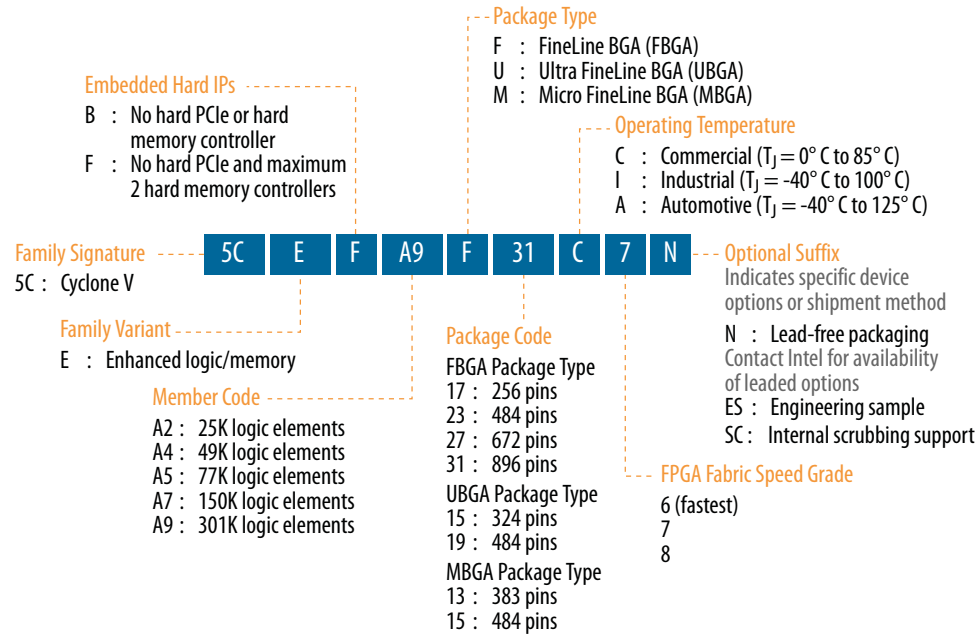
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- ⁽²⁾ The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.
- ⁽³⁾ The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel® sales representatives.



Available Options

Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

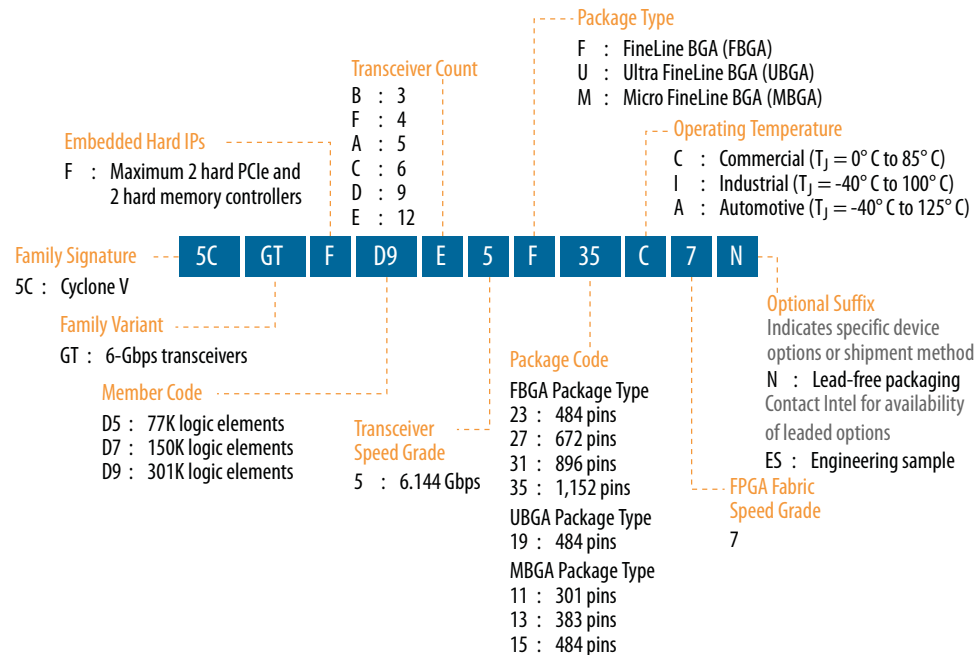
Table 4. Maximum Resource Counts for Cyclone V E Devices

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	150	301
ALM		9,430	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO		224	224	240	480	480
LVDS	Transmitter	56	56	60	120	120
	Receiver	56	56	60	120	120
Hard Memory Controller		1	1	2	2	2



Available Options

Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices



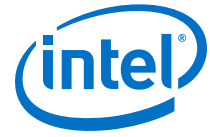
Maximum Resources

Table 8. Maximum Resource Counts for Cyclone V GT Devices

Resource		Member Code		
		D5	D7	D9
Logic Elements (LE) (K)		77	150	301
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DSP Block		150	156	342
18 x 18 Multiplier		300	312	684
PLL		6	7	8
6 Gbps Transceiver		6	9	12
GPIO ⁽⁵⁾		336	480	560
LVDS	Transmitter	84	120	140

continued...

⁽⁵⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



Resource		Member Code		
		D5	D7	D9
	Receiver	84	120	140
PCIe Hard IP Block		2	2	2
Hard Memory Controller		2	2	2

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 9. Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	129	4	175	6	—	—	224	6
D7	—	—	—	—	240	3	240	6
D9	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	240	6	336	6	—	—	—	—
D7	240	6	336	9 ⁽⁶⁾	480	9 ⁽⁶⁾	—	—
D9	224	6	336	9 ⁽⁶⁾	480	12 ⁽⁷⁾	560	12 ⁽⁷⁾

Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

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- ⁽⁶⁾ If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.
- ⁽⁷⁾ If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.



Maximum Resources

Table 10. Maximum Resource Counts for Cyclone V SE Devices

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 11. Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O
A2	66	151	145	181	—	—
A4	66	151	145	181	—	—
A5	66	151	145	181	288	181
A6	66	151	145	181	288	181



Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 12. Maximum Resource Counts for Cyclone V SX Devices

Resource		Member Code			
		C2	C4	C5	C6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
continued...					



Resource		Member Code			
		C2	C4	C5	C6
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO ⁽⁸⁾		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 ⁽⁹⁾	2 ⁽⁹⁾
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

Package Plan

Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ 1 PCIe Hard IP Block in U672 package.



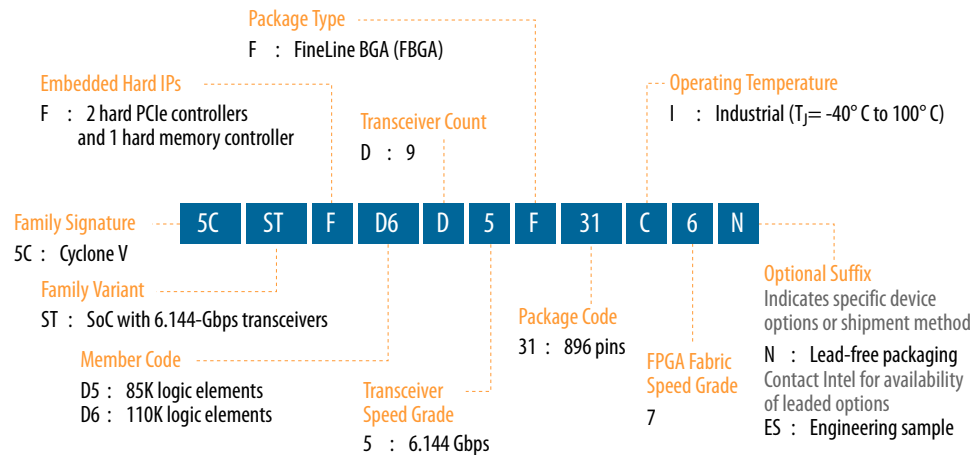
Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices



Maximum Resources

Table 14. Maximum Resource Counts for Cyclone V ST Devices

Resource		Member Code	
		D5	D6
Logic Elements (LE) (K)		85	110
ALM		32,070	41,910
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,570
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL		6	6
HPS PLL		3	3
6.144 Gbps Transceiver		9	9
FPGA GPIO ⁽¹⁰⁾		288	288
HPS I/O		181	181
LVDS	Transmitter	72	72
continued...			

⁽¹⁰⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



Resource		Member Code	
		D5	D6
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤ 5 Gbps. 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 ⁽¹¹⁾
D6	288	181	9 ⁽¹¹⁾

Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

⁽¹¹⁾ If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Figure 8. ALM for Cyclone V Devices



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

[Embedded Memory Capacity in Cyclone V Devices](#) on page 21
Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software



PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture



External Memory Performance

Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

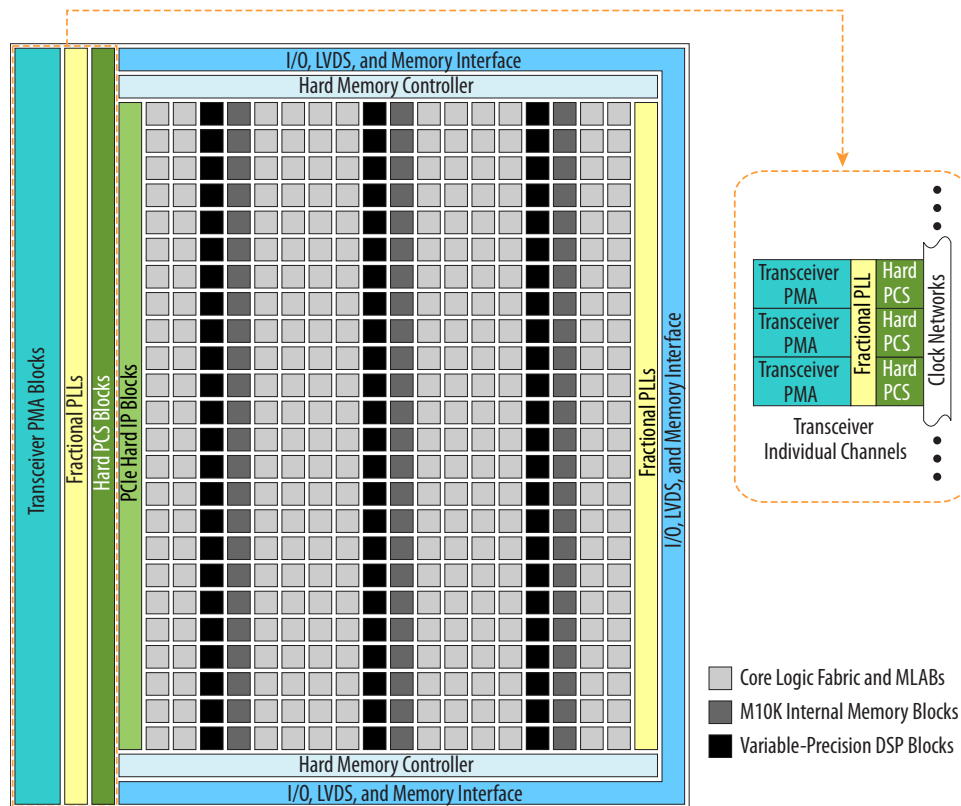
Cyclone V devices deliver the industry's lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

Figure 10. Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 22. PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	<ul style="list-style-type: none"> Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization No decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels



PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Serial ATA Gen1 and Gen2	1.5 and 3.0	<ul style="list-style-type: none">Custom PHY IP core with preset featureElectrical idle	<ul style="list-style-type: none">Custom PHY IP core with preset featureSignal detectWider spread of asynchronous SSC
CPRI 4.1 ⁽¹⁶⁾	0.6144 to 6.144	<ul style="list-style-type: none">Dedicated deterministic latency PHY IP coreTransmitter (TX) manual bit-slip mode	<ul style="list-style-type: none">Dedicated deterministic latency PHY IP coreReceiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072		
V-by-One HS	Up to 3.75	Custom PHY IP core	<ul style="list-style-type: none">Custom PHY IP coreWider spread of asynchronous SSC
DisplayPort 1.2 ⁽¹⁷⁾	1.62 and 2.7		

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

⁽¹⁶⁾ High-voltage output mode (1000-BASE-CX) is not supported.

⁽¹⁷⁾ Pending characterization.

Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor



System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.



Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

[Cyclone V Device Family Pin Connection Guidelines](#)

Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

[International Altera Sales Support Offices](#)

Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial Reconfiguration

Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

Table 24. Configuration Schemes and Features Supported by Cyclone V Devices

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration ⁽¹⁸⁾	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	
CvP (PCIe)	x1, x2, and x4 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Related Information

[Configuration via Protocol \(CvP\) Implementation in Intel FPGAs User Guide](#)

Provides more information about CvP.

⁽¹⁸⁾ The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Date	Version	Changes
July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	<ul style="list-style-type: none"> Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. Added link to Altera Product Selector for each device variant. Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120. Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84. Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168. Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252. Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37. Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5. Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. Added decompression support for the CvP configuration mode.
May 2013	2013.05.06	<ul style="list-style-type: none"> Added link to the known document issues in the Knowledge Base. Moved all links to the Related Information section of respective topics for easy reference. Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. Updated the package plan with M383 for the Cyclone V E device. Removed the M301 and M383 packages from the Cyclone V GX C4 device. Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. Updated 5 Gbps to '6.144 Gbps' for Cyclone V GT device.

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Date	Version	Changes
		<ul style="list-style-type: none"> Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6. Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices. Removed '36 x 36' from the Variable-Precision DSP Block. Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device. Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices. Updated Figure 7 which shows the I/O vertical migration table. Updated Table 17 for Cyclone V SX C4 device. Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. Removed 'Counter reconfiguration' from the PLL Features. Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps. Removed 'Distributed Memory' symbol. Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'. Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps. Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'. Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'. Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'. Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.
December 2012	2012.12.28	<ul style="list-style-type: none"> Updated the pin counts for the MBGA packages. Updated the GPIO and transceiver counts for the MBGA packages. Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices. Updated the vertical migration table for vertical migration of the U484 packages. Updated the MLAB supported programmable widths at 32 bits depth.
November 2012	2012.11.19	<ul style="list-style-type: none"> Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT. Added ordering code for five-transceiver devices for Cyclone V GT and ST. Updated the vertical migration table to add MBGA packages. Added performance information for HPS memory controller. Removed DDR3U support. Updated Cyclone V ST speed grade information. Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance. Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software. Updated template.
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	<ul style="list-style-type: none"> Restructured the document. Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. Added Table 1, Table 3, Table 16, Table 19, and Table 20. Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.

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Date	Version	Changes
		<ul style="list-style-type: none"> Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. Text edits throughout the document.
February 2012	1.2	<ul style="list-style-type: none"> Updated Table 1-2, Table 1-3, and Table 1-6. Updated "Cyclone V Family Plan" on page 1-4 and "Clock Networks and PLL Clock Sources" on page 1-15. Updated Figure 1-1 and Figure 1-6.
November 2011	1.1	<ul style="list-style-type: none"> Updated Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-5, and Table 1-6. Updated Figure 1-4, Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8. Updated "System Peripherals" on page 1-18, "HPS-FPGA AXI Bridges" on page 1-19, "HPS SDRAM Controller Subsystem" on page 1-19, "FPGA Configuration and Processor Booting" on page 1-19, and "Hardware and Software Development" on page 1-20. Minor text edits.
October 2011	1.0	Initial release.