Intel - 5CSEBA4U19C8SN Datasheet





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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Single ARM® Cortex®-A9 MPCore [™] with CoreSight [™]
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 40K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba4u19c8sn

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Cyclone V Device Overview

The Cyclone[®] V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

Related Information

Cyclone V Device Handbook: Known Issues Lists the planned updates to the Cyclone V Device Handbook chapters.

Key Advantages of Cyclone V Devices

Table 1. Key Advantages of the Cyclone V Device Family

Advantage	Supporting Feature
Lower power consumption	 Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks Up to 40% lower power consumption than the previous generation device
Improved logic integration and differentiation capabilities	 8-input adaptive logic module (ALM) Up to 13.59 megabits (Mb) of embedded memory Variable-precision digital signal processing (DSP) blocks
Increased bandwidth capacity	3.125 gigabits per second (Gbps) and 6.144 Gbps transceiversHard memory controllers
Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor	 Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC) Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Lowest system cost	 Requires only two core voltages to operate Available in low-cost wirebond packaging Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration

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Feature	Description
	 HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller Arm CoreSight[™] JTAG debug access port, trace port, and on-chip trace storage
Configuration	 Tamper protection—comprehensive design protection to protect your valuable IP investments Enhanced advanced encryption standard (AES) design security features CvP Dynamic reconfiguration of the FPGA Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options Internal scrubbing ⁽²⁾ Partial reconfiguration ⁽³⁾

Cyclone V Device Variants and Packages

Table 3. Device Variants for the Cyclone V Device Family

Variant	Description
Cyclone V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone V SE	SoC with integrated Arm-based HPS
Cyclone V SX	SoC with integrated Arm-based HPS and 3.125 Gbps transceivers
Cyclone V ST	SoC with integrated Arm-based HPS and 6.144 Gbps transceivers

Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

⁽²⁾ The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

⁽³⁾ The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel[®] sales representatives.



Available Options

Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 6. Maximum Resource Counts for Cyclone V GX Devices

Resource				Member Code		
		C3	C4	C5	C7	С9
Logic Elements	(LE) (K)	36	50	77	150	301
ALM		13,460	18,860	29,080	56,480	113,560
Register	Register		75,440	116,320	225,920	454,240
Memory (Kb)	M10K	1,350	2,500	4,460	6,860	12,200
	MLAB	182	424	424	836	1,717
Variable-precisio	on DSP Block	57	70	150	156	342
18 x 18 Multiplie	er	114	140	300	312	684
PLL		4	6	6	7	8
3 Gbps Transceiver		3	6	6	9	12
GPIO ⁽⁴⁾		208	336	336	480	560
						continued

⁽⁴⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus[®] Prime software, the number of user I/Os includes transceiver I/Os.



Resource		Member Code						
		С3	C4	C5	C7	С9		
LVDS	Transmitter	52	84	84	120	140		
	Receiver	52	84	84	120	140		
PCIe Hard IP Block		1	2	2	2	2		
Hard Memory Controller		1	2	2	2	2		

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices Provides the number of LVDS channels in each device package.

Package Plan

Table 7. Package Plan for Cyclone V GX Devices

Member Code	M301 (11 mm)		M301 M383 (11 mm) (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	-	—	-	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	_	_	_	_	—	_	—	—	240	5

Member Code	F4 (23)	84 mm)	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	208	3	_	_	_	-	-	-
C4	240	6	336	6	_	-	_	_
C5	240	6	336	6	_	-	_	-
C7	240	6	336	9	480	9	-	-
C9	224	6	336	9	480	12	560	12

Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.



Available Options

Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices



Maximum Resources

Table 8. Maximum Resource Counts for Cyclone V GT Devices

R	esource		Member Code	
		D5	D7	D9
Logic Elements (LE)	(К)	77	150	301
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DS	SP Block	150	156	342
18 x 18 Multiplier		300	312	684
PLL		6	7	8
6 Gbps Transceiver	6 Gbps Transceiver		9	12
GPIO ⁽⁵⁾		336	480	560
LVDS	Transmitter	84	120	140
		•	·	continued

⁽⁵⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



Resource		Member Code				
		D5	D7	D9		
	Receiver	84	120	140		
PCIe Hard IP Block		2	2	2		
Hard Memory Controller	-	2	2	2		

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

Package Plan

Table 9.Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤ 5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	M301 (11 mm)		M301 M383 (11 mm) (13 mm)		M4 (15 r	M484 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	
D5	129	4	175	6	_	_	224	6	
D7	_	_	_	_	240	3	240	6	
D9	_	_	—	_		_	240	5	

Member Code	F484 (23 mm)		F6 (27 i	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	
D5	240	6	336	6	_	_	_	-	
D7	240	6	336	9 (6)	480	9 (6)	—	—	
D9	224	6	336	9 (6)	480	12 (7)	560	12 (7)	

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers

Provides more information about 6 Gbps transceiver channel count.

⁽⁶⁾ If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

⁽⁷⁾ If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.



Cyclone V SE

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 4. Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.





Maximum Resources

Table 10. Maximum Resource Counts for Cyclone V SE Devices

Resource			Member Code					
		A2	A4	A5	A6			
Logic Elements (LE) (K)	25	40	85	110			
ALM		9,430	15,880	32,070	41,910			
Register		37,736	60,376	128,300	166,036			
Memory (Kb)	M10K	1,400	2,700	3,970	5,570			
	MLAB	138	231	480	621			
Variable-precision DSP Block		36	84	87	112			
18 x 18 Multiplier		72	168	174	224			
FPGA PLL		5	5	6	6			
HPS PLL		3	3	3	3			
FPGA GPIO		145	145	288	288			
HPS I/O		181	181	181	181			
LVDS	Transmitter	32	32	72	72			
	Receiver	37	37	72	72			
FPGA Hard Memory Controller		1	1	1	1			
HPS Hard Memory Controller		1	1	1	1			
Arm Cortex-A9 N	1PCore Processor	Single- or dual- core	Single- or dual- core	Single- or dual-core	Single- or dual-core			

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices Provides the number of LVDS channels in each device package.

Package Plan

Table 11.Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O
A2	66	151	145	181	—	—
A4	66	151	145	181	-	-
A5	66	151	145	181	288	181
A6	66	151	145	181	288	181





Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 12. Maximum Resource Counts for Cyclone V SX Devices

Resource		Member Code				
		C2	C4	C5	C6	
Logic Elements (LE) (K)		25	40	85	110	
ALM		9,430	15,880	32,070	41,910	
Register		37,736	60,376	128,300	166,036	
Memory (Kb)	M10K	1,400	2,700	3,970	5,570	
	MLAB	138	231	480	621	
Variable-precision	Variable-precision DSP Block		84	87	112	
18 x 18 Multiplier		72	168	174	224	
FPGA PLL		5	5	6	6	
		•	•		continued	

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Resource		Member Code					
		C2	C4	C5	C6		
HPS PLL		3	3	3	3		
3 Gbps Transceiver	-	6	6	9	9		
FPGA GPIO ⁽⁸⁾		145	145	288	288		
HPS I/O		181	181	181	181		
LVDS	Transmitter	32	32	72	72		
	Receiver	37	37	72	72		
PCIe Hard IP Block		2	2	2 (9)	2 (9)		
FPGA Hard Memory Controller		1	1	1	1		
HPS Hard Memory Controller		1	1	1	1		
Arm Cortex-A9 MP	Core Processor	Dual-core	Dual-core	Dual-core	Dual-core		

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices Provides the number of LVDS channels in each device package.

Package Plan

Table 13.Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	_	_	_
C4	145	181	6	-	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ 1 PCIe Hard IP Block in U672 package.

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Reso	urce	Member Code		
		D5	D6	
	Receiver	72	72	
PCIe Hard IP Block		2	2	
FPGA Hard Memory Controller		1	1	
HPS Hard Memory Controller		1	1	
Arm Cortex-A9 MPCore Proces	sor	Dual-core	Dual-core	

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPSspecific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the Cyclone V Device Handbook Volume 2: Transceivers.

Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 (11)
D6	288	181	9 (11)

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers

Provides more information about 6 Gbps transceiver channel count.

⁽¹¹⁾ If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.



I/O Vertical Migration for Cyclone V Devices

Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.



You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.



Variant	Member Code	Variable- precision	Indepen Multi	dent Input and plications Ope	18 x 18 Multiplier	18 x 18 Multiplier	
		DSP Block	9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier	Adder Mode	Summed with 36 bit Input
	C6	112	336	224	112	112	112
Cyclone V ST	D5	87	261	174	87	87	87
	D6	112	336	224	112	112	112

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks—blocks of dedicated memory resources. The M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Cyclone V Devices

Table 18. Embedded Memory Capacity and Distribution in Cyclone V Devices

	Mombor	M10K		MLAB		
Variant	Code	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	(Kb)
Cyclone V E	A2	176	1,760	314	196	1,956
	A4	308	3,080	485	303	3,383
	A5	446	4,460	679	424	4,884
	A7	686	6,860	1338	836	7,696
	A9	1,220	12,200	2748	1,717	13,917
Cyclone V GX	C3	135	1,350	291	182	1,532
	C4	250	2,500	678	424	2,924
	C5	446	4,460	678	424	4,884
	C7	686	6,860	1338	836	7,696
	C9	1,220	12,200	2748	1,717	13,917
						continued



	Mombor	M1	.0К	ML	AB	
Variant	Code	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	(Kb)
Cyclone V GT	D5	446	4,460	679	424	4,884
	D7	686	6,860	1338	836	7,696
	D9	1,220	12,200	2748	1,717	13,917
Cyclone V SE	A2	140	1,400	221	138	1,538
	A4	270	2,700	370	231	2,460
	A5	397	3,970	768	480	4,450
	A6	553	5,530	994	621	6,151
Cyclone V SX	C2	140	1,400	221	138	1,538
	C4	270	2,700	370	231	2,460
	C5	397	3,970	768	480	4,450
	C6	553	5,530	994	621	6,151
Cyclone V ST	D5	397	3,970	768	480	4,450
	D6	553	5,530	994	621	6,151

Embedded Memory Configurations

Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1К	x10 or x8
	2К	x5 or x4
	4К	x2
	8К	×1

Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

Note: To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.



PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 9. PCIe Multifunction for Cyclone V Devices



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.



Figure 10. Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 22. PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	 Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization No decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels



PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO[®] (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23.	Transceiver	PCS	Features	for	Cvclone	V	Devices
						_	

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature			
3-Gbps and 6-Gbps Basic	0.614 to 6.144	 Phase compensation FIFO Byte serializer 8B/10B encoder Transmitter bit-slip 	 Word aligner Deskew FIFO Rate-match FIFO 8B/10B decoder Byte deserializer Byte ordering Receiver phase compensation FIFO 			
PCIe Gen1 (x1, x2, x4)	2.5 and 5.0	 Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic 	 Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic 			
PCIe Gen2 (x1, x2, x4) ⁽¹²⁾		logic	logic			
GbE	1.25	 Custom PHY IP core with preset feature GbE transmitter synchronization state machine 	 Custom PHY IP core with preset feature GbE receiver synchronization state machine 			
XAUI (13)	3.125	Dedicated XAUI PHY IP core	Dedicated XAUI PHY IP core			
HiGig	3.75	XAUI synchronization state machine for bonding four channels	 XAUI synchronization state machine for realigning four channels 			
SRIO 1.3 and 2.1	1.25 to 3.125	 Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 channel bonding 	 Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 deskew state machine 			
SDI, SD/HD, and 3G-SDI	0.27 ⁽¹⁴⁾ , 1.485, and 2.97	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature			
JESD204A	0.3125 ⁽¹⁵⁾ to 3.125					
continued						

⁽¹²⁾ PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

⁽¹⁵⁾ The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹³⁾ XAUI is supported through the soft PCS.

 $^{^{(14)}}$ The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.





Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.



HPS-FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA[®]) Advanced eXtensible Interface (AXI[™]) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon[®] Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 400 MHz (800 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

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Date	Version	Changes
		 Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: Cyclone V GX C3: Updated from 181 to 182 Cyclone V GX C4: Updated from 295 to 424 Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: Cyclone V GX C3: Updated from 1,531 to 1,532 Cyclone V GX C4: Updated from 2,795 to 2,924 Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: Cyclone V GX C4: Updated from 2,795 to 2,924 Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: Cyclone V GX C4: Updated from 472 to 678 Cyclone V GX C5: Updated from 679 to 678
March 2015	2015.03.31	 Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table. Added optional suffix "SC: Internal scrubbing support" to the following diagrams: Sample Ordering Code and Available Options for Cyclone V E Devices Sample Ordering Code and Available Options for Cyclone V GX Devices Sample Ordering Code and Available Options for Cyclone V SE Devices Sample Ordering Code and Available Options for Cyclone V SE Devices Sample Ordering Code and Available Options for Cyclone V SX Devices
January 2015	2015.01.23	 Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and -7 speed grade. Operating Temperature: Removed C and A temperature grades FPGA Fabric Speed Grade: Removed -6 and -8 speed grades Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps: Device Variants for the Cyclone V Device Family table Sample Ordering Code and Available Options for Cyclone V ST Devices figure Maximum Resource Counts for Cyclone V ST Devices Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices. Logic elements (LE) (K): Updated from 35.7 to 35.5 Variable-precision DSP block: Updated from 51 to 57 18 x 18 multiplier: Updated from 102 to 114 Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. Variableprecision DSP Block: Updated from 51 to 57 9 x 9 Multiplier: Updated from 102 to 114 Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. Variableprecision DSP Block: Updated from 51 to 57 18 x 18 Multiplier: Updated from 102 to 114 27 x 27 Multiplier: Updated from 102 to 114 27 x 27 Multiplier: Updated from 51 to 57 18 x 18 Multiplier Adder Mode: Updated from 51 to 57 18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57 Widated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices. M10K RAM bit (Kb): Updated from 1,190 to 1,350 MLAB block: Updated from 255 to 291 MLAB RAM bit (Kb): Updated from 159 to 181 Total RAM bit (Kb): Updated from 1,349 to 1,531
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.