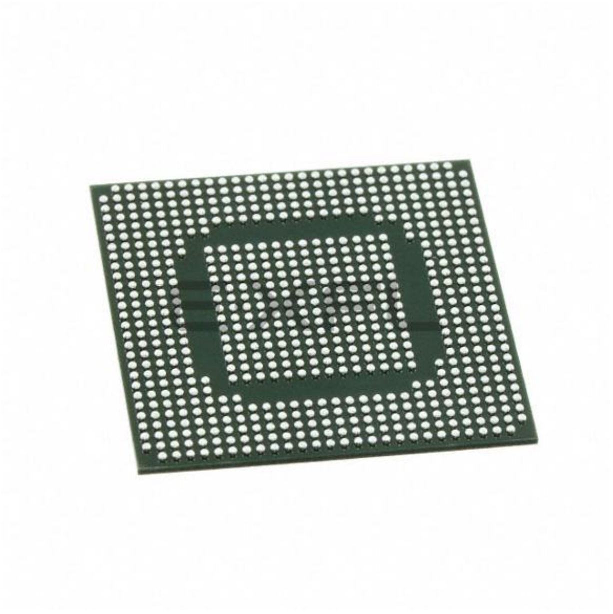

**Welcome to E-XFL.COM**

## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| **Details** | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 64KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 600MHz |
| Primary Attributes | FPGA - 25K Logic Elements |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-FBGA |
| Supplier Device Package | 672-UBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5csema2u23c8n |

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# Summary of Cyclone V Features

## Table 2. Summary of Features for Cyclone V Devices

| Feature | Description | |
|---|---|---|
| Technology | • TSMC's 28-nm low-power (28LP) process technology<br>• 1.1 V core voltage | |
| Packaging | • Wirebond low-halogen packages<br>• Multiple device densities with compatible package footprints for seamless migration between different device densities<br>• RoHS-compliant and leaded(1)options | |
| High-performance FPGA fabric | Enhanced 8-input ALM with four registers | |
| Internal memory blocks | • M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory | |
| Embedded Hard IP blocks | Variable-precision DSP | • Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block<br>• 64-bit accumulator and cascade<br>• Embedded internal coefficient memory<br>• Preadder/subtractor for improved efficiency |
| | Memory controller | DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support |
| | Embedded transceiver I/O | PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port |
| Clock networks | • Up to 550 MHz global clock network<br>• Global, quadrant, and peripheral clock networks<br>• Clock networks that are not used can be powered down to reduce dynamic power | |
| Phase-locked loops (PLLs) | • Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)<br>• Integer mode and fractional mode | |
| FPGA General-purpose I/Os (GPIOs) | • 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter<br>• 400 MHz/800 Mbps external memory interface<br>• On-chip termination (OCT)<br>• 3.3 V support with up to 16 mA drive strength | |
| Low-power high-speed serial interface | • 614 Mbps to 6.144 Gbps integrated transceiver speed<br>• Transmit pre-emphasis and receiver equalization<br>• Dynamic partial reconfiguration of individual channels | |
| HPS (Cyclone V SE, SX, and ST devices only) | • Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing<br>• Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I$^2$C interface, and up to 85 HPS GPIO interfaces<br>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers<br>• On-chip RAM and boot ROM | |

*continued...*

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(1) Contact Intel for availability.

| Feature | Description |
|---|---|
| | • HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa<br>• FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller<br>• Arm CoreSight™ JTAG debug access port, trace port, and on-chip trace storage |
| Configuration | • Tamper protection—comprehensive design protection to protect your valuable IP investments<br>• Enhanced advanced encryption standard (AES) design security features<br>• CvP<br>• Dynamic reconfiguration of the FPGA<br>• Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options<br>• Internal scrubbing (2)<br>• Partial reconfiguration (3) |

## Cyclone V Device Variants and Packages

### Table 3. Device Variants for the Cyclone V Device Family

| Variant | Description |
|---|---|
| Cyclone V E | Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications |
| Cyclone V GX | Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications |
| Cyclone V GT | The FPGA industry’s lowest cost and lowest power requirement for 6.144 Gbps transceiver applications |
| Cyclone V SE | SoC with integrated Arm-based HPS |
| Cyclone V SX | SoC with integrated Arm-based HPS and 3.125 Gbps transceivers |
| Cyclone V ST | SoC with integrated Arm-based HPS and 6.144 Gbps transceivers |

## Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

### Related Information

Product Selector Guide
Provides the latest information about Intel products.

---

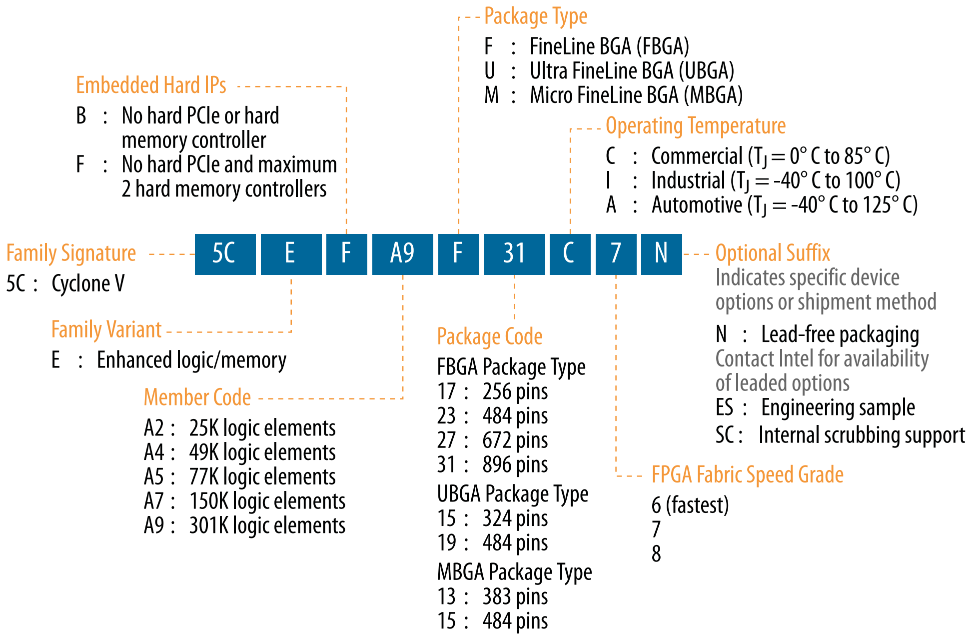
(2) The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

(3) The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel® sales representatives.

## Available Options

### Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Maximum Resources

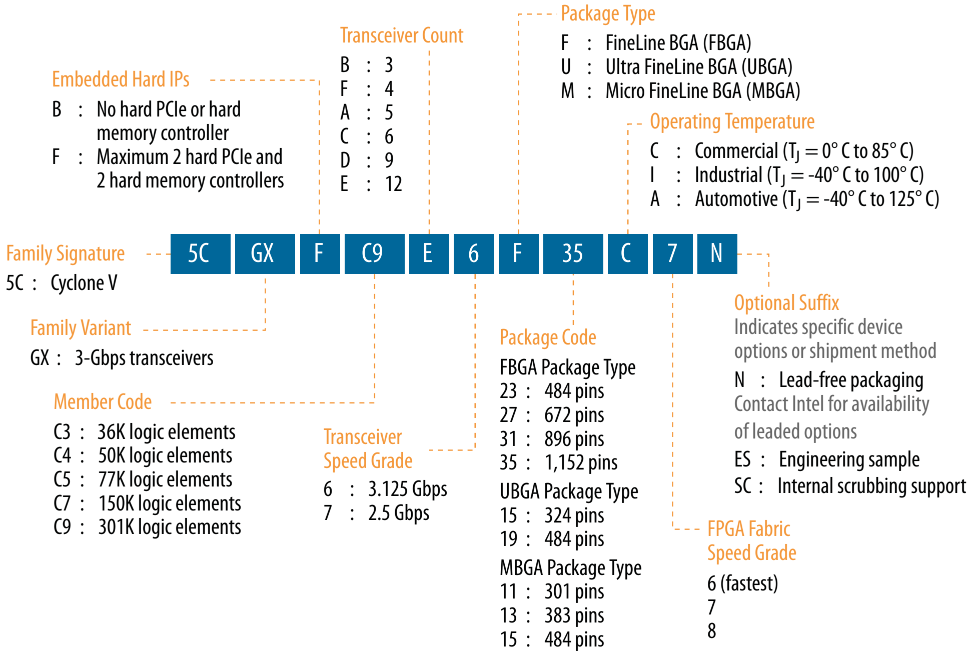
### Table 4. Maximum Resource Counts for Cyclone V E Devices

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | A2 | A4 | A5 | A7 | A9 |
| Logic Elements (LE) (K) | | 25 | 49 | 77 | 150 | 301 |
| ALM | | 9,430 | 18,480 | 29,080 | 56,480 | 113,560 |
| Register | | 37,736 | 73,920 | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 1,760 | 3,080 | 4,460 | 6,860 | 12,200 |
| | MLAB | 196 | 303 | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 25 | 66 | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 50 | 132 | 300 | 312 | 684 |
| PLL | | 4 | 4 | 6 | 7 | 8 |
| GPIO | | 224 | 224 | 240 | 480 | 480 |
| LVDS | Transmitter | 56 | 56 | 60 | 120 | 120 |
| | Receiver | 56 | 56 | 60 | 120 | 120 |
| Hard Memory Controller | | 1 | 1 | 2 | 2 | 2 |

## Available Options

### Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Maximum Resources

### Table 6. Maximum Resource Counts for Cyclone V GX Devices

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | C3 | C4 | C5 | C7 | C9 |
| Logic Elements (LE) (K) | | 36 | 50 | 77 | 150 | 301 |
| ALM | | 13,460 | 18,860 | 29,080 | 56,480 | 113,560 |
| Register | | 53,840 | 75,440 | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 1,350 | 2,500 | 4,460 | 6,860 | 12,200 |
| | MLAB | 182 | 424 | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 57 | 70 | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 114 | 140 | 300 | 312 | 684 |
| PLL | | 4 | 6 | 6 | 7 | 8 |
| 3 Gbps Transceiver | | 3 | 6 | 6 | 9 | 12 |
| GPIO(4) | | 208 | 336 | 336 | 480 | 560 |

*continued...*

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(4) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | C3 | C4 | C5 | C7 | C9 |
| LVDS | Transmitter | 52 | 84 | 84 | 120 | 140 |
| | Receiver | 52 | 84 | 84 | 120 | 140 |
| PCIe Hard IP Block | | 1 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 1 | 2 | 2 | 2 | 2 |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 7. Package Plan for Cyclone V GX Devices

| Member Code | M301 (11 mm) | | M383 (13 mm) | | M484 (15 mm) | | U324 (15 mm) | | U484 (19 mm) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| C3 | — | — | — | — | — | — | 144 | 3 | 208 | 3 |
| C4 | 129 | 4 | 175 | 6 | — | — | — | — | 224 | 6 |
| C5 | 129 | 4 | 175 | 6 | — | — | — | — | 224 | 6 |
| C7 | — | — | — | — | 240 | 3 | — | — | 240 | 6 |
| C9 | — | — | — | — | — | — | — | — | 240 | 5 |

| Member Code | F484 (23 mm) | | F672 (27 mm) | | F896 (31 mm) | | F1152 (35 mm) | |
|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| C3 | 208 | 3 | — | — | — | — | — | — |
| C4 | 240 | 6 | 336 | 6 | — | — | — | — |
| C5 | 240 | 6 | 336 | 6 | — | — | — | — |
| C7 | 240 | 6 | 336 | 9 | 480 | 9 | — | — |
| C9 | 224 | 6 | 336 | 9 | 480 | 12 | 560 | 12 |

# Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

Product Selector Guide
Provides the latest information about Intel products.

## Cyclone V SE

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

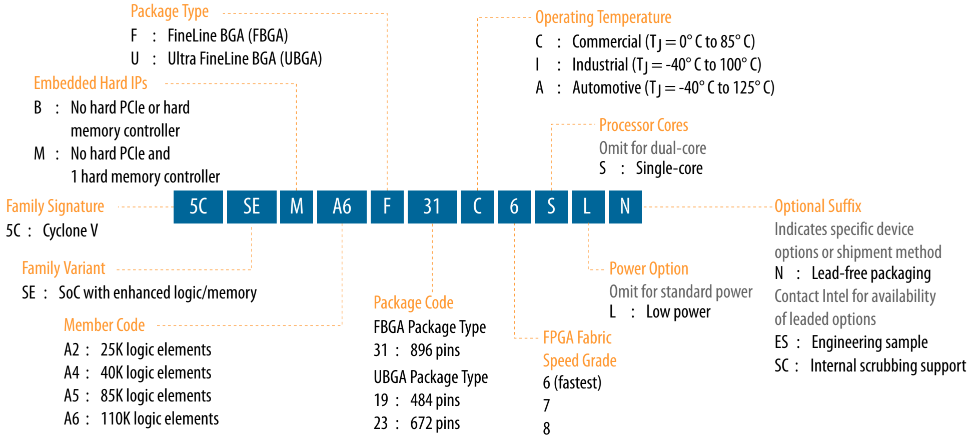
Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 4. Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



## Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

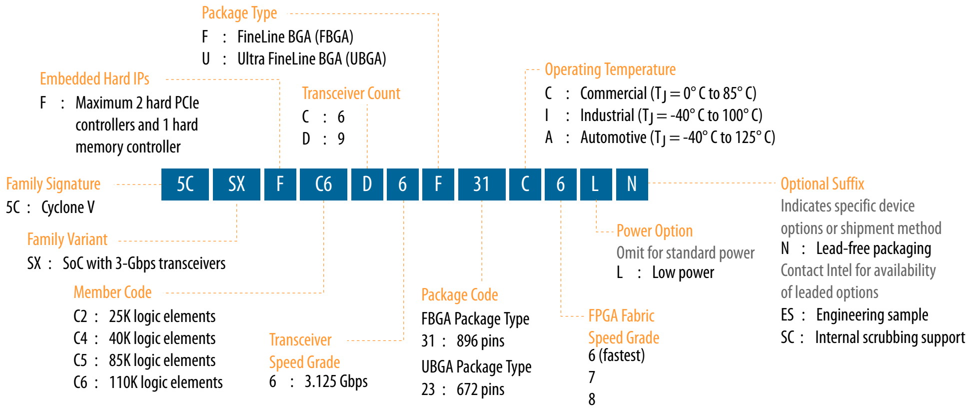
Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



## Maximum Resources

### Table 12. Maximum Resource Counts for Cyclone V SX Devices

| Resource | | Member Code | | | |
|---|---|---|---|---|---|
| | | C2 | C4 | C5 | C6 |
| Logic Elements (LE) (K) | | 25 | 40 | 85 | 110 |
| ALM | | 9,430 | 15,880 | 32,070 | 41,910 |
| Register | | 37,736 | 60,376 | 128,300 | 166,036 |
| Memory (Kb) | M10K | 1,400 | 2,700 | 3,970 | 5,570 |
| | MLAB | 138 | 231 | 480 | 621 |
| Variable-precision DSP Block | | 36 | 84 | 87 | 112 |
| 18 x 18 Multiplier | | 72 | 168 | 174 | 224 |
| FPGA PLL | | 5 | 5 | 6 | 6 |

***continued...***

| Resource | | Member Code | | | |
|---|---|---|---|---|---|
| | | C2 | C4 | C5 | C6 |
| HPS PLL | | 3 | 3 | 3 | 3 |
| 3 Gbps Transceiver | | 6 | 6 | 9 | 9 |
| FPGA GPIO (8) | | 145 | 145 | 288 | 288 |
| HPS I/O | | 181 | 181 | 181 | 181 |
| LVDS | Transmitter | 32 | 32 | 72 | 72 |
| | Receiver | 37 | 37 | 72 | 72 |
| PCIe Hard IP Block | | 2 | 2 | 2 (9) | 2 (9) |
| FPGA Hard Memory Controller | | 1 | 1 | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Dual-core | Dual-core | Dual-core | Dual-core |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | U672 (23 mm) | | | F896 (31 mm) | | |
|---|---|---|---|---|---|---|
| | FPGA GPIO | HPS I/O | XCVR | FPGA GPIO | HPS I/O | XCVR |
| C2 | 145 | 181 | 6 | — | — | — |
| C4 | 145 | 181 | 6 | — | — | — |
| C5 | 145 | 181 | 6 | 288 | 181 | 9 |
| C6 | 145 | 181 | 6 | 288 | 181 | 9 |

## Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

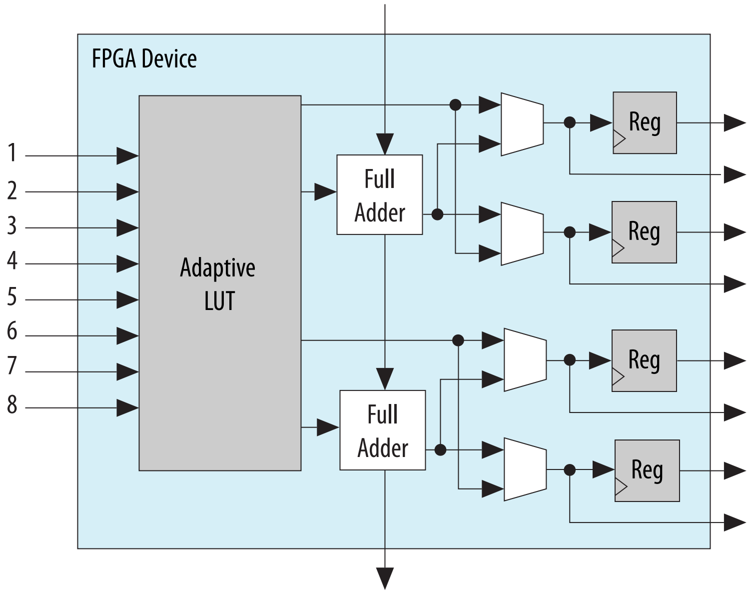
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

---

(8) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(9) 1 PCIe Hard IP Block in U672 package.

**Figure 8. ALM for Cyclone V Devices**



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

### Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21
Lists the embedded memory capacity for each device.

## Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

## Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

| Usage Example | Multiplier Size (Bit) | DSP Block Resource |
|---|---|---|
| Low precision fixed point for video applications | Three 9 x 9 | 1 |
| Medium precision fixed point in FIR filters | Two 18 x 18 | 1 |
| FIR filters and general DSP usage | Two 18 x 18 with accumulate | 1 |
| High precision fixed- or floating-point implementations | One 27 x 27 with accumulate | 1 |

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

## Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

| Variant | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---|---|---|---|---|---|---|---|
| | | | 9 x 9 Multiplier | 18 x 18 Multiplier | 27 x 27 Multiplier | | |
| Cyclone V E | A2 | 25 | 75 | 50 | 25 | 25 | 25 |
| | A4 | 66 | 198 | 132 | 66 | 66 | 66 |
| | A5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | A7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | A9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GX | C3 | 57 | 171 | 114 | 57 | 57 | 57 |
| | C4 | 70 | 210 | 140 | 70 | 70 | 70 |
| | C5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | C7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | C9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GT | D5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | D7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | D9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V SE | A2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | A4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | A5 | 87 | 261 | 174 | 87 | 87 | 87 |
| | A6 | 112 | 336 | 224 | 112 | 112 | 112 |
| Cyclone V SX | C2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | C4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | C5 | 87 | 261 | 174 | 87 | 87 | 87 |

***continued...***

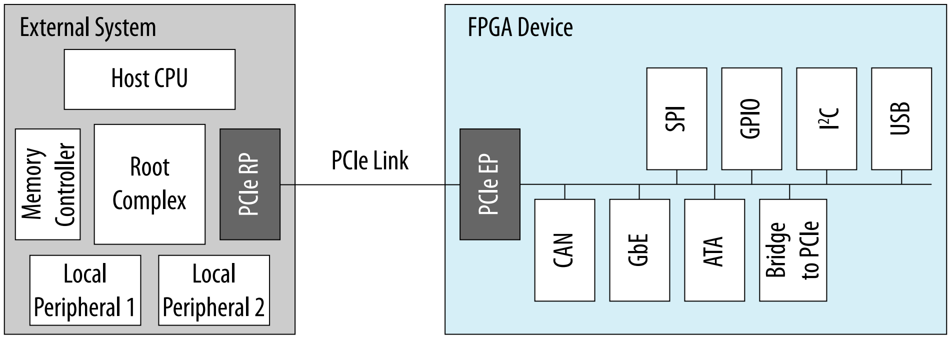
## PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

**Figure 9. PCIe Multifunction for Cyclone V Devices**



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

## External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

## Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.

## PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

### Table 23. Transceiver PCS Features for Cyclone V Devices

| PCS Support | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|---|---|---|---|
| 3-Gbps and 6-Gbps Basic | 0.614 to 6.144 | • Phase compensation FIFO<br>• Byte serializer<br>• 8B/10B encoder<br>• Transmitter bit-slip | • Word aligner<br>• Deskew FIFO<br>• Rate-match FIFO<br>• 8B/10B decoder<br>• Byte deserializer<br>• Byte ordering<br>• Receiver phase compensation FIFO |
| PCIe Gen1 (x1, x2, x4) | 2.5 and 5.0 | • Dedicated PCIe PHY IP core<br>• PIPE 2.0 interface to the core logic | • Dedicated PCIe PHY IP core<br>• PIPE 2.0 interface to the core logic |
| PCIe Gen2 ( x1, x2, x4)(12) | | | |
| GbE | 1.25 | • Custom PHY IP core with preset feature<br>• GbE transmitter synchronization state machine | • Custom PHY IP core with preset feature<br>• GbE receiver synchronization state machine |
| XAUI (13) | 3.125 | • Dedicated XAUI PHY IP core<br>• XAUI synchronization state machine for bonding four channels | • Dedicated XAUI PHY IP core<br>• XAUI synchronization state machine for realigning four channels |
| HiGig | 3.75 | | |
| SRIO 1.3 and 2.1 | 1.25 to 3.125 | • Custom PHY IP core with preset feature<br>• SRIO version 2.1-compliant x2 and x4 channel bonding | • Custom PHY IP core with preset feature<br>• SRIO version 2.1-compliant x2 and x4 deskew state machine |
| SDI, SD/HD, and 3G-SDI | 0.27(14), 1.485, and 2.97 | Custom PHY IP core with preset feature | Custom PHY IP core with preset feature |
| JESD204A | 0.3125(15) to 3.125 | | |

*continued...*

---

(12) PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

(13) XAUI is supported through the soft PCS.

(14) The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

(15) The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

| PCS Support | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|---|---|---|---|
| Serial ATA Gen1 and Gen2 | 1.5 and 3.0 | • Custom PHY IP core with preset feature<br>• Electrical idle | • Custom PHY IP core with preset feature<br>• Signal detect<br>• Wider spread of asynchronous SSC |
| CPRI 4.1(16) | 0.6144 to 6.144 | • Dedicated deterministic latency PHY IP core<br>• Transmitter (TX) manual bit-slip mode | • Dedicated deterministic latency PHY IP core<br>• Receiver (RX) deterministic latency state machine |
| OBSAI RP3 | 0.768 to 3.072 | | |
| V-by-One HS | Up to 3.75 | Custom PHY IP core | • Custom PHY IP core<br>• Wider spread of asynchronous SSC |
| DisplayPort 1.2(17) | 1.62 and 2.7 | | |

## SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

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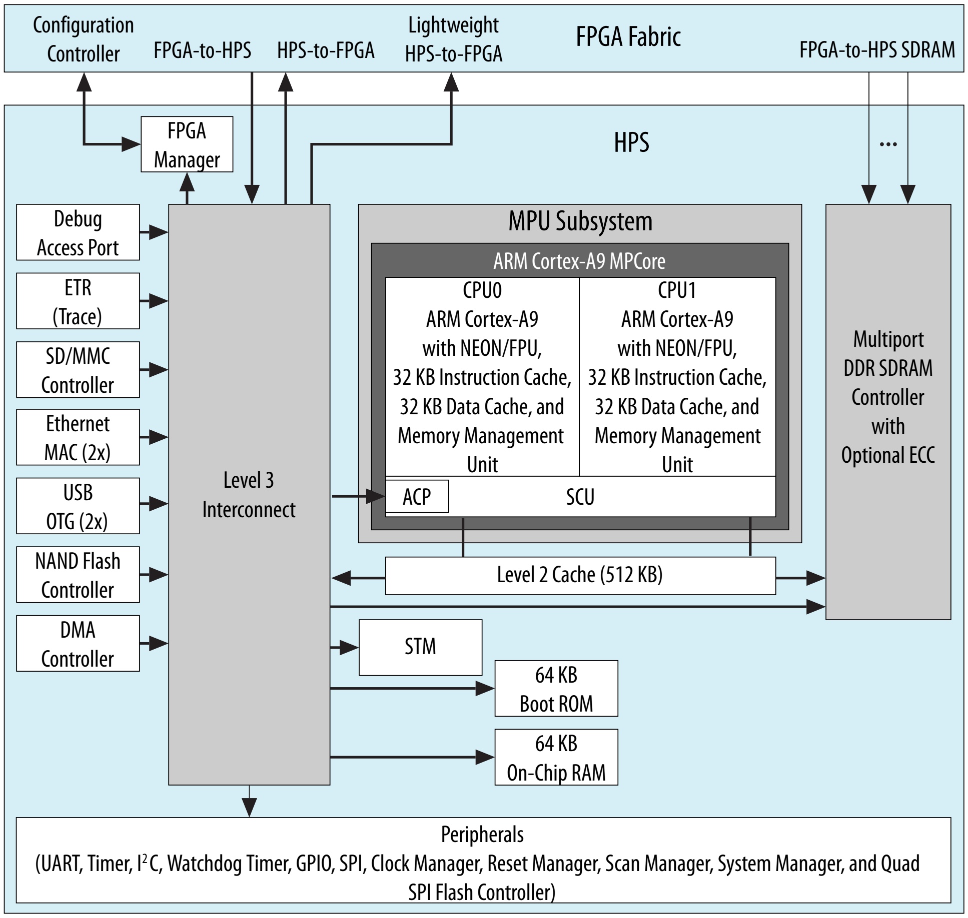
(16) High-voltage output mode (1000-BASE-CX) is not supported.

(17) Pending characterization.

**Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor**



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.

*Note:* Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

**Related Information**

Cyclone V Device Family Pin Connection Guidelines
Provides detailed information about power supply pin connection guidelines and power regulator sharing.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

**Related Information**

International Altera Sales Support Offices

## Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

## Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

## Partial Reconfiguration

*Note:* The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

| Date | Version | Changes |
|---|---|---|
| | | - Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<br>— Cyclone V GX C3: Updated from 181 to 182<br>— Cyclone V GX C4: Updated from 295 to 424<br>- Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<br>— Cyclone V GX C3: Updated from 1,531 to 1,532<br>— Cyclone V GX C4: Updated from 2,795 to 2,924<br>- Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<br>— Cyclone V GX C4: Updated from 472 to 678<br>— Cyclone V GX C5: Updated from 679 to 678 |
| March 2015 | 2015.03.31 | - Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table.<br>- Added optional suffix "SC: Internal scrubbing support" to the following diagrams:<br>— Sample Ordering Code and Available Options for Cyclone V E Devices<br>— Sample Ordering Code and Available Options for Cyclone V GX Devices<br>— Sample Ordering Code and Available Options for Cyclone V SE Devices<br>— Sample Ordering Code and Available Options for Cyclone V SX Devices |
| January 2015 | 2015.01.23 | - Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and –7 speed grade.<br>— Operating Temperature: Removed C and A temperature grades<br>— FPGA Fabric Speed Grade: Removed –6 and –8 speed grades<br>- Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps:<br>— Device Variants for the Cyclone V Device Family table<br>— Sample Ordering Code and Available Options for Cyclone V ST Devices figure<br>— Maximum Resource Counts for Cyclone V ST Devices<br>- Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices.<br>— Logic elements (LE) (K): Updated from 35.7 to 35.5<br>— Variable-precision DSP block: Updated from 51 to 57<br>— 18 x 18 multiplier: Updated from 102 to 114<br>- Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices.<br>— Variableprecision DSP Block: Updated from 51 to 57<br>— 9 x 9 Multiplier: Updated from 153 to 171<br>— 18 x 18 Multiplier: Updated from 102 to 114<br>— 27 x 27 Multiplier: Updated from 51 to 57<br>— 18 x 18 Multiplier Adder Mode: Updated from 51 to 57<br>— 18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57<br>- Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices.<br>— M10K block: Updated from 119 to 135<br>— M10K RAM bit (Kb): Updated from 1,190 to 1,350<br>— MLAB block: Updated from 255 to 291<br>— MLAB RAM bit (Kb): Updated from 159 to 181<br>— Total RAM bit (Kb): Updated from 1,349 to 1,531 |
| October 2014 | 2014.10.06 | Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| July 2014 | 2014.07.07 | Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices. |
| December 2013 | 2013.12.26 | • Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz.<br>• Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables.<br>• Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE.<br>• Added link to Altera Product Selector for each device variant.<br>• Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers.<br>• Added leaded package options.<br>• Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table.<br>• Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60.<br>• Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120.<br>• Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84.<br>• Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168.<br>• Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252.<br>• Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32.<br>• Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37.<br>• Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5.<br>• Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V.<br>• Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance.<br>• Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V.<br>• Added decompression support for the CvP configuration mode. |
| May 2013 | 2013.05.06 | • Added link to the known document issues in the Knowledge Base.<br>• Moved all links to the Related Information section of respective topics for easy reference.<br>• Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2.<br>• Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'.<br>• Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'.<br>• Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'.<br>• Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3.<br>• Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'.<br>• Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values.<br>• Updated the package plan with M383 for the Cyclone V E device.<br>• Removed the M301 and M383 packages from the Cyclone V GX C4 device.<br>• Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device.<br>• Updated 5 Gbps to '6.144 Gbps' forCyclone V GT device. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| | | - Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6.<br>- Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices.<br>- Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices.<br>- Removed '36 x 36' from the Variable-Precision DSP Block.<br>- Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device.<br>- Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices.<br>- Updated Figure 7 which shows the I/O vertical migration table.<br>- Updated Table 17 for Cyclone V SX C4 device.<br>- Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices.<br>- Removed 'Counter reconfiguration' from the PLL Features.<br>- Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps.<br>- Removed 'Distributed Memory' symbol.<br>- Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'.<br>- Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps.<br>- Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'.<br>- Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'.<br>- Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'.<br>- Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature. |
| December 2012 | 2012.12.28 | - Updated the pin counts for the MBGA packages.<br>- Updated the GPIO and transceiver counts for the MBGA packages.<br>- Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices.<br>- Updated the vertical migration table for vertical migration of the U484 packages.<br>- Updated the MLAB supported programmable widths at 32 bits depth. |
| November 2012 | 2012.11.19 | - Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT.<br>- Added ordering code for five-transceiver devices for Cyclone V GT and ST.<br>- Updated the vertical migration table to add MBGA packages.<br>- Added performance information for HPS memory controller.<br>- Removed DDR3U support.<br>- Updated Cyclone V ST speed grade information.<br>- Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance.<br>- Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software.<br>- Updated template. |
| July 2012 | 2.1 | Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible) |
| June 2012 | 2.0 | - Restructured the document.<br>- Added the “Embedded Memory Capacity” and “Embedded Memory Configurations” sections.<br>- Added Table 1, Table 3, Table 16, Table 19, and Table 20.<br>- Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| | | • Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10.<br>• Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections.<br>• Text edits throughout the document. |
| February 2012 | 1.2 | • Updated Table 1–2, Table 1–3, and Table 1–6.<br>• Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15.<br>• Updated Figure 1–1 and Figure 1–6. |
| November 2011 | 1.1 | • Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6.<br>• Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8.<br>• Updated "System Peripherals" on page 1–18, "HPS–FPGA AXI Bridges" on page 1–19, "HPS SDRAM Controller Subsystem" on page 1–19, "FPGA Configuration and Processor Booting" on page 1–19, and "Hardware and Software Development" on page 1–20.<br>• Minor text edits. |
| October 2011 | 1.0 | Initial release. |