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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 25K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-FBGA
Supplier Device Package	672-UBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csxfc2c6u23c7n

Feature	Description
	• HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller • Arm CoreSight™ JTAG debug access port, trace port, and on-chip trace storage
Configuration	• Tamper protection—comprehensive design protection to protect your valuable IP investments • Enhanced advanced encryption standard (AES) design security features • CvP • Dynamic reconfiguration of the FPGA • Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options • Internal scrubbing [2] • Partial reconfiguration [3]

Cyclone V Device Variants and Packages

Table 3.   Device Variants for the Cyclone V Device Family

Variant	Description
Cyclone V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone V SE	SoC with integrated Arm-based HPS
Cyclone V SX	SoC with integrated Arm-based HPS and 3.125 Gbps transceivers
Cyclone V ST	SoC with integrated Arm-based HPS and 6.144 Gbps transceivers

Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

Related Information

Product Selector Guide
> Provides the latest information about Intel products.

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[2] The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

[3] The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel® sales representatives.
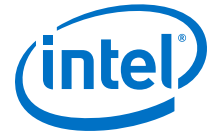
Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 5. **Package Plan for Cyclone V E Devices**

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	223	—	176	128	224	224	—	—
A4	223	—	176	128	224	224	—	—
A5	175	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.
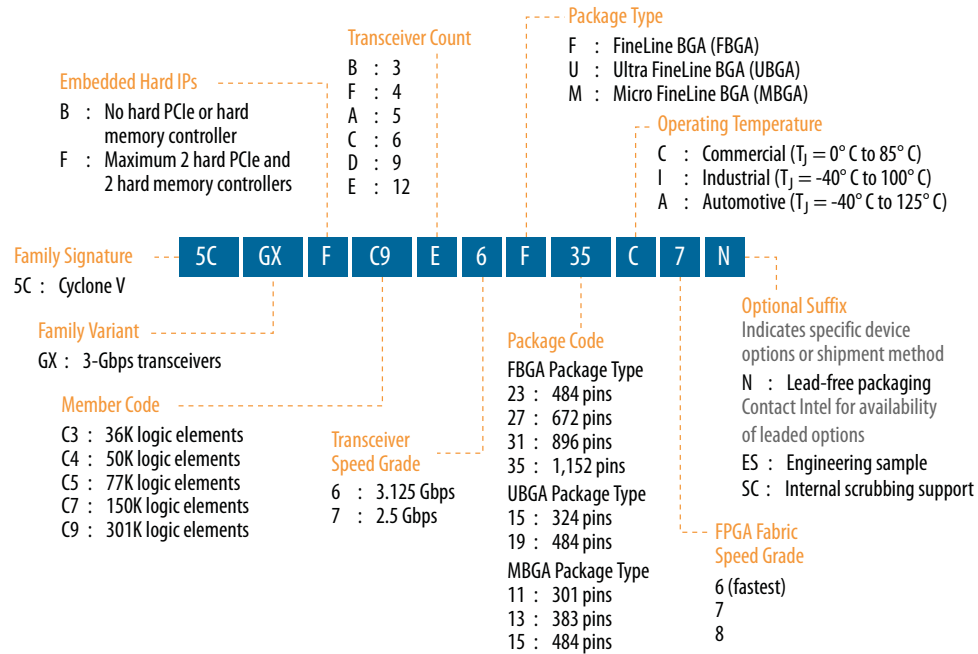
Maximum Resources

Table 6. Maximum Resource Counts for Cyclone V GX Devices

Resource		C3	C4	C5	C7	C9
Logic Elements (LE) (K)		36	50	77	150	301
ALM		13,460	18,860	29,080	56,480	113,560
Register		53,840	75,440	116,320	225,920	454,240
Memory (Kb)	M10K	1,350	2,500	4,460	6,860	12,200
	MLAB	182	424	424	836	1,717
Variable-precision DSP Block		57	70	150	156	342
18 x 18 Multiplier		114	140	300	312	684
PLL		4	6	6	7	8
3 Gbps Transceiver		3	6	6	9	12
GPIO[4]		208	336	336	480	560
						continued...

Note: The header row for the data columns is labelled "Member Code" spanning C3, C4, C5, C7, C9.

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[4] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code				
		C3	**C4**	**C5**	**C7**	**C9**
LVDS	Transmitter	52	84	84	120	140
	Receiver	52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 7.   Package Plan for Cyclone V GX Devices

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	—	—	—	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	—	—	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**
C3	208	3	—	—	—	—	—	—
C4	240	6	336	6	—	—	—	—
C5	240	6	336	6	—	—	—	—
C7	240	6	336	9	480	9	—	—
C9	224	6	336	9	480	12	560	12

Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.
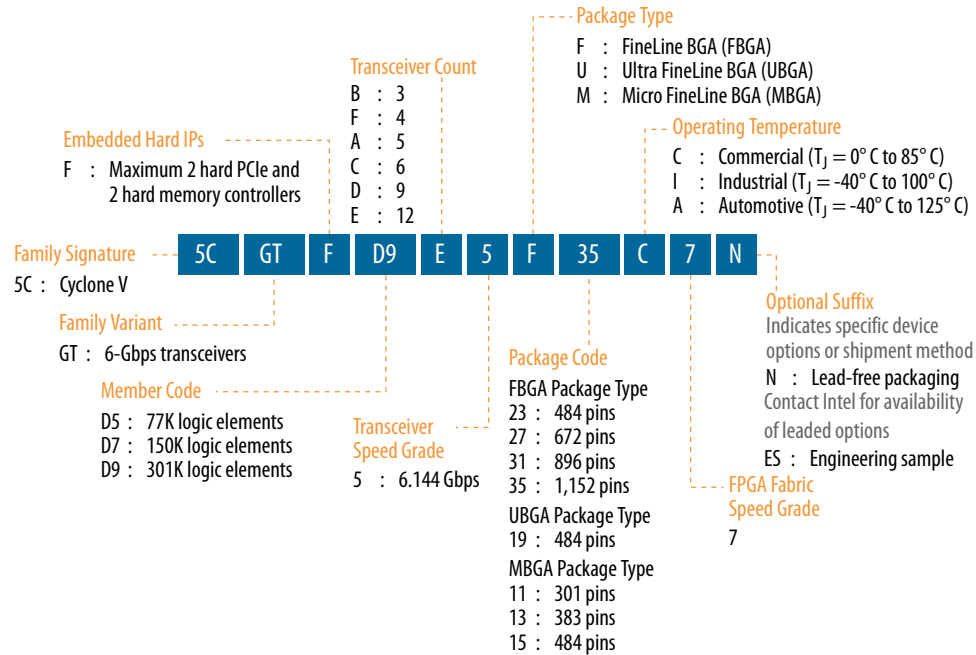
Related Information

Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 3. **Sample Ordering Code and Available Options for Cyclone V GT Devices**

Maximum Resources

Table 8. **Maximum Resource Counts for Cyclone V GT Devices**

Resource		Member Code		
		D5	**D7**	**D9**
Logic Elements (LE) (K)		77	150	301
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DSP Block		150	156	342
18 x 18 Multiplier		300	312	684
PLL		6	7	8
6 Gbps Transceiver		6	9	12
GPIO[5]		336	480	560
LVDS	Transmitter	84	120	140
				continued...

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[5] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code		
		D5	**D7**	**D9**
	Receiver	84	120	140
PCIe Hard IP Block		2	2	2
Hard Memory Controller		2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
    Provides the number of LVDS channels in each device package.

Package Plan

Table 9.   Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U484 (19 mm)	
	GPIO	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**
D5	129	4	175	6	—	—	224	6
D7	—	—	—	—	240	3	240	6
D9	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**	**GPIO**	**XCVR**
D5	240	6	336	6	—	—	—	—
D7	240	6	336	9 [6]	480	9 [6]	—	—
D9	224	6	336	9 [6]	480	12 [7]	560	12 [7]

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
    Provides more information about 6 Gbps transceiver channel count.

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[6] If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

[7] If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.
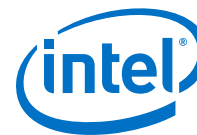
Maximum Resources

Table 10.   Maximum Resource Counts for Cyclone V SE Devices

Resource		Member Code			
		A2	**A4**	**A5**	**A6**
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 11.   Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	**HPS I/O**	**FPGA GPIO**	**HPS I/O**	**FPGA GPIO**	**HPS I/O**
A2	66	151	145	181	—	—
A4	66	151	145	181	—	—
A5	66	151	145	181	288	181
A6	66	151	145	181	288	181
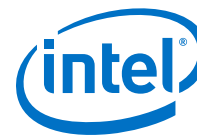
Resource		Member Code			
		C2	**C4**	**C5**	**C6**
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO [8]		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 [9]	2 [9]
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 13.   Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	**HPS I/O**	**XCVR**	**FPGA GPIO**	**HPS I/O**	**XCVR**
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

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[8] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.
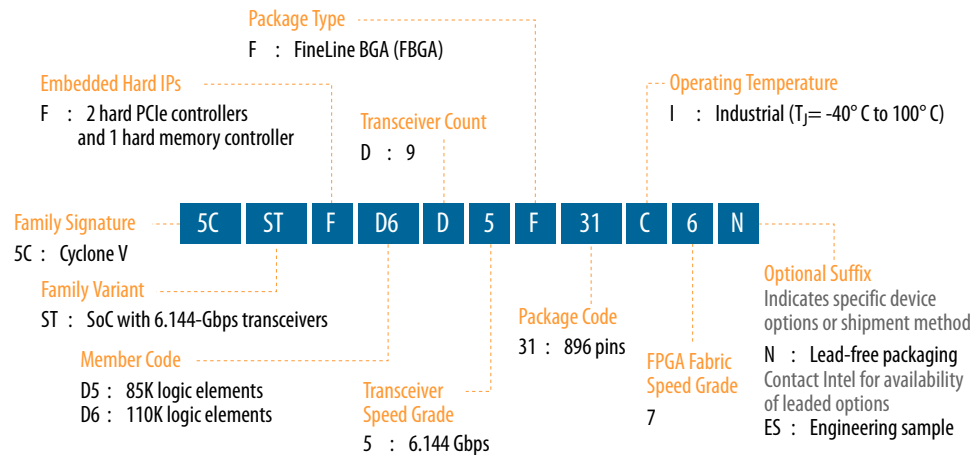
[9] 1 PCIe Hard IP Block in U672 package.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Available Options

**Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices**

Maximum Resources

Table 14. Maximum Resource Counts for Cyclone V ST Devices

Resource		Member Code	
		D5	**D6**
Logic Elements (LE) (K)		85	110
ALM		32,070	41,910
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,570
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL		6	6
HPS PLL		3	3
6.144 Gbps Transceiver		9	9
FPGA GPIO[10]		288	288
HPS I/O		181	181
LVDS	Transmitter	72	72
			continued...

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[10] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.
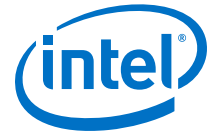
Resource		Member Code	
		D5	**D6**
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	**HPS I/O**	**XCVR**
D5	288	181	9 [11]
D6	288	181	9 [11]

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

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[11] If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Figure 8.   ALM for Cyclone V Devices
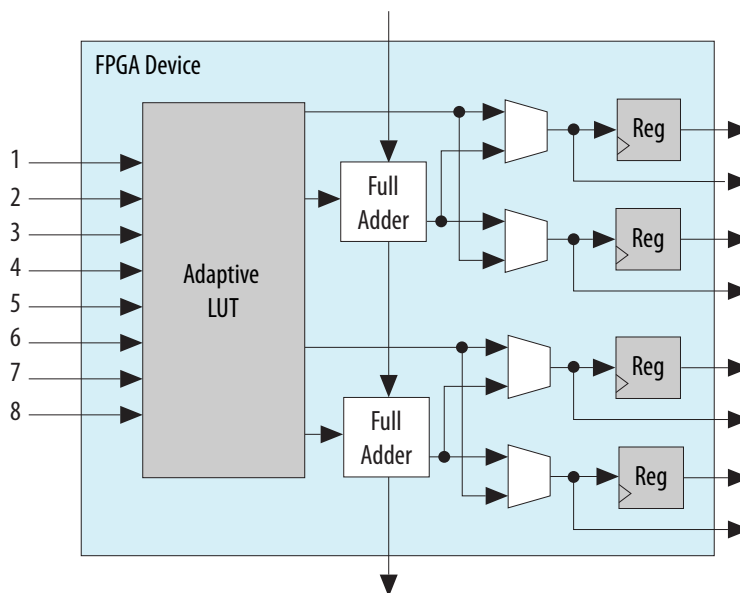
You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21
    Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

*   Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively

*   A 64-bit accumulator

*   A hard preadder that is available in both 18- and 27-bit modes

*   Cascaded output adders for efficient systolic finite impulse response (FIR) filters

*   Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode

*   Fully independent multiplier operation

*   A second accumulator feedback register to accommodate complex multiply-accumulate functions

*   Fully independent Efficient support for single-precision floating point arithmetic

*   The inferability of all modes by the Intel Quartus Prime design software
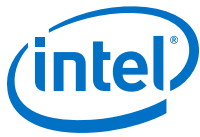
Table 16.   Variable-Precision DSP Block Configurations for Cyclone V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters and general DSP usage	Two 18 x 18 with accumulate	1
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 17.   Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
Cyclone V E	A2	25	75	50	25	25	25
	A4	66	198	132	66	66	66
	A5	150	450	300	150	150	150
	A7	156	468	312	156	156	156
	A9	342	1,026	684	342	342	342
Cyclone V GX	C3	57	171	114	57	57	57
	C4	70	210	140	70	70	70
	C5	150	450	300	150	150	150
	C7	156	468	312	156	156	156
	C9	342	1,026	684	342	342	342
Cyclone V GT	D5	150	450	300	150	150	150
	D7	156	468	312	156	156	156
	D9	342	1,026	684	342	342	342
Cyclone V SE	A2	36	108	72	36	36	36
	A4	84	252	168	84	84	84
	A5	87	261	174	87	87	87
	A6	112	336	224	112	112	112
Cyclone V SX	C2	36	108	72	36	36	36
	C4	84	252	168	84	84	84
	C5	87	261	174	87	87	87

PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 9.   PCIe Multifunction for Cyclone V Devices
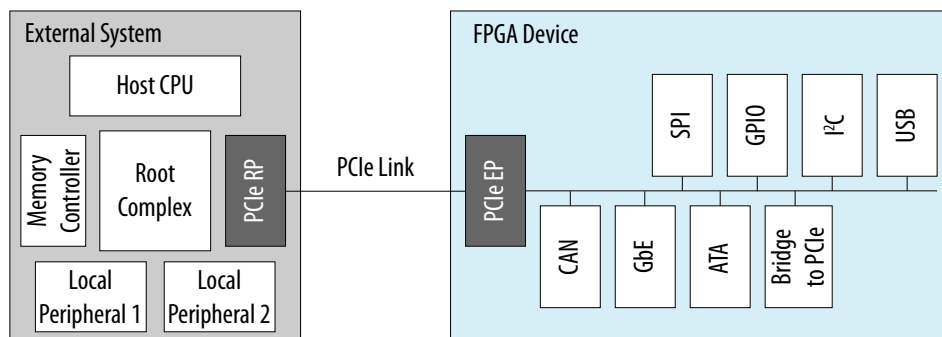
The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.

External Memory Performance

Table 20.   External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21.   HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

Cyclone V Device Family Pin Connection Guidelines
Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

International Altera Sales Support Offices

Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial Reconfiguration

Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

Table 24.   Configuration Schemes and Features Supported by Cyclone V Devices

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration[18]	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	
CvP (PCIe)	x1, x2, and x4 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Related Information

Configuration via Protocol (CvP) Implementation in Intel FPGAs User Guide
   Provides more information about CvP.

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[18] The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.

- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the *Sample Ordering Code and Available Options* diagrams. • Rebranded as Intel.

Date	Version	Changes
December 2017	2017.12.18	• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.
June 2016	2016.06.10	Updated Cyclone V GT speed grade to −7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	• Added descriptions to package plan tables for Cyclone V GT and ST devices. • Changed instances of *Quartus II* to *Quartus Prime*.

June 2015	2015.06.12	• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives.
		• Updated logic elements (LE) (K) for the following devices:
		  — Cyclone V E A7: Updated from 149.5 to 150
		  — Cyclone V GX C3: Updated from 35.5 to 36
		  — Cyclone V GX C7: Updated from 149.7 to 150
		  — Cyclone V GT D7: Updated from 149.5 to 150
		• Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows:
		  — Cyclone V GX C3: Updated from 291 to 182
		  — Cyclone V GX C4: Updated from 678 to 424
		  — Cyclone V GX C5: Updated from 678 to 424
		  — Cyclone V GX C7: Updated from 1,338 to 836
		  — Cyclone V GX C9: Updated from 2,748 to 1,717

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Date	Version	Changes
		• Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C3: Updated from 181 to 182 — Cyclone V GX C4: Updated from 295 to 424 • Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C3: Updated from 1,531 to 1,532 — Cyclone V GX C4: Updated from 2,795 to 2,924 • Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C4: Updated from 472 to 678 — Cyclone V GX C5: Updated from 679 to 678
March 2015	2015.03.31	• Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table. • Added optional suffix "SC: Internal scrubbing support" to the following diagrams: — Sample Ordering Code and Available Options for Cyclone V E Devices — Sample Ordering Code and Available Options for Cyclone V GX Devices — Sample Ordering Code and Available Options for Cyclone V SE Devices — Sample Ordering Code and Available Options for Cyclone V SX Devices
January 2015	2015.01.23	• Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and –7 speed grade. — Operating Temperature: Removed C and A temperature grades — FPGA Fabric Speed Grade: Removed –6 and –8 speed grades • Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps: — Device Variants for the Cyclone V Device Family table — Sample Ordering Code and Available Options for Cyclone V ST Devices figure — Maximum Resource Counts for Cyclone V ST Devices • Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices. — Logic elements (LE) (K): Updated from 35.7 to 35.5 — Variable-precision DSP block: Updated from 51 to 57 — 18 x 18 multiplier: Updated from 102 to 114 • Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. — Variableprecision DSP Block: Updated from 51 to 57 — 9 x 9 Multiplier: Updated from 153 to 171 — 18 x 18 Multiplier: Updated from 102 to 114 — 27 x 27 Multiplier: Updated from 51 to 57 — 18 x 18 Multiplier Adder Mode: Updated from 51 to 57 — 18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57 • Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices. — M10K block: Updated from 119 to 135 — M10K RAM bit (Kb): Updated from 1,190 to 1,350 — MLAB block: Updated from 255 to 291 — MLAB RAM bit (Kb): Updated from 159 to 181 — Total RAM bit (Kb): Updated from 1,349 to 1,531
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.
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Date	Version	Changes
July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	• Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. • Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. • Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. • Added link to Altera Product Selector for each device variant. • Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. • Added leaded package options. • Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. • Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60. • Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120. • Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84. • Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168. • Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252. • Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. • Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37. • Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5. • Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V. • Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. • Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. • Added decompression support for the CvP configuration mode.
May 2013	2013.05.06	• Added link to the known document issues in the Knowledge Base. • Moved all links to the Related Information section of respective topics for easy reference. • Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. • Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. • Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. • Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. • Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. • Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. • Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. • Updated the package plan with M383 for the Cyclone V E device. • Removed the M301 and M383 packages from the Cyclone V GX C4 device. • Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. • Updated 5 Gbps to '6.144 Gbps' forCyclone V GT device.

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