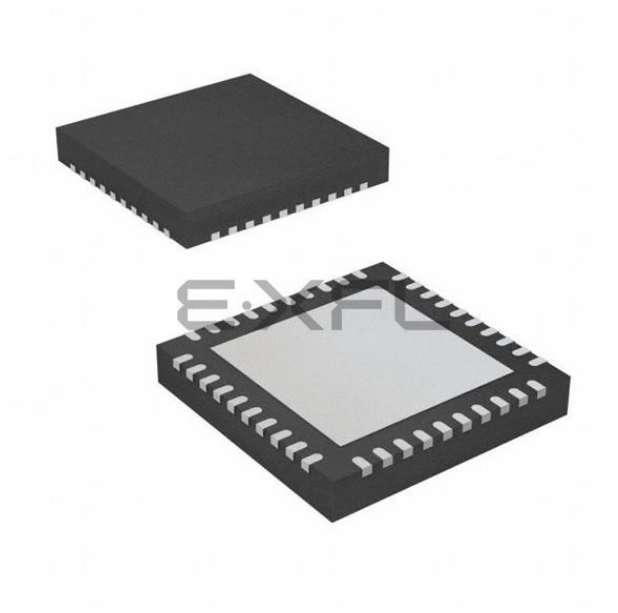

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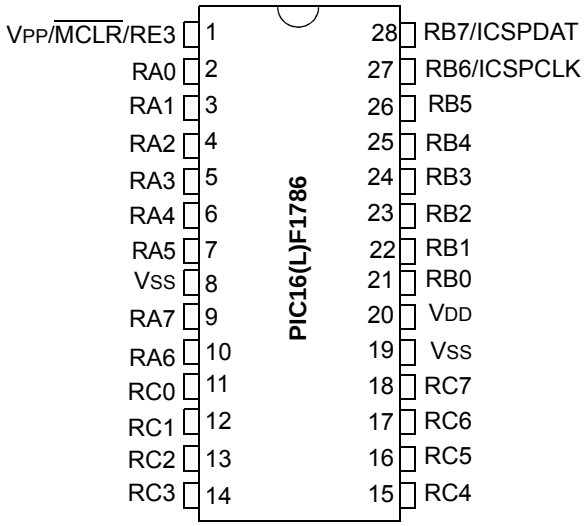
## Applications of "Embedded - Microcontrollers"

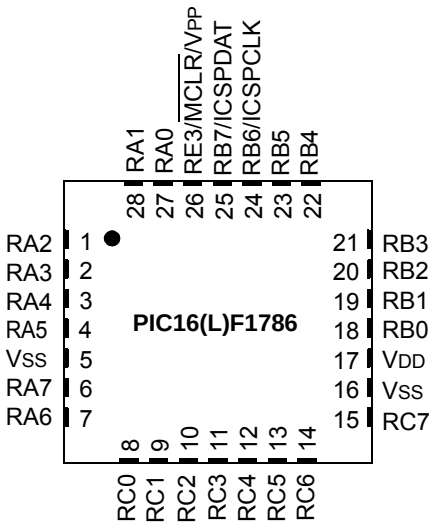
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PSMC, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 14x12b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-UFQFN Exposed Pad |
| Supplier Device Package | 40-UQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f1784-e-mv |

### Pin Diagram – 28-Pin SPDIP, SOIC, SSOP




**Note:** See Table 1 for the location of all peripheral functions.

### Pin Diagram – 28-Pin QFN




**Note:** See Table 1 for the location of all peripheral functions.

**TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 7** | | | | | | | | | | | |
| 38Ch | INLVLA | Input Type Control for PORTA | | | | | | | | 0000 0000 | 0000 0000 |
| 38Dh | INLVLB | Input Type Control for PORTB | | | | | | | | 0000 0000 | 0000 0000 |
| 38Eh | INLVLC | Input Type Control for PORTC | | | | | | | | 1111 1111 | 1111 1111 |
| 38Fh | INLVLD(3) | Input Type Control for PORTD | | | | | | | | 1111 1111 | 1111 1111 |
| 390h | INLVLE | — | — | — | — | INLVLE3 | INLVLE2(3) | INLVLE1(3) | INLVLE0(3) | ---- 1111 | ---- 1111 |
| 391h | IOCAP | IOCAP<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 392h | IOCAN | IOCAN<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 393h | IOCAF | IOCAF<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 394h | IOCBP | IOCBP<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 395h | IOCBN | IOCBN<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 396h | IOCBF | IOCBF<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 397h | IOCCP | IOCCP<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 398h | IOCCN | IOCCN<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 399h | IOCCF | IOCCF<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 39Ah — 39Ch | — | Unimplemented | | | | | | | | — | — |
| 39Dh | IOCEP | — | — | — | — | IOCEP3 | — | — | — | ---- 0--- | ---- 0--- |
| 39Eh | IOCEN | — | — | — | — | IOCEN3 | — | — | — | ---- 0--- | ---- 0--- |
| 39Fh | IOCEF | — | — | — | — | IOCEF3 | — | — | — | ---- 0--- | ---- 0--- |
| **Bank 8-9** | | | | | | | | | | | |
| 40Ch or 41Fh and 48Ch or 49Fh | — | Unimplemented | | | | | | | | — | — |
| **Bank 10** | | | | | | | | | | | |
| 50Ch — 510h | — | Unimplemented | | | | | | | | — | — |
| 511h | OPA1CON | OPA1EN | OPA1SP | — | — | — | — | OPA1PCH<1:0> | | 00-- --00 | 00-- --00 |
| 512h | — | Unimplemented | | | | | | | | — | — |
| 513h | OPA2CON | OPA2EN | OPA2SP | — | — | — | — | OPA2PCH<1:0> | | 00-- --00 | 00-- --00 |
| 514h | — | Unimplemented | | | | | | | | — | — |
| 515h | OPA3CON(3) | OPA3EN | OPA3SP | — | — | — | — | OPA3PCH<1:0> | | 00-- --00 | 00-- --00 |
| 51Ah | CLKRCON | CLKREN | CLKROE | CLKRSLR | CLKRDC<1:0> | | CLKRDIV<2:0> | | | 0011 0000 | 0011 0000 |
| 51Bh — 51Fh | — | Unimplemented | | | | | | | | — | — |

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

**Note 1:** These registers can be addressed from any bank.
**2:** Unimplemented, read as '1'.
**3:** PIC16(L)F1784/7 only.
**4:** PIC16F1784/6/7 only.

**REGISTER 8-9: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4**

| U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | PSMC3TIF | PSMC2TIF | PSMC1TIF | — | PSMC3SIF | PSMC2SIF | PSMC1SIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **Unimplemented:** Read as '0'

bit 6 **PSMC3TIF:** PSMC3 Time Base Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **PSMC2TIF:** PSMC2 Time Base Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **PSMC1TIF:** PSMC1 Time Base Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **Unimplemented:** Read as '0'

bit 2 **PSMC3SIF:** PSMC3 Auto-shutdown Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **PSMC2SIF:** PSMC2 Auto-shutdown Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **PSMC1SIF:** PSMC1 Auto-shutdown Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

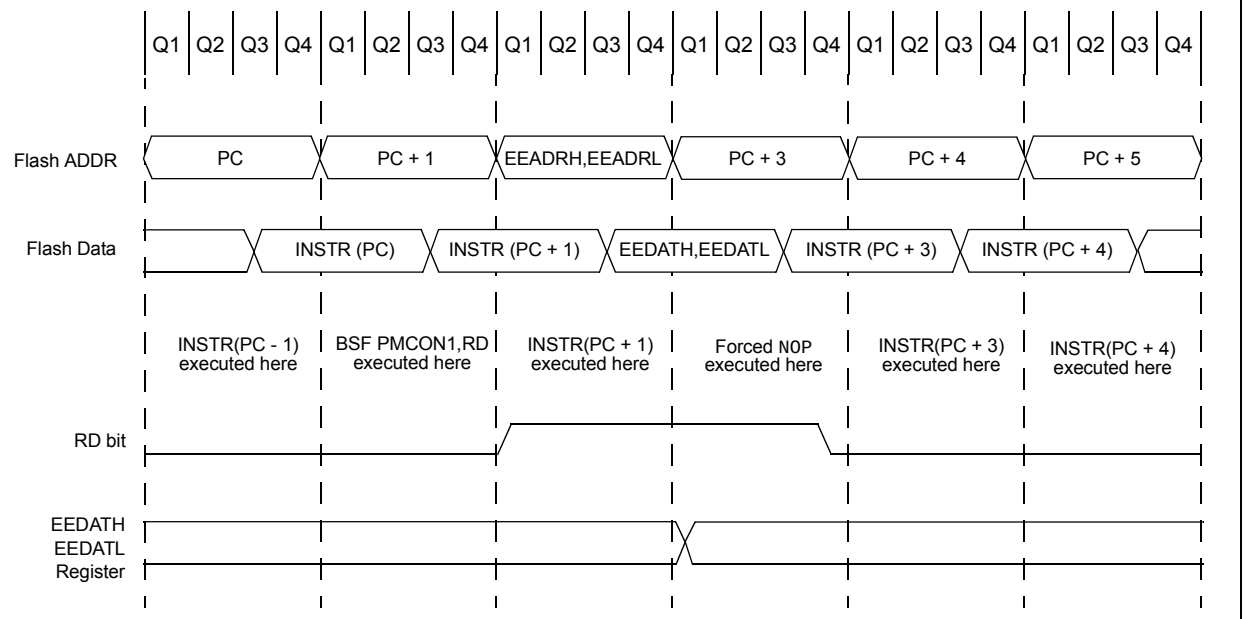
**EXAMPLE 12-2: DATA EEPROM WRITE**

Required Sequence

```
        BANKSEL  EEADRL          ;
        MOVLW    DATA_EE_ADDR    ;
        MOVWF    EEADRL          ;Data Memory Address to write
        MOVLW    DATA_EE_DATA    ;
        MOVWF    EEDATL          ;Data Memory Value to write
        BCF      EECON1, CFGS    ;Deselect Configuration space
        BCF      EECON1, EEPGD   ;Point to DATA memory
        BSF      EECON1, WREN    ;Enable writes

        BCF      INTCON, GIE     ;Disable INTs.
        MOVLW    55h             ;
        MOVWF    EECON2          ;Write 55h
        MOVLW    0AAh            ;
        MOVWF    EECON2          ;Write AAh
        BSF      EECON1, WR      ;Set WR bit to begin write
        BSF      INTCON, GIE     ;Enable Interrupts
        BCF      EECON1, WREN    ;Disable writes
        BTFSC    EECON1, WR      ;Wait for write to complete
        GOTO     $-2             ;Done
```

**FIGURE 12-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION**



**REGISTER 13-29: ANSELD: PORTD ANALOG SELECT REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | ANSD2 | ANSD1 | ANSD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **ANSD<2:0>**: Analog Select between Analog or Digital Function on pins RD<2:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**REGISTER 13-30: WPUD: WEAK PULL-UP PORTD REGISTER**

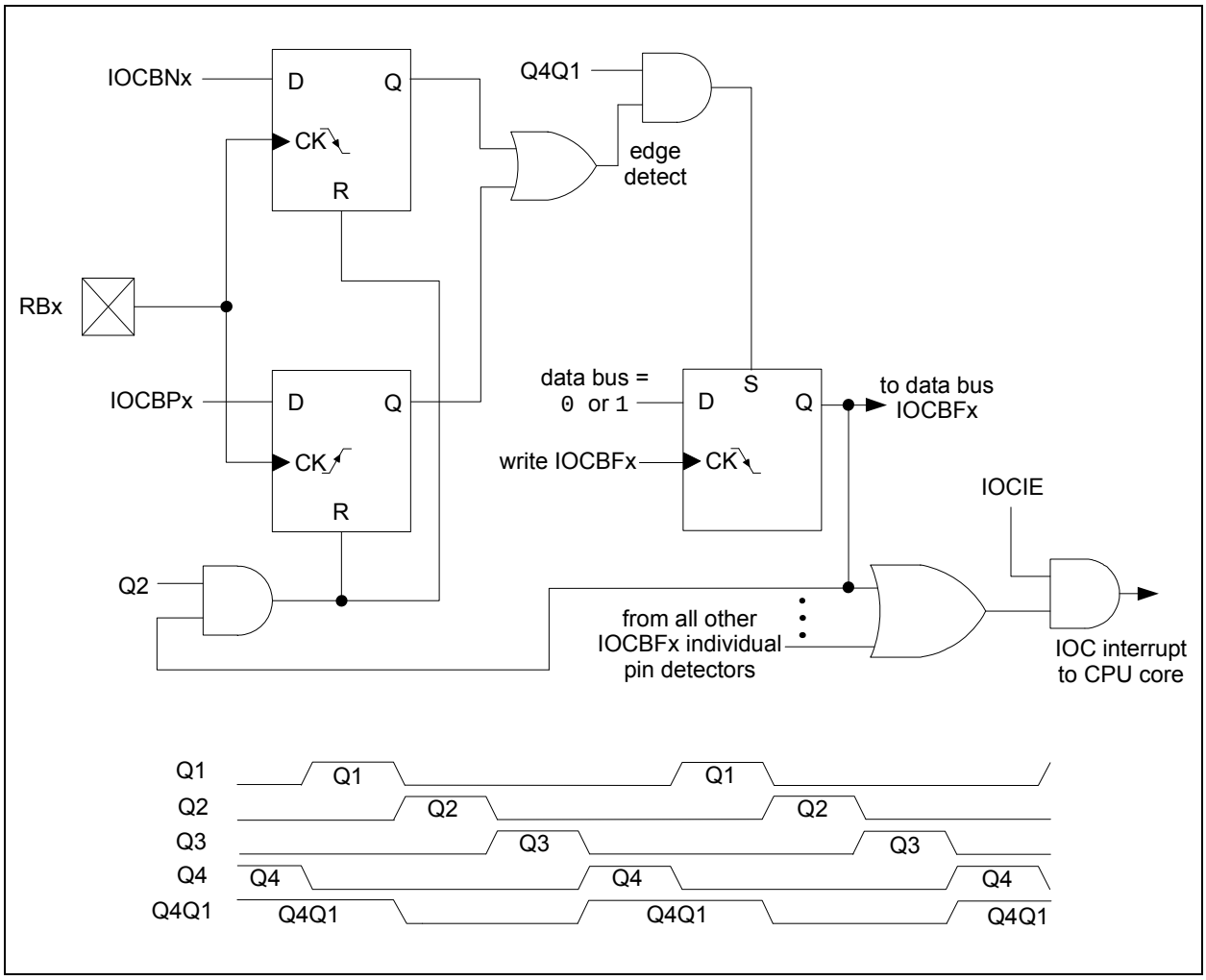
| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| WPUD7 | WPUD6 | WPUD5 | WPUD4 | WPUD3 | WPUD2 | WPUD1 | WPUD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0 **WPUD<7:0>**: Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

**Note 1:** Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.

**FIGURE 14-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM**



## 19.6 Register Definitions: DAC Control

### REGISTER 19-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

| R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| DAC1EN | — | DAC1OE1 | DAC1OE2 | DAC1PSS<1:0> | | — | DAC1NSS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7 **DAC1EN:** DAC1 Enable bit
1 = DAC1 is enabled
0 = DAC1 is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **DAC1OE1:** DAC1 Voltage Output 1 Enable bit
1 = DAC1 voltage level is also an output on the DAC1OUT1 pin
0 = DAC1 voltage level is disconnected from the DAC1OUT1 pin

bit 4 **DAC1OE2:** DAC1 Voltage Output 2 Enable bit
1 = DAC1 voltage level is also an output on the DAC1OUT2 pin
0 = DAC1 voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 **DAC1PSS<1:0>:** DAC1 Positive Source Select bits
11 = Reserved, do not use
10 = FVR Buffer2 output
01 = $V_{REF+}$ pin
00 = $V_{DD}$

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **DAC1NSS:** DAC1 Negative Source Select bits
1 = $V_{REF-}$ pin
0 = $V_{SS}$

### REGISTER 19-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| DAC1R<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **DAC1R<7:0>:** DAC1 Voltage Output Select bits

### TABLE 19-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC MODULE

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on page |
|---|---|---|---|---|---|---|---|---|---|
| FVRCON | FVREN | FVRRDY | TSEN | TSRNG | CDAFVR<1:0> | | ADFVR<1:0> | | **162** |
| DAC1CON0 | DAC1EN | — | DAC1OE1 | DAC1OE2 | DAC1PSS<1:0> | | — | DAC1NSS | **186** |
| DAC1CON1 | DAC1R<7:0> | | | | | | | | **186** |

**Legend:** — = Unimplemented location, read as ‘0’. Shaded cells are not used with the DAC module.

**REGISTER 22-2: T1GCON: TIMER1 GATE CONTROL REGISTER**

| R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W/HC-0/u | R-x/x | R/W-0/u | R/W-0/u |
|---|---|---|---|---|---|---|---|
| TMR1GE | T1GPOL | T1GTM | T1GSPM | T1GGO/$\overline{\text{DONE}}$ | T1GVAL | T1GSS<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | HC = Bit is cleared by hardware |

bit 7 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle Mode bit

1 = Timer1 Gate Toggle mode is enabled
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single-Pulse Mode bit

1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 Gate Single-Pulse mode is disabled

bit 3 **T1GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit

1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started

bit 2 **T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1-0 **T1GSS<1:0>:** Timer1 Gate Source Select bits

11 = Comparator 2 optionally synchronized output (sync_C2OUT)
10 = Comparator 1 optionally synchronized output (sync_C1OUT)
01 = Timer0 overflow output
00 = Timer1 gate pin

**TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| CCP2CON | — | — | DC2B<1:0> | | CCP2M<3:0> | | | | 280 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 94 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| PR2 | Timer2 Module Period Register | | | | | | | | 210* |
| T2CON | — | T2OUTPS<3:0> | | | | TMR2ON | T2CKPS<1:0> | | 212 |
| TMR2 | Holding Register for the 8-bit TMR2 Register | | | | | | | | 210* |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

* Page provides register information.

### 25.3.7 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

### 25.3.8 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 6.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for additional details.

### 25.3.9 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

**TABLE 25-3: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| APFCON1 | C2OUTSEL | CC1PSEL | SDOSEL | SCKSEL | SDISEL | TXSEL | RXSEL | CCP2SEL | 127 |
| APFCON2 | — | — | — | — | — | — | — | CCP3SEL | 280 |
| CCP1CON | — | — | DC1B<1:0> | | CCP1M<3:0> | | | | 280 |
| CCP2CON | — | — | DC2B<1:0> | | CCP2M<3:0> | | | | 280 |
| CCP33CON | — | — | DC3B<1:0> | | CCP3M<3:0> | | | | 280 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 93 |
| PIE2 | OSFIE | C2IE | C1IE | EEIE | BCL1IE | C4IE | C3IE | CCP2IE | 95 |
| PIE3 | — | — | — | CCP3IE | — | — | — | — | 96 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| PIR2 | OSFIF | C2IF | C1IF | EEIF | BCL1IF | C4IF | C3IF | CCP2IF | 99 |
| PIR3 | — | — | — | CCP3IF | — | — | — | — | 100 |
| PR2 | Timer2 Period Register | | | | | | | | 210* |
| T2CON | — | T2OUTPS<3:0> | | | | TMR2ON | T2CKPS<1:0> | | 212 |
| TMR2 | Timer2 Module Register | | | | | | | | 210 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 131 |

**Legend:** — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.
* Page provides register information.

### 26.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all 8 bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

**TABLE 26-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| ANSELA | ANSA7 | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | 132 |
| APFCON1 | C2OUTSEL | CCP1SEL | SDOSEL | SCKSEL | SDISEL | TXSEL | RXSEL | CCP2SEL | 127 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 94 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| SSP1BUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | 285* |
| SSP1CON1 | WCOL | SSPOV | SSPEN | CKP | SSPM<3:0> | | | | 331 |
| SSP1CON3 | ACKTIM | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN | 333 |
| SSP1STAT | SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF | 329 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 131 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISA0 | 142 |

**Legend:** — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

**Note 1:** PIC16(L)F1784/7 only.

### 26.6.7 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

| **Note:** | The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded. |
|---|---|

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

#### 26.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

#### 26.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

#### 26.6.7.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

#### 26.6.7.4 Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/$\overline{W}$ bit set.
5. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
8. User sets the RCEN bit of the SSPCON2 register and the master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSP1IF and BF are set.
10. User clears the SSP1IF bit and reads the received byte from SSPUF, which clears the BF flag.
11. The user either clears the SSPCON2 register's ACKDT bit to receive another byte or sets the ADKDT bit to suppress further data and then initiates the acknowledge sequence by setting the ACKEN bit.
12. Master's ACK or $\overline{ACK}$ is clocked out to the slave and SSP1IF is set.
13. User clears SSP1IF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. If the ACKST bit was set in step 11 then the user can send a STOP to release the bus.

### 26.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level.
b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 26-35). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 26-36.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

**FIGURE 26-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)**

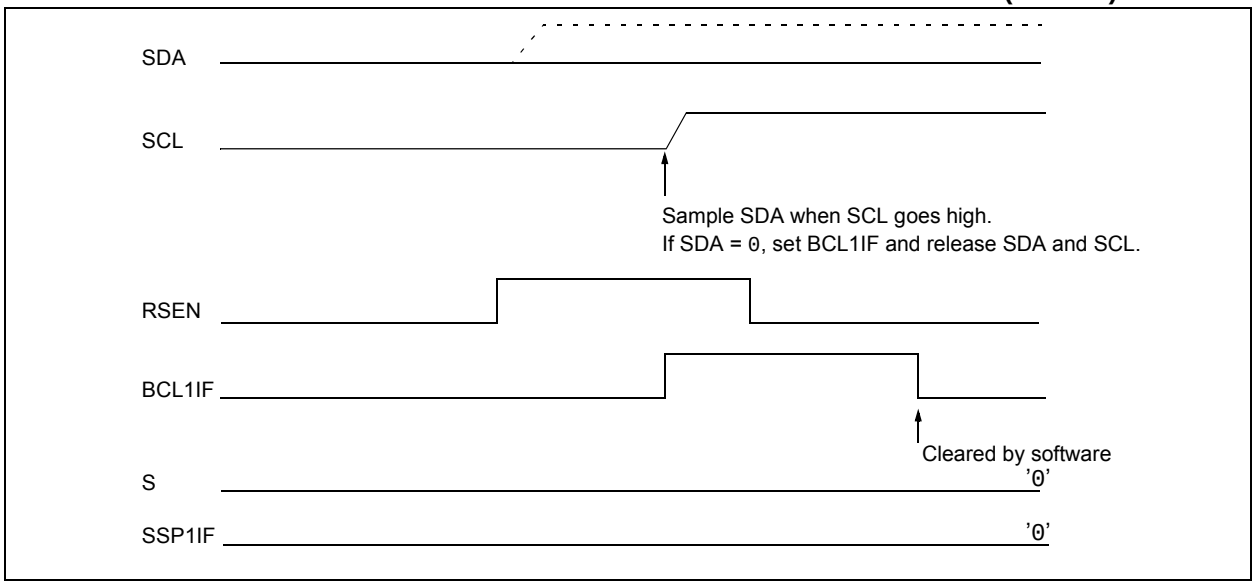
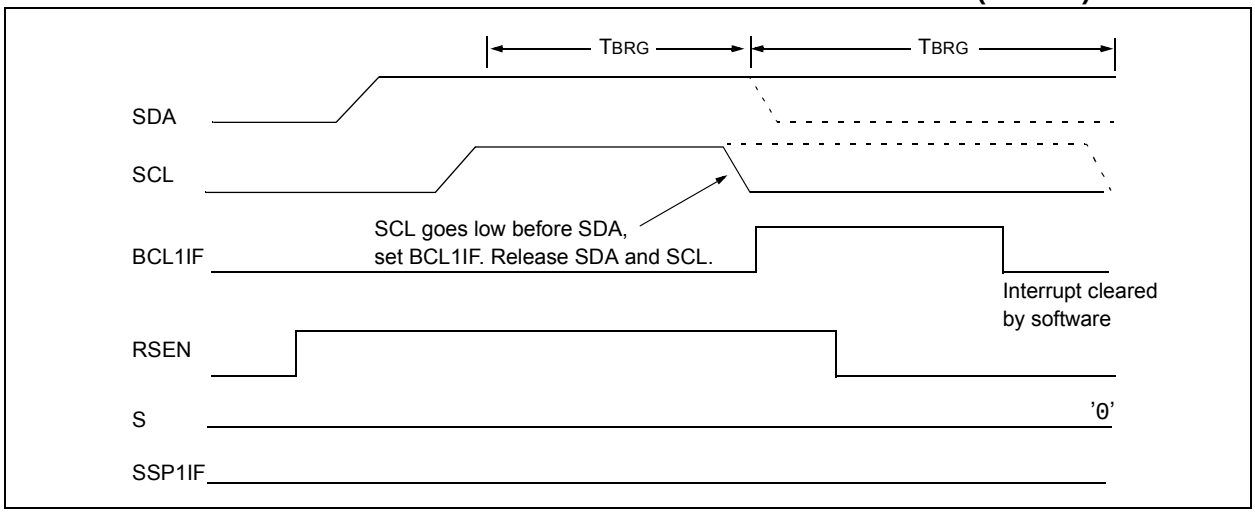



**FIGURE 26-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)**



## 26.8 Register Definitions: MSSP Control

### REGISTER 26-1: SSPSTAT: SSP STATUS REGISTER

| R/W-0/0 | R/W-0/0 | R-0/0 | R-0/0 | R-0/0 | R-0/0 | R-0/0 | R-0/0 |
|---|---|---|---|---|---|---|---|
| SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **SMP:** SPI Data Input Sample bit

SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode

In $I^2C$ Master or Slave mode:
1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for high speed mode (400 kHz)

bit 6 **CKE:** SPI Clock Edge Select bit (SPI mode only)

In SPI Master or Slave mode:
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state

In $I^2C$™ mode only:
1 = Enable input logic so that thresholds are compliant with SMBus specification
0 = Disable SMBus specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit ($I^2C$ mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit
($I^2C$ mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)
0 = Stop bit was not detected last

bit 3 **S:** Start bit
($I^2C$ mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
0 = Start bit was not detected last

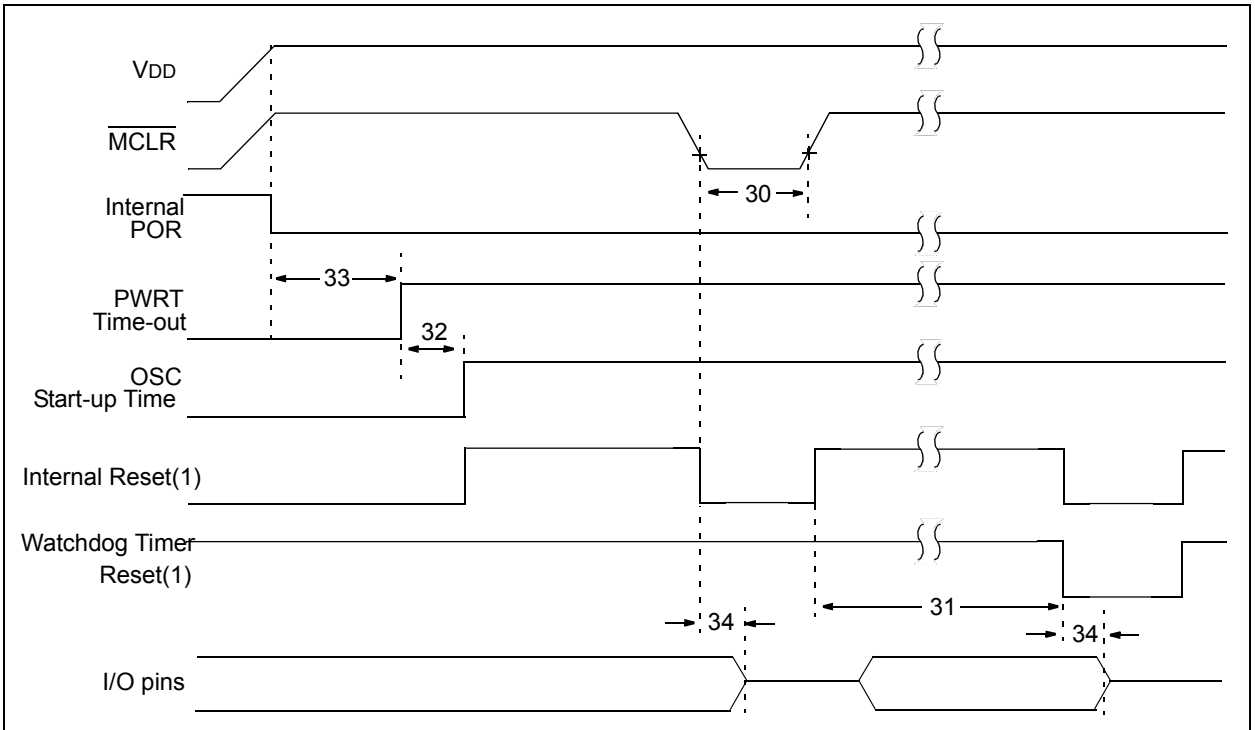
bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information ($I^2C$ mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit.

In $I^2C$ Slave mode:
1 = Read
0 = Write

In $I^2C$ Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

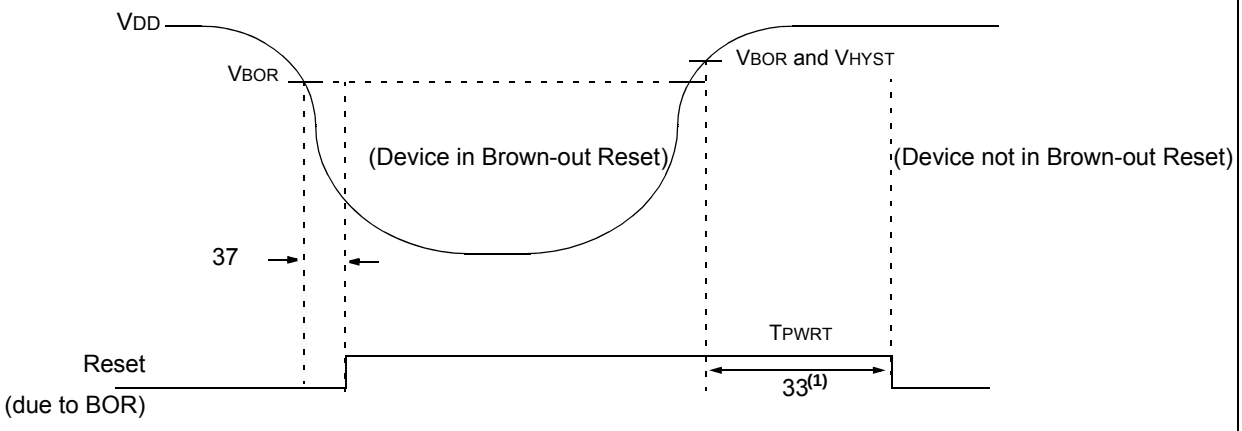
bit 1 **UA:** Update Address bit (10-bit $I^2C$ mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

**FIGURE 30-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




**Note 1:** Asserted low.

**FIGURE 30-9: BROWN-OUT RESET TIMING AND CHARACTERISTICS**




**Note 1:** The delay, (TPWRT) releasing Reset, only occurs when the Power-up Timer is enabled, ($\overline{PWRTE}$ = 0).

**TABLE 30-13: ADC CONVERTER (ADC) 12-BIT DIFFERENTIAL CHARACTERISTICS:**

| **Operating Conditions** $V_{DD}$ = 3V, Temp. = 25°C, Single-ended 2 μs TAD, $V_{REF+}$ = 3V, $V_{REF-}$ = $V_{SS}$ | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| AD01 | $N_R$ | Resolution | — | — | 10 | bit | |
| AD02 | $E_{IL}$ | Integral Error | — | ±1 | ±1.6 | LSb | |
| AD03 | $E_{DL}$ | Differential Error | — | ±1 | ±1.4 | LSb | No missing codes |
| AD04 | $E_{OFF}$ | Offset Error | — | ±1 | ±3.5 | LSb | |
| AD05 | $E_{GN}$ | Gain Error | — | ±1 | ±2 | LSb | |
| AD06 | $V_{REF}$ | Reference Voltage(3) | 1.8 | — | $V_{DD}$ | V | $V_{REF}$ = ($V_{REF+}$ minus $V_{REF-}$) |
| AD07 | $V_{AIN}$ | Full-Scale Range | — | — | $V_{REF}$ | V | |
| AD08 | $Z_{AIN}$ | Recommended Impedance of Analog Voltage Source | — | — | 10 | kΩ | Can go higher if external 0.01μF capacitor is present on input pin. |
| AD09 | $N_R$ | Resolution | — | — | 12 | bit | |
| AD10 | $E_{IL}$ | Integral Error | — | ±2 | — | LSb | |
| AD11 | $E_{DL}$ | Differential Error | — | ±2 | — | LSb | |
| AD12 | $E_{OFF}$ | Offset Error | — | ±1 | — | LSb | |
| AD13 | $E_{GN}$ | Gain Error | — | ±1 | — | LSb | |
| AD14 | $V_{REF}$ | Reference Voltage(3) | 1.8 | — | $V_{DD}$ | V | $V_{REF}$ = ($V_{REF+}$ minus $V_{REF-}$) |
| AD15 | $V_{AIN}$ | Full-Scale Range | — | — | $V_{REF}$ | V | |
| AD16 | $Z_{AIN}$ | Recommended Impedance of Analog Voltage Source | — | — | 10 | kΩ | Can go higher if external 0.01μF capacitor is present on input pin. |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Total Absolute Error includes integral, differential, offset and gain errors.

**2:** The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.

**3:** ADC $V_{REF}$ is from external $V_{REF}$, $V_{DD}$ pin or FVR, whichever is selected as reference input.

**4:** When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

**TABLE 30-14: ADC CONVERSION REQUIREMENTS**

| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| AD130* | $T_{AD}$ | ADC Clock Period | 1.0 | — | 9.0 | μs | $T_{OSC}$-based |
| | | ADC Internal RC Oscillator Period | 1.0 | 2.5 | 6.0 | μs | ADCS<1:0> = 11 (ADRC mode) |
| AD131 | $T_{CNV}$ | Conversion Time (not including Acquisition Time)(1) | — | 15 (12-bit) 13 (10-bit) | — | $T_{AD}$ | Set GO/$\overline{\text{DONE}}$ bit to conversion complete |
| AD132* | $T_{ACQ}$ | Acquisition Time | — | 5.0 | — | μs | |

* These parameters are characterized but not tested.

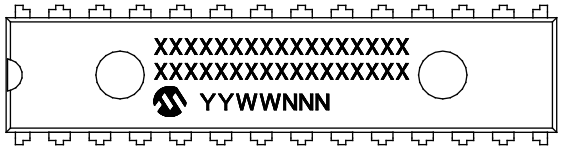
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The ADRES register may be read on the following $T_{CY}$ cycle.

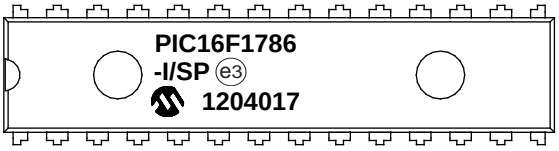
## 33.0 PACKAGING INFORMATION

### 33.1 Package Marking Information

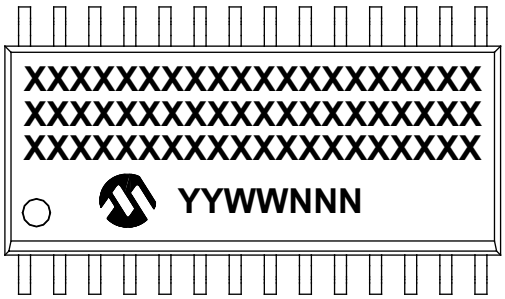
28-Lead SPDIP (.300")



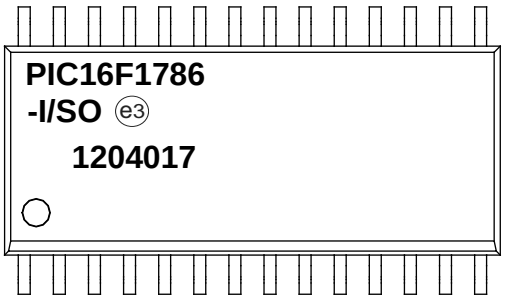

Example



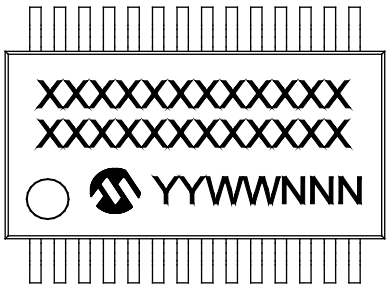

28-Lead SOIC (7.50 mm)



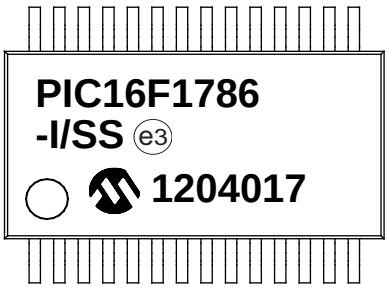

Example




28-Lead SSOP (5.30 mm)




Example

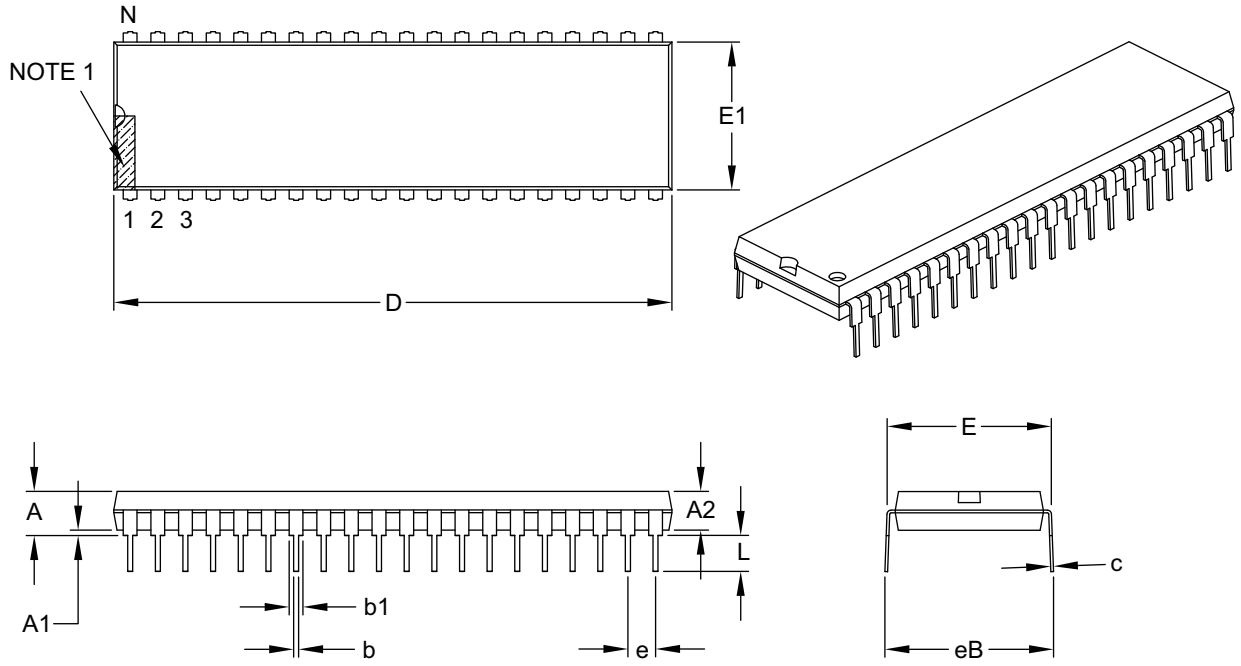



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 40 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .250 |
| Molded Package Thickness | A2 | .125 | – | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .590 | – | .625 |
| Molded Package Width | E1 | .485 | – | .580 |
| Overall Length | D | 1.980 | – | 2.095 |
| Tip to Seating Plane | L | .115 | – | .200 |
| Lead Thickness | c | .008 | – | .015 |
| Upper Lead Width | b1 | .030 | – | .070 |
| Lower Lead Width | b | .014 | – | .023 |
| Overall Row Spacing § | eB | – | – | .700 |

**Notes:**

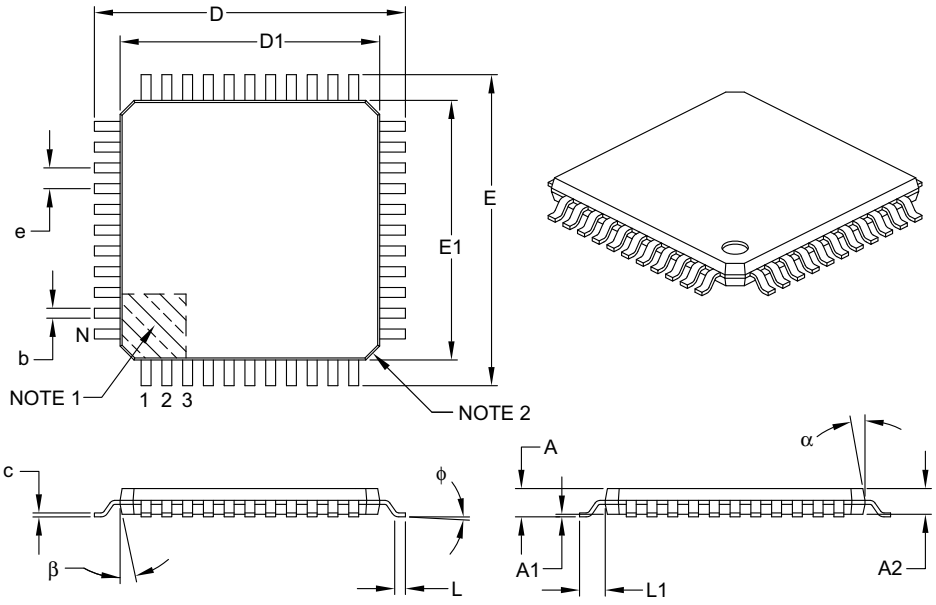
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

### 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 44 | |
| Lead Pitch | e | | 0.80 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | φ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.30 | 0.37 | 0.45 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

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