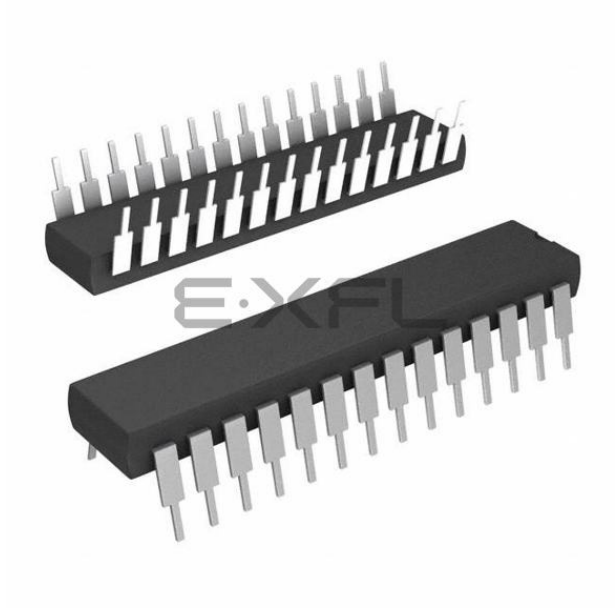

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1786-e-sp

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0											
00Ch	PORTA	PORTA Data Latch when written: PORTA pins when read								xxxx xxxx	uuuu uuuu
00Dh	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
00Eh	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
00Fh	PORTD(3)	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
010h	PORTE	—	—	—	—	RE3	RE2(3)	RE1(3)	RE0(3)	---- xxxx	---- uuuu
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	0000 0-00	0000 0-00
13h	PIR3	—	—	—	CCP3IF	—	—	—	—	---0 ----	0000 0000
014h	PIR4	—	PSMC3TIF	PSMC2TIF	PSMC1TIF	—	PSMC3SIF	PSMC2SIF	PSMC1SIF	-000 -000	-000 -000
015h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
016h	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
017h	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
018h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		0000 0x00	uuuu uxuu
016h	TMR2	Holding Register for the Least Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
017h	PR2	Holding Register for the Most Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
018h	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
01Dh to 01Fh	—	Unimplemented								—	—
Bank 1											
08Ch	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
08Dh	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
08Eh	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
08Fh	TRISD(3)	PORTD Data Direction Register								1111 1111	1111 1111
090h	TRISE	—	—	—	—	—(2)	TRISE2(3)	TRISE1(3)	TRISE0(3)	---- 1111	---- 1111
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
092h	PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	0000 0-00	0000 0-00
093h	PIE3	—	—	—	CCP3IE	—	—	—	—	---0 ----	0000 0000
094h	PIE4	—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE	-000 -000	-000 -000
095h	OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	00-1 11qq	qq-q qquu
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
098h	OSCTUNE	—	—	TUN<5:0>						--00 0000	--00 0000
099h	OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		0011 1-00	0011 1-00
09Ah	OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	00q0 --00	qqqq --0q
09Bh	ADRESL	A/D Result Register Low								xxxx xxxx	uuuu uuuu
09Ch	ADRESH	A/D Result Register High								xxxx xxxx	uuuu uuuu
09Dh	ADCON0	ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
09Eh	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
09Fh	ADCON2	TRIGSEL<3:0>				CHSN<3:0>				000- -000	000- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 31											
F8Ch to FE3h	—	Unimplemented								—	—
FE4h	STATUS_ SHAD	—	—	—	—	—	Z	DC	C	---- -xxx	---- -uuu
FE5h	WREG_SHAD	Working Register Shadow								xxxx xxxx	uuuu uuuu
FE6h	BSR_SHAD	—	—	—	Bank Select Register Shadow					---x xxxx	---u uuuu
FE7h	PCLATH_ SHAD	—	Program Counter Latch High Register Shadow							-xxx xxxx	uuuu uuuu
FE8h	FSR0L_SHAD	Indirect Data Memory Address 0 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FE9h	FSR0H_ SHAD	Indirect Data Memory Address 0 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FEAh	FSR1L_SHAD	Indirect Data Memory Address 1 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FEBh	FSR1H_ SHAD	Indirect Data Memory Address 1 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack Pointer					---1 1111	---1 1111
FEEh	TOSL	Top of Stack Low byte								xxxx xxxx	uuuu uuuu
FEFh	TOSH	—	Top of Stack High byte							-xxx xxxx	-uuu uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

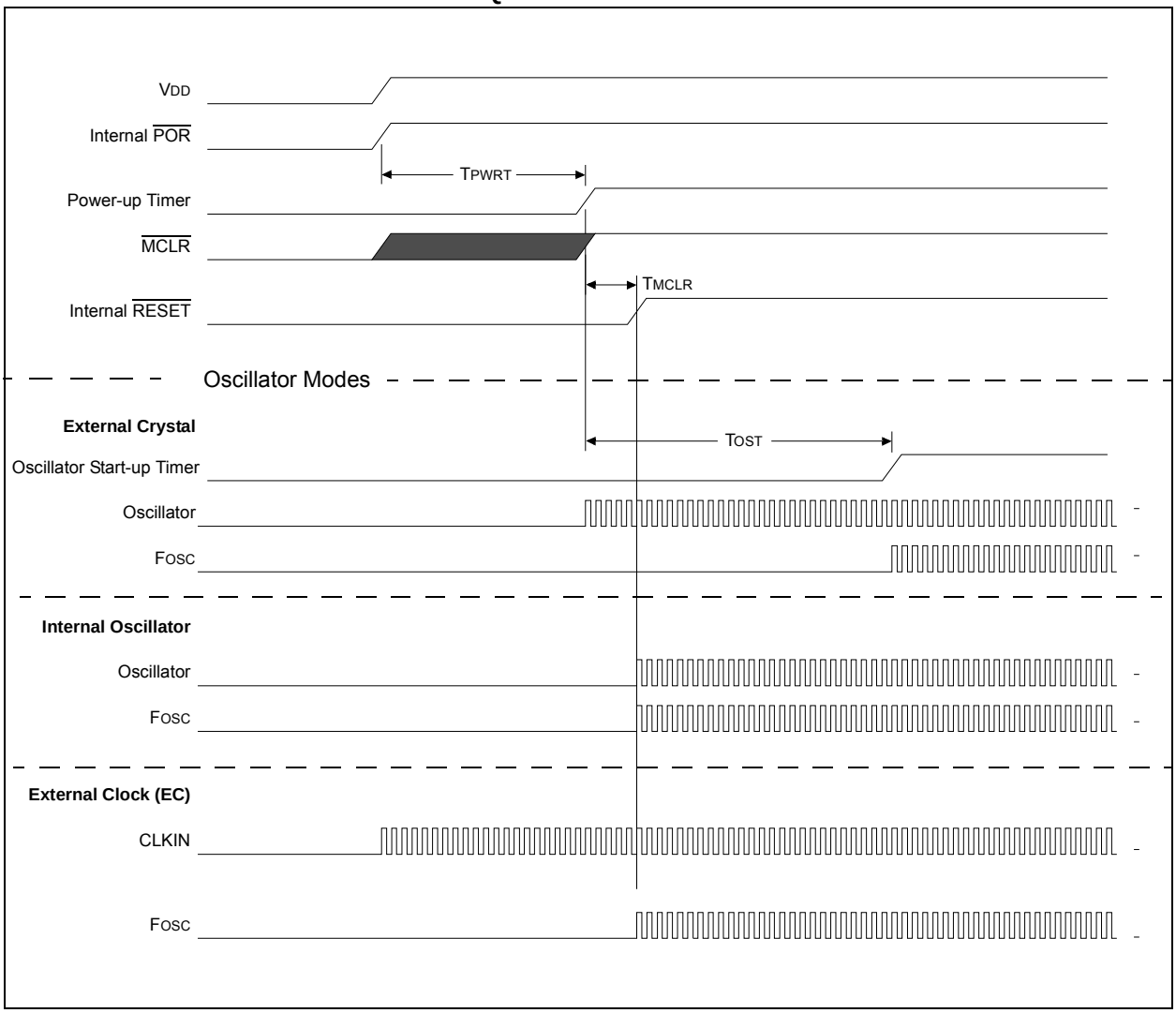
Note 1: These registers can be addressed from any bank.

2: Unimplemented, read as '1'.

3: PIC16(L)F1784/7 only.

4: PIC16F1784/6/7 only.

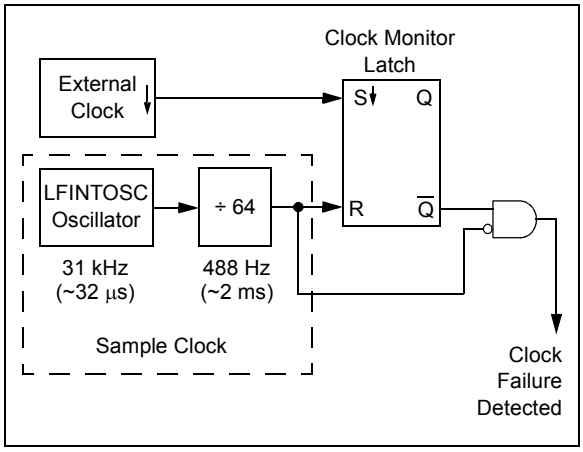
FIGURE 5-3: RESET START-UP SEQUENCE



6.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, Timer1 Oscillator and RC).

FIGURE 6-9: FSCM BLOCK DIAGRAM



6.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 6-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

6.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<3:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

6.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

6.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note:	Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the Status bits in the OSCSTAT register to verify the oscillator start-up and that the system clock switchover has successfully completed.

REGISTER 8-7: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **C2IF:** Comparator C2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **EEIF:** EEPROM Write Completion Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **BCL1IF:** MSSP Bus Collision Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **C4IF:** Comparator C4 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **C3IF:** Comparator C3 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

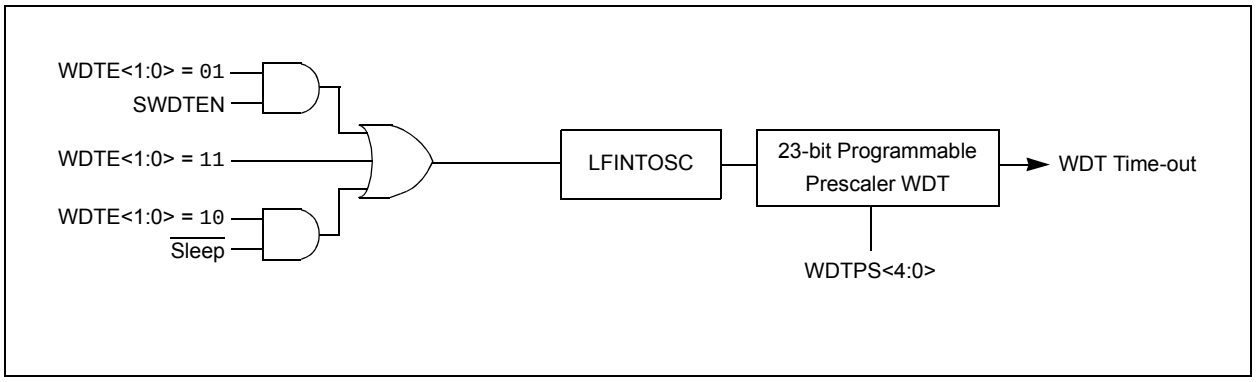
11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 13-2: APFCON2: ALTERNATE PIN FUNCTION CONTROL 2 REGISTER

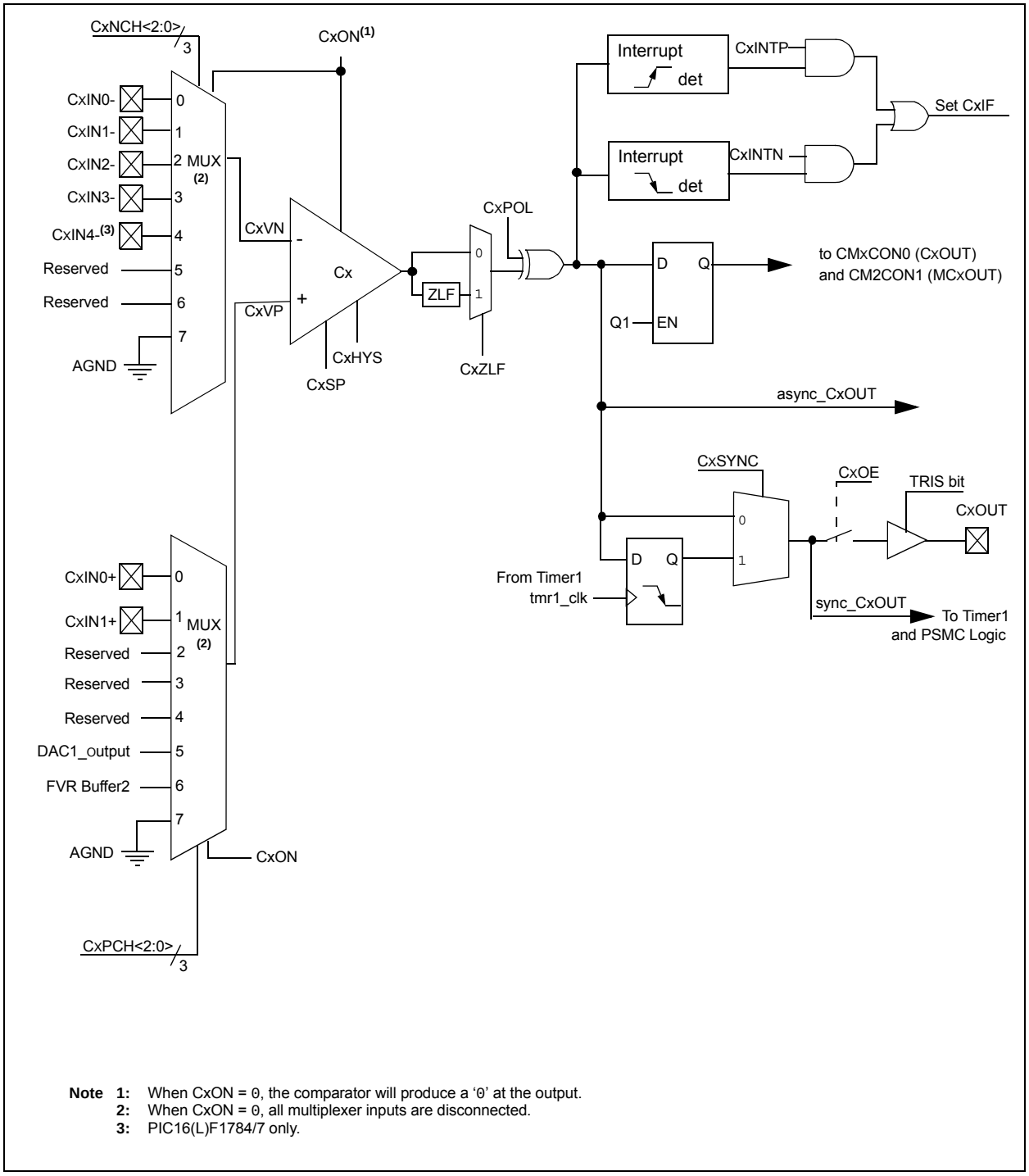
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	CCP3SEL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-1 **Unimplemented:** Read as '0'

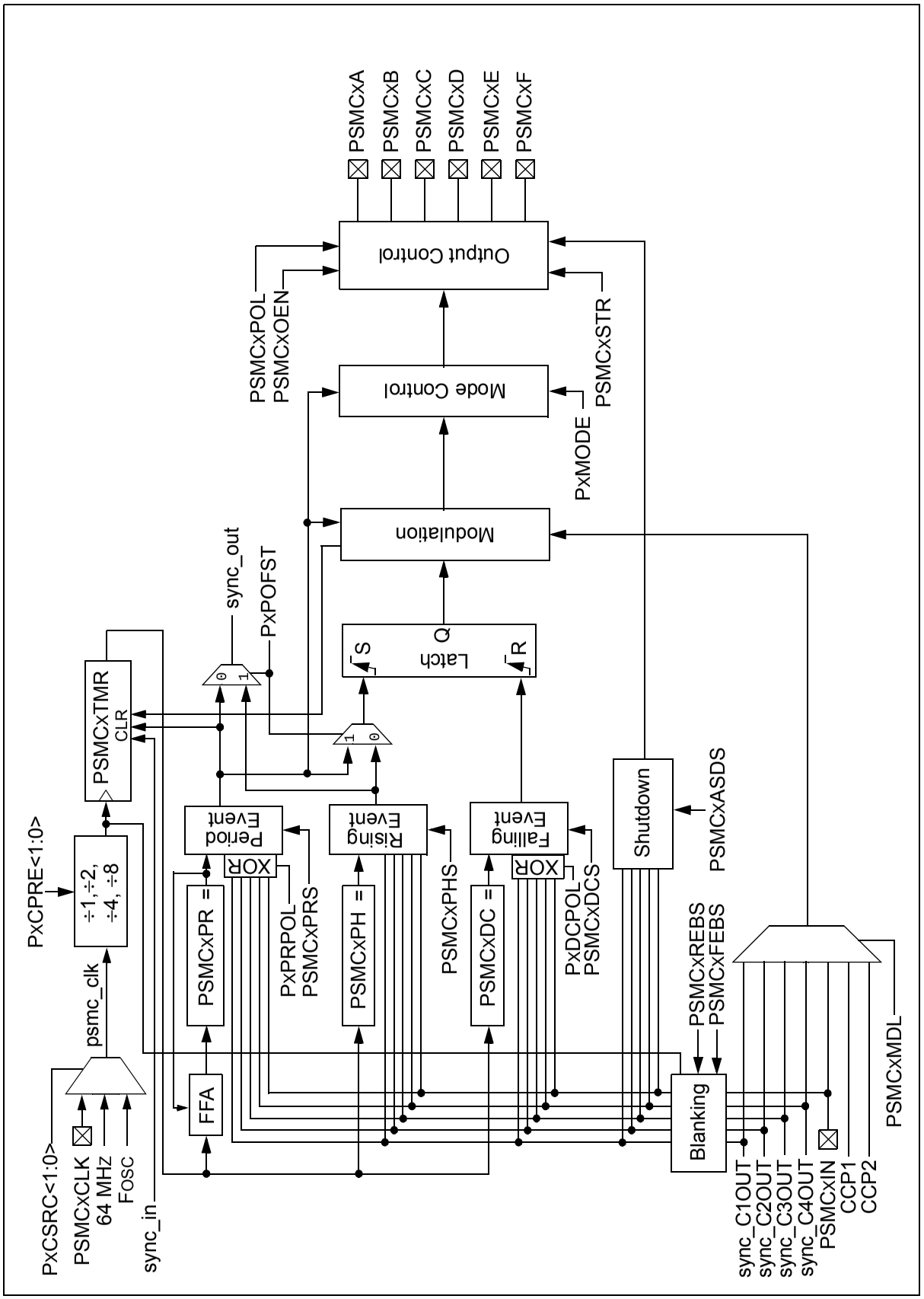
bit 0 **CCP3SEL**: CCP3 Input/Output Pin Selection bit
1 = CCP3 is on pin RB5
PIC16(L)F1786 devices:
0 = CCP3 is on pin RC6
PIC16(L)F1784/7 devices:
0 = CCP3 is on pin RE0

FIGURE 20-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



Note 1: When CxON = 0, the comparator will produce a '0' at the output.
2: When CxON = 0, all multiplexer inputs are disconnected.
3: PIC16(L)F1784/7 only.

FIGURE 24-1: PSMC SIMPLIFIED BLOCK DIAGRAM



24.3.4 PUSH-PULL PWM WITH COMPLEMENTARY OUTPUTS

The complementary push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge. The PWM waveform is output on four pins presented as two pairs of two-output signals with a normal and complementary output in each pair. Dead band can be inserted between the normal and complementary outputs at the transition times.

24.3.4.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM output is only on:
  - PSMCxA
  - PSMCxB
- Complementary PWM output is only on:
  - PSMCxE
  - PSMCxF

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See **Section 24.3.6 "Push-Pull PWM with Four Full-Bridge and Complementary Outputs"**.

24.3.4.2 Waveform Generation

Push-Pull waveforms generate alternating outputs on the output pairs. Therefore, there are two sets of rising edge events and two sets of falling edge events

Odd numbered period rising edge event:

- PSMCxE is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxA is set active

Odd numbered period falling edge odd event:

- PSMCxA is set inactive
- Dead-band falling is activated (if enabled)
- PSMCxE is set active

Even numbered period rising edge event:

- PSMCxF is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxB is set active

Even numbered period falling edge event:

- PSMCxB is set inactive
- Dead-band falling is activated (if enabled)
- PSMCxF is set active

FIGURE 24-7: PUSH-PULL WITH COMPLEMENTARY OUTPUTS PWM WAVEFORM

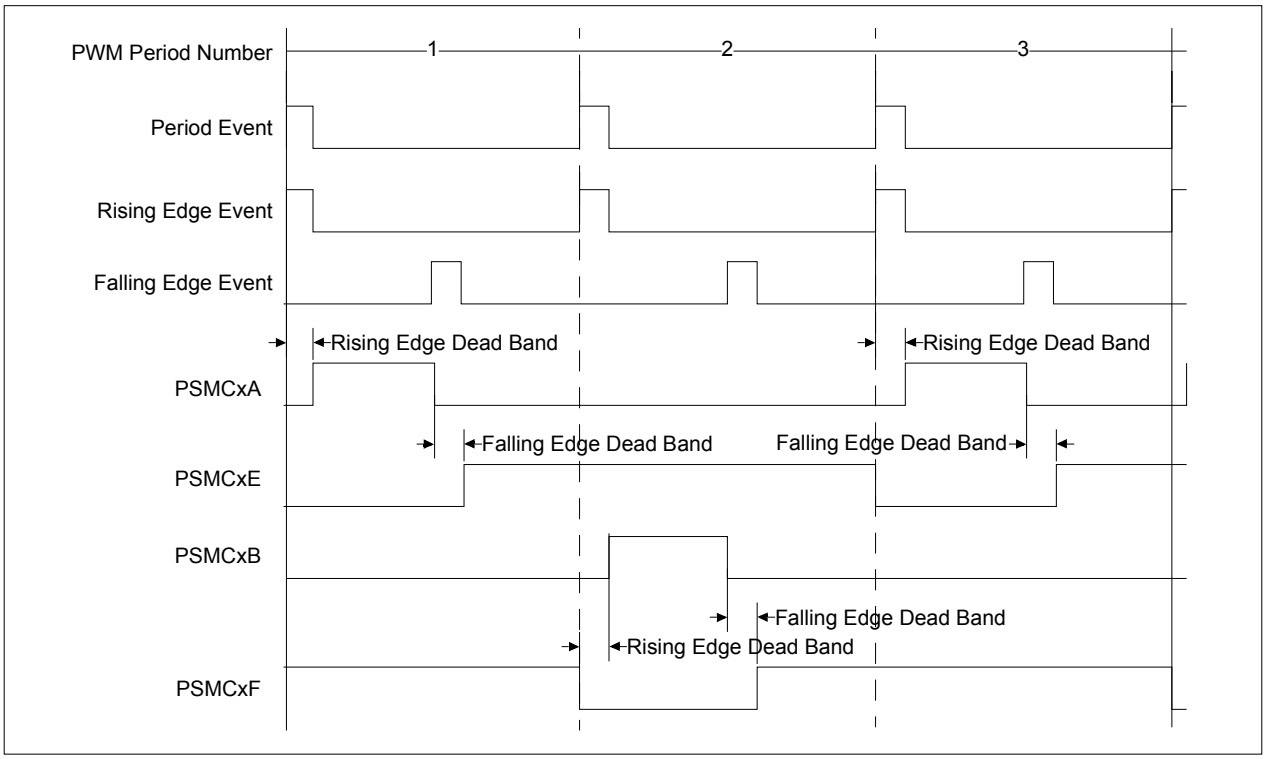


FIGURE 24-15: 3-PHASE PWM STEERING WAVEFORM (PXHSMEN = 0 AND PXLSMEN = 1)

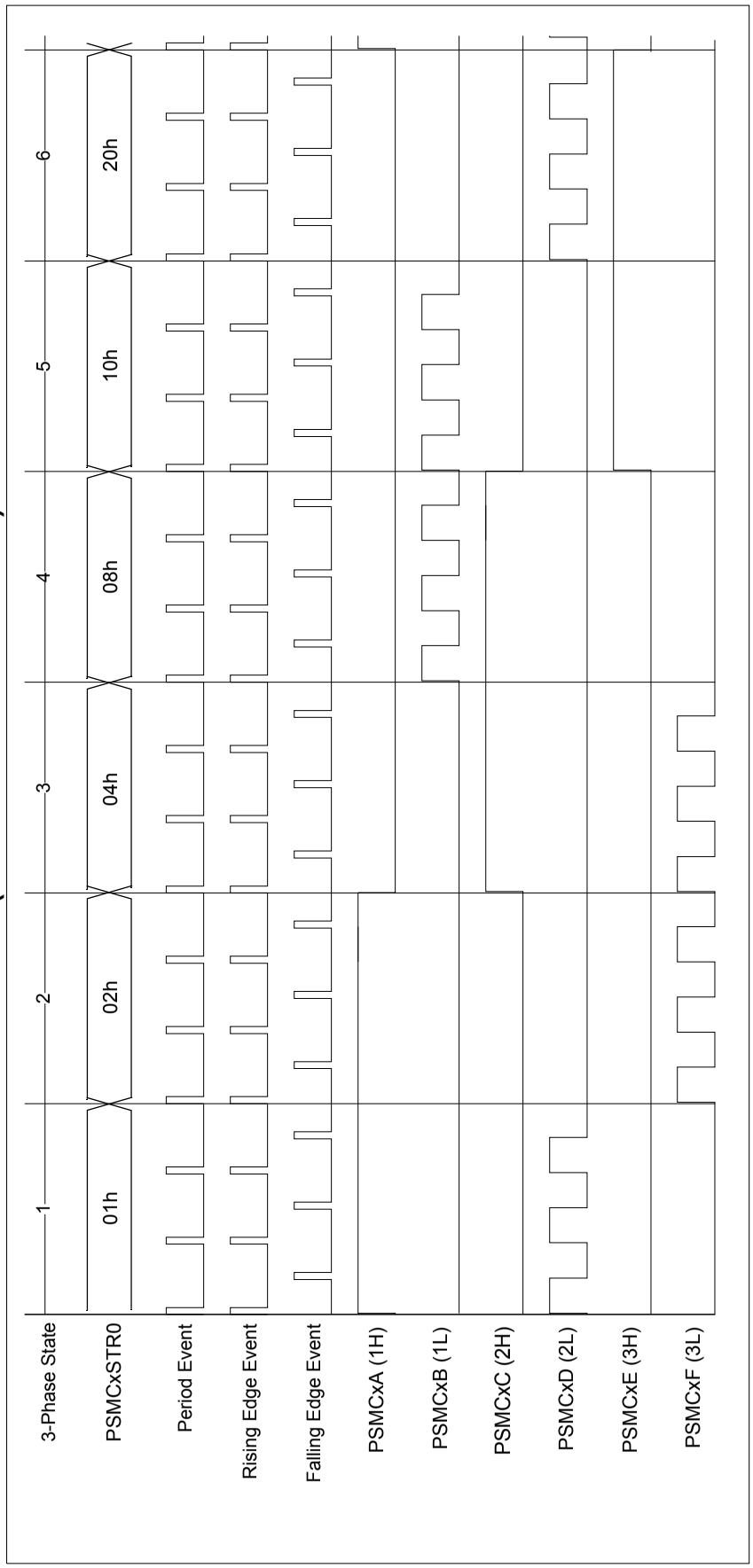
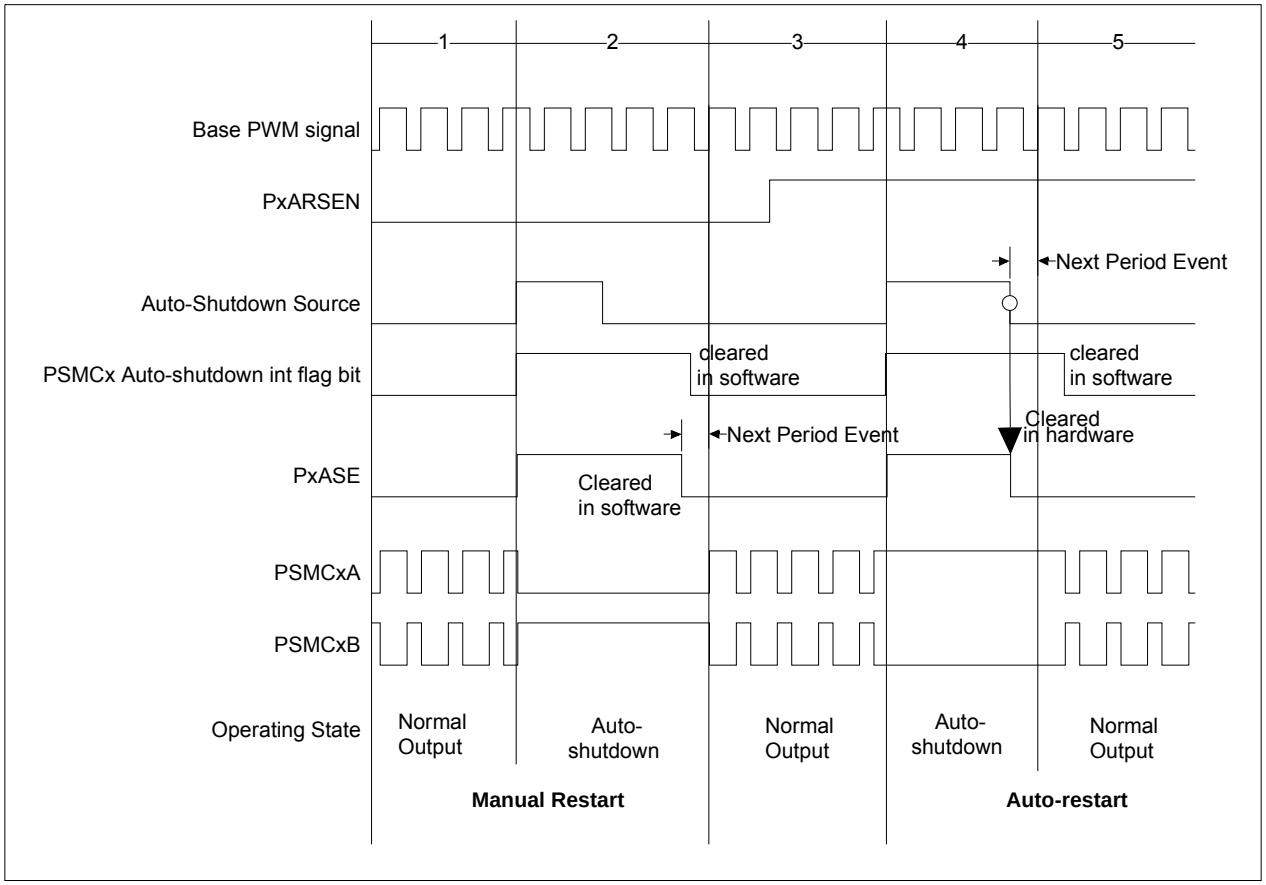


FIGURE 24-20: AUTO-SHUTDOWN AND RESTART WAVEFORM

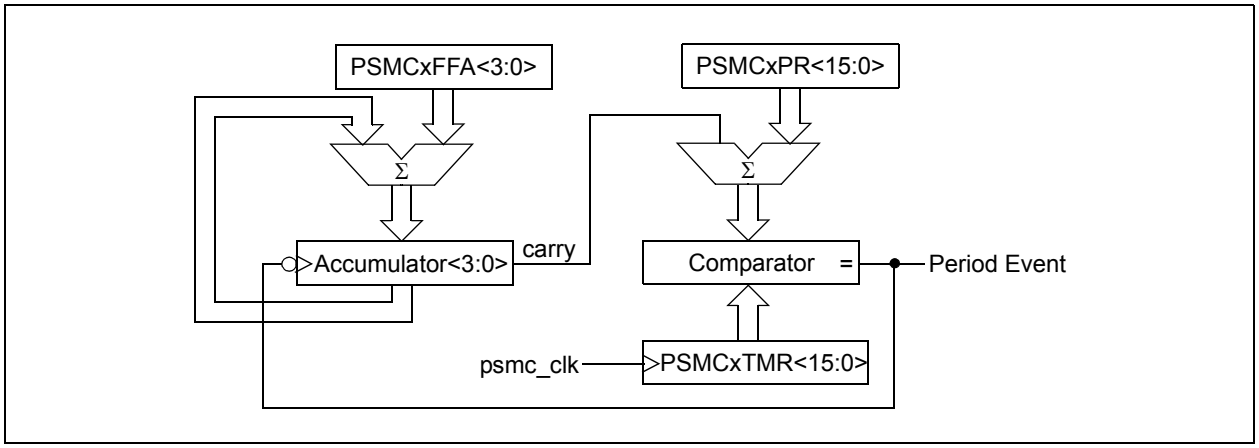


24.9 Fractional Frequency Adjust (FFA)

FFA is a method by which PWM resolution can be improved on 50% fixed duty cycle signals. Higher resolution is achieved by altering the PWM period by a single count for calculated intervals. This increased resolution is based upon the PWM frequency averaged over a large number of PWM periods. For example, if the period event time is increased by one psmc_clk period (TPSMC_CLK) every N events, then the effective resolution of the average event period is TPSMC_CLK/N.

When active, after every period event the FFA hardware adds the PSMCxFFA value with the previously accumulated result. Each time the addition causes an overflow, the period event time is increased by one. Refer to Figure 24-22.

FIGURE 24-22: FFA BLOCK DIAGRAM.



The FFA function is only available when using one of the two Fixed Duty Cycle modes of operation. In fixed duty cycle operation each PWM period is comprised of two period events. That is why the PWM periods in Table 24-3 example calculations are multiplied by two as opposed to the normal period calculations for normal mode operation.

The extra resolution gained by the FFA is based upon the number of bits in the FFA register and the psmc_clk frequency. The parameters of interest are:

- TPWM – this is the lower bound of the PWM period that will be adjusted
- TPWM+1 – this is the upper bound of the PWM period that will be adjusted. This is used to help determine the step size for each increment of the FFA register
- TRESOLUTION – each increment of the FFA register will add this amount of period to average PWM frequency

TABLE 24-3: FRACTIONAL FREQUENCY ADJUST CALCULATIONS

Parameter	Value
FPSMC_CLK	64 MHz
TPSMC_CLK	15.625 ns
PSMCxPR<15:0>	00FFh = 255
TPWM	= (PSMCxPR<15:0>+1)*2*TPSMC_CLK = 256*2*15.625ns = 8 us
FPWM	125 kHz
TPWM+1	= (PSMCxPR<15:0>+2)*2*TPSMC_CLK = 257*2*15.625ns = 8.03125 us
FPWM+1	= 124.513 kHz
TRESOLUTION	= (TPWM+1-TPWM)/$2^{FFA\text{-}Bits}$ = (8.03125us - 8.0 us)/16 = 0.03125us/16 ~ 1.95 ns
FRESOLUTION	(FPWM+1-FPWM)/$2^{FFA\text{-}Bits}$ ~ -30.4 Hz

REGISTER 24-3: PSMC1SYNC: PSMC1 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
P1POFST	P1PRPOL	P1DCPOL	—	—	—	P1SYNC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P1POFST:** PSMC1 Phase Offset Control bit
1 = sync_out source is phase event and latch set source is synchronous period event
0 = sync_out source is period event and latch set source is phase event

bit 6 **P1PRPOL:** PSMC1 Period Polarity Event Control bit
1 = Selected asynchronous period event inputs are inverted
0 = Selected asynchronous period event inputs are not inverted

bit 5 **P1DCPOL:** PSMC1 Duty-cycle Event Polarity Control bit
1 = Selected asynchronous duty-cycle event inputs are inverted
0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-2 **Unimplemented:** Read as '0'

bit 1-0 **P1SYNC<1:0>:** PSMC1 Period Synchronization Mode bits
11 = PSMC1 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
10 = PSMC1 is synchronized with the PSMC2 module (sync_in comes from PSMC2 sync_out)
01 = Reserved - Do not use
00 = PSMC1 is synchronized with period event

REGISTER 24-4: PSMC2SYNC: PSMC2 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
P2POFST	P2PRPOL	P2DCPOL	—	—	—	P2SYNC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P2POFST:** PSMC2 Phase Offset Control bit
1 = sync_out source is phase event and latch set source is synchronous period event
0 = sync_out source is period event and latch set source is phase event

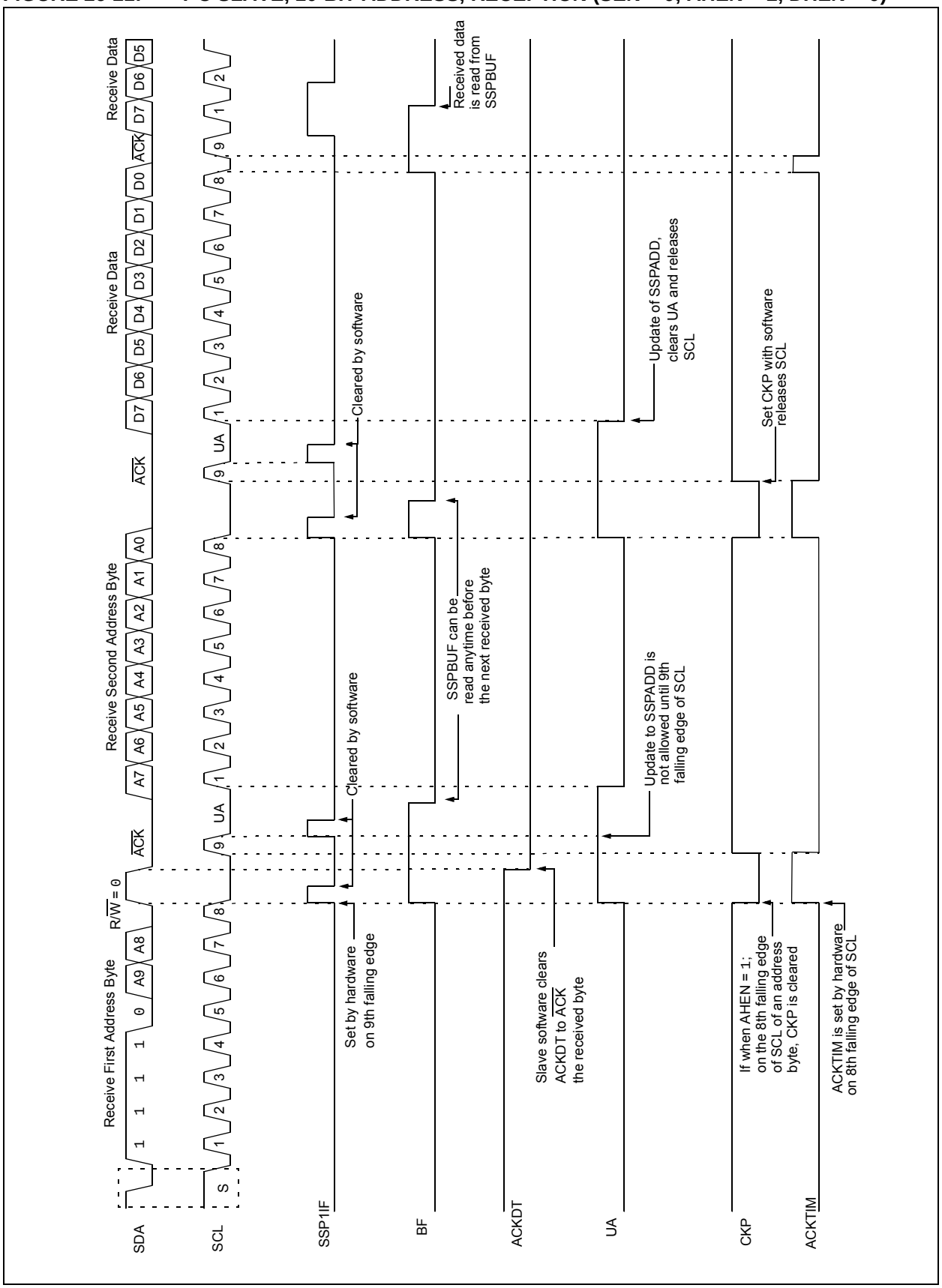
bit 6 **P2PRPOL:** PSMC2 Period Polarity Event Control bit
1 = Selected asynchronous period event inputs are inverted
0 = Selected asynchronous period event inputs are not inverted

bit 5 **P2DCPOL:** PSMC2 Duty-cycle Event Polarity Control bit
1 = Selected asynchronous duty-cycle event inputs are inverted
0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-2 **Unimplemented:** Read as '0'

bit 1-0 **P2SYNC<1:0>:** PSMC2 Period Synchronization Mode bits
11 = PSMC2 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
10 = Reserved – Do not use
01 = PSMC2 is synchronized with the PSMC1 module (sync_in comes from PSMC1 sync_out)
00 = PSMC2 is synchronized with period event

FIGURE 26-21: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)



26.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 26-29).

26.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

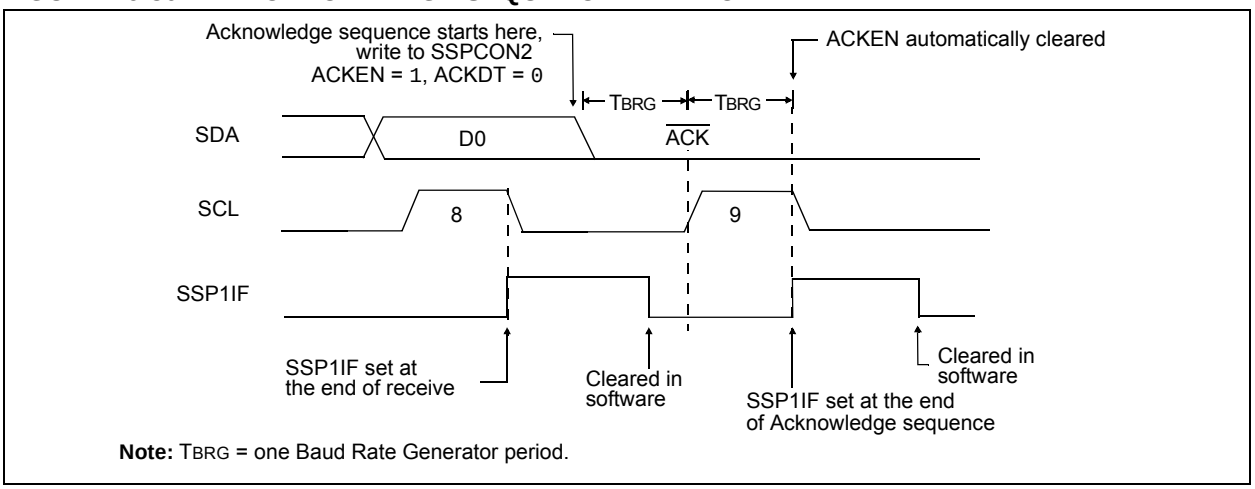
26.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 26-30).

26.6.9.1 WCOL Status Flag

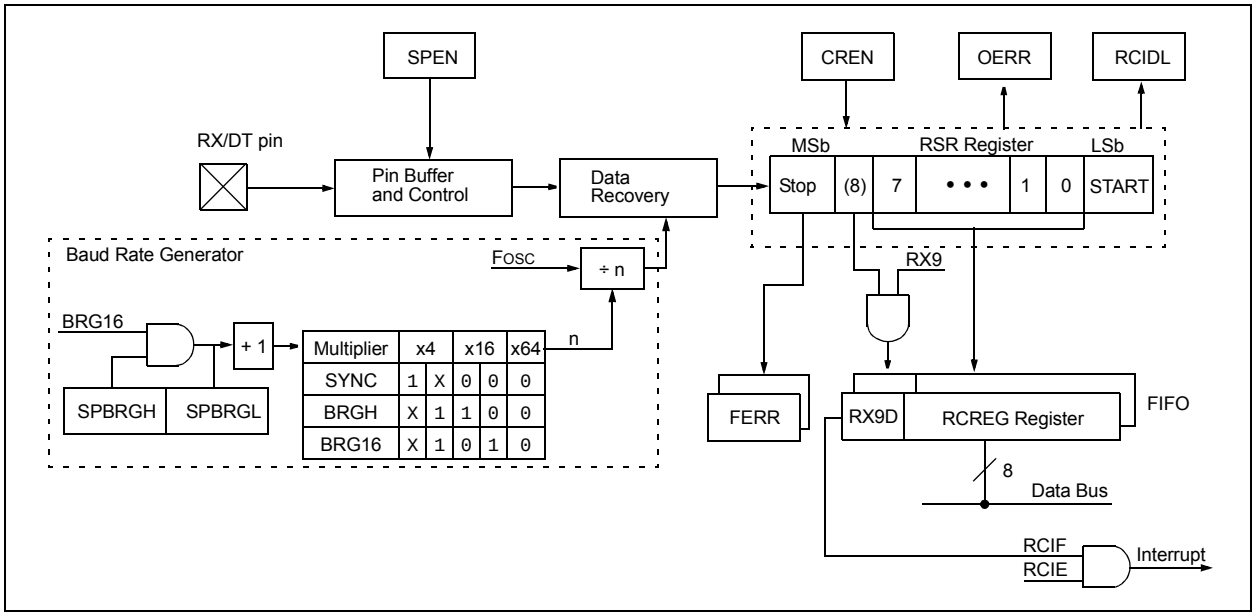
If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 26-30: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

FIGURE 27-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 27-1, Register 27-2 and Register 27-3, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.

TABLE 30-8: PLL CLOCK TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
F10	FOSC	Oscillator Frequency Range	4	—	8	MHz	
F11	FSYS	On-Chip VCO System Frequency	16	—	32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%	—	+0.25%	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 30-7: CLKOUT AND I/O TIMING

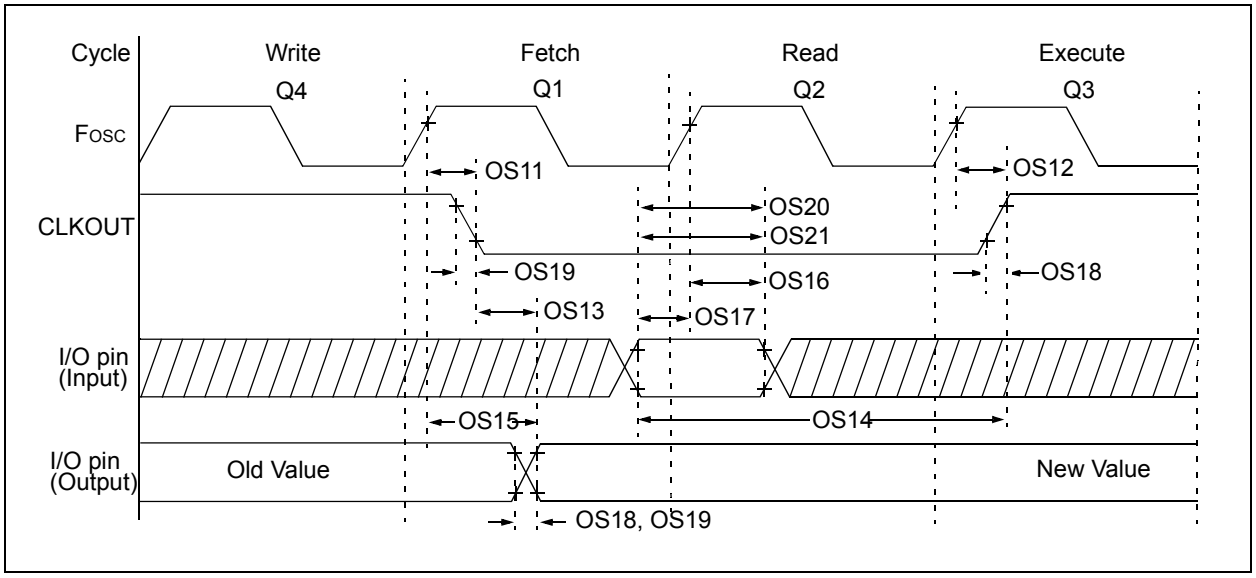
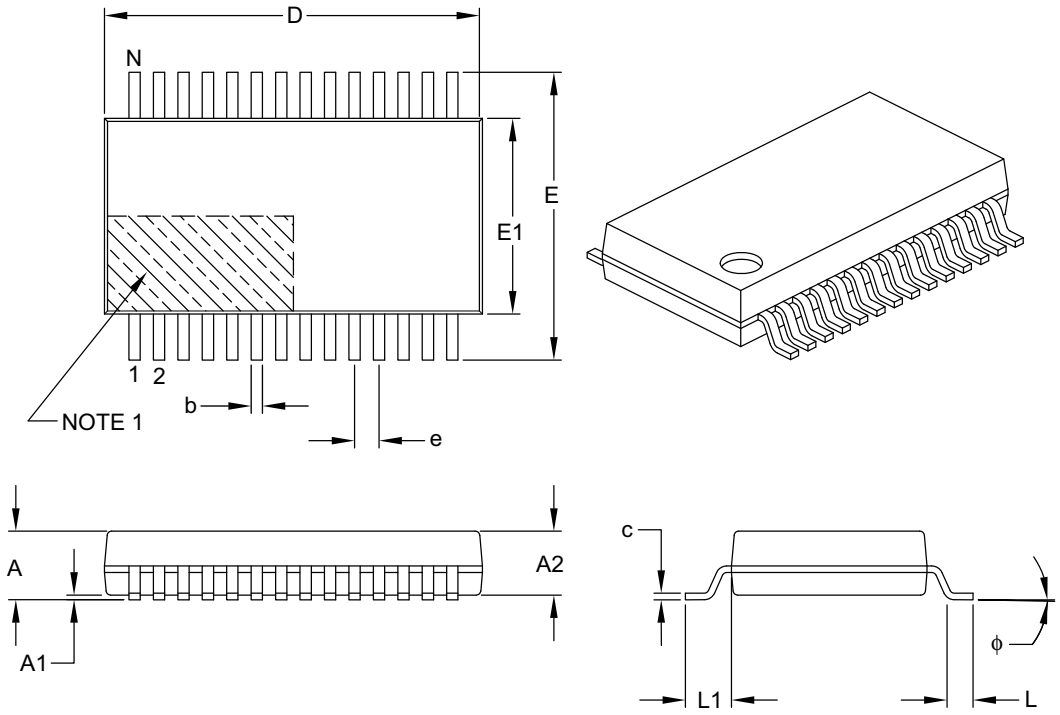


TABLE 30-19: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-hold before CK ↓ (DT hold time)	10	—	ns	
US126	TCKL2DTL	Data-hold after CK ↓ (DT hold time)	15	—	ns	

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B