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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1786-e-ss

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3.3.5 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-11 can be addressed from any Bank.

TABLE 3-11:	CORE FUNCTION REGISTERS SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets		
Bank 0-31													
x00h or x80h	INDF0	Addressing (not a phys	this location ical register)		xxxx xxxx	uuuu uuuu							
x01h or x81h	INDF1	Addressing (not a phys	this location ical register)		xxxx xxxx	uuuu uuuu							
x02h or x82h	PCL	Program C	ounter (PC)	Least Signifi	cant Byte					0000 0000	0000 0000		
x03h or x83h	STATUS	—	_		ТО	PD	Z	DC	С	1 1000	q quuu		
x04h or x84h	FSR0L	Indirect Da	ta Memory A		0000 0000	uuuu uuuu							
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer									0000 0000		
x06h or x86h	FSR1L	Indirect Da	ta Memory A	ddress 1 Lo	w Pointer					0000 0000	uuuu uuuu		
x07h or x87h	FSR1H	Indirect Da	ta Memory A	ddress 1 Hig	gh Pointer					0000 0000	0000 0000		
x08h or x88h	BSR	—	_		BSR4	BSR3	BSR2	BSR1	BSR0	0 0000	0 0000		
x09h or x89h	WREG	Working Re		0000 0000	uuuu uuuu								
x0Ahor x8Ah	PCLATH	Write Buffer for the upper 7 bits of the Program Counter									-000 0000		
x0Bhor x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000		

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

6.6 Register Definitions: Oscillator Control

REGISTER 6-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0	
SPLLEN		IRCF	<3:0>		_	SCS	<1:0>	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'		
u = Bit is unc	hanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all o	other Resets	
'1' = Bit is set	t	'0' = Bit is clea	ared					
bit 7	SPLLEN: So <u>If PLLEN in (</u> SPLLEN bit i <u>If PLLEN in (</u> 1 = 4x PLL I 0 = 4x PLL i	ftware PLL Ena <u>Configuration W</u> s ignored. 4x P <u>Configuration W</u> s enabled s disabled	able bit ′ <u>ords = 1:</u> LL is always e ′ <u>ords = 0:</u>	nabled (subject	t to oscillator re	equirements)		
bit 6-3 IRCF<3:0>: Internal Oscillator Frequency Select bits $1111 = 16 \text{ MHz HF or 32 MHz HF}^{(2)}$ $110 = 8 \text{ MHz or 32 MHz HF}^{(2)}$ 1101 = 4 MHz HF 100 = 2 MHz HF $1010 = 500 \text{ KHz HF}^{(1)}$ $1010 = 500 \text{ KHz HF}^{(1)}$ $1001 = 250 \text{ KHz HF}^{(1)}$ 0111 = 500 KHz MF (default upon Reset) 0110 = 250 KHz MF 0101 = 125 KHz MF 0101 = 125 KHz MF $0101 = 31.25 \text{ KHz MF}^{(1)}$ 0010 = 31.25 KHz MF								
bit 2 bit 1-0	Unimplemen SCS<1:0>: S 1x = Internal 01 = Timer1 00 = Clock d	nted: Read as ' System Clock S oscillator block oscillator etermined by F	0' elect bits SSC<2:0> in t	Configuration W	Vords.			
Note 1: Du	uplicate frequen	cy derived from	HFINTOSC.					

2: 32 MHz when SPLLEN bit is set. Refer to Section 6.2.2.6 "32 MHz Internal Oscillator Frequency Selection".

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0					
—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE					
bit 7					·		bit 0					
Legend:												
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'						
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets					
'1' = Bit is set		'0' = Bit is clea	ared									
bit 7	bit 7 Unimplemented: Read as '0'											
bit 6	PSMC3TIE: F	SMC3 Time B	ase Interrupt I	Enable bit								
	1 = Enables	PSMC3 time ba	ase generated	l interrupts								
	0 = Disables	PSMC3 time b	ase generated	d interrupts								
bit 5	PSMC2TIE: F	SMC2 Time B	ase Interrupt I	Enable bit								
	1 = Enables	PSMC2 time ba	ase generated	l interrupts								
hit 4			ase Interrunt F	Enable bit								
	1 = Enables	PSMC1 time b	ase generated	interrupts								
	0 = Disables	PSMC1 time b	ase generated	d interrupts								
bit 3	Unimplemen	ted: Read as '	0'									
bit 2	PSMC3SIE: F	PSMC3 Auto-S	hutdown Inter	rupt Enable bit	:							
	1 = Enables	PSMC3 auto-s	hutdown interr	rupts								
	0 = Disables	PSMC3 auto-s	hutdown inter	rupts								
bit 1	PSMC2SIE: F	PSMC2 Auto-S	hutdown Inter	rupt Enable bit	:							
	1 = Enables	PSMC2 auto-s	hutdown interr	rupts								
h # 0		PSMC2 auto-s		rupis wat Enchla hit								
DIT U		SINCT Auto-S	nutdown inter	rupt Enable bit								
	1 = Enables 0 = Disables	PSMC1 auto-si PSMC1 auto-si	hutdown inter	rupis								
	2.000/00											
Note: Bit	PEIE of the IN	TCON register	must be									
set	to enable any p	peripheral inter	rupt.									

REGISTER 8-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented						as '0'	
u = Bit is unchanged x = Bit is unknown			-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 13-25: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

bit 7-0 INLVLC<7:0>: PORTC Input Level Select bits

For RC<7:0> pins, respectively

1 = ST input used for PORT reads and interrupt-on-change

0 = TTL input used for PORT reads and interrupt-on-change

TABLE 13-0. SUMMANT OF REGISTERS ASSOCIATED WITH TORT	TABLE 13-8:	SUMMARY OF REGISTERS ASSOCIATED WITH PORTC
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Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	142
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	142
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	143
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	144
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	142
ODCONC	ODC7	ODC6	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	143
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	142
SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	143

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

REGISTER 13-31: ODCOND: PORTD OPEN DRAIN CONTROL REGIS	ſER
--	-----

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0						
ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0						
bit 7 bi													
Legend:													
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'									
u = Bit is unchanged x = Bit is unknown			-n/n = Value at POR and BOR/Value at all other Resets										

'1' = Bit is set	'0' = Bit is cleared

bit 7-0 ODD<7:0>: PORTD Open Drain Enable bits

For RD<7:0> pins, respectively

1 = Port pin operates as open-drain drive (sink current only)

0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 13-32: SLRCOND: PORTD SLEW RATE CONTROL REGISTER

| R/W-1/1 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SLRD7 | SLRD6 | SLRD5 | SLRD4 | SLRD3 | SLRD2 | SLRD1 | SLRD0 |
| bit 7 | | | • | | | • | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 SLRD<7:0>: PORTD Slew Rate Enable bits For RD<7:0> pins, respectively 1 = Port pin slew rate is limited 0 = Port pin slews at maximum rate

REGISTER 13-33: INLVLD: PORTD INPUT LEVEL CONTROL REGISTER

| R/W-1/1 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| INLVLD7 | INLVLD6 | INLVLD5 | INLVLD4 | INLVLD3 | INLVLD2 | INLVLD1 | INLVLD0 |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

INLVLD<7:0>: PORTD Input Level Select bits

For RD<7:0> pins, respectively

1 = ST input used for PORT reads and interrupt-on-change

0 = TTL input used for PORT reads and interrupt-on-change

20.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 20-1) contains Control and Status bits for the following:

- Enable
- Output selection
- Output polarity
- · Speed/Power selection
- · Hysteresis enable
- Output synchronization

The CMxCON1 register (see Register 20-2) contains Control bits for the following:

- Interrupt enable
- Interrupt edge polarity
- · Positive input channel selection
- · Negative input channel selection

20.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

20.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- · Corresponding TRIS bit must be cleared
- · CxON bit of the CMxCON0 register must be set

Note 1:	The CxOE bit of the CMxCON0 register
	overrides the PORT data latch. Setting
	the CxON bit of the CMxCON0 register
	has no impact on the port override.

2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

20.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 20-2 shows the output state versus input conditions, including polarity control.

TABLE 20-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

20.2.4 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

20.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See **Section 30.0 "Electrical Specifications"** for more information.

20.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 22.6 "Timer1 Gate"** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

20.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the CxSYNC bit of the CMx-CON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 20-2) and the Timer1 Block Diagram (Figure 22-1) for more information.

20.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- CxON, CxPOL and CxSP bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- CxINTP bit of the CMxCON1 register (for a rising edge detection)
- CxINTN bit of the CMxCON1 register (for a falling edge detection)
- · PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

20.6 Comparator Positive Input Selection

Configuring the CxPCH<2:0> bits of the CMxCON1 register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- Vss (Ground)

See Section 15.0 "Fixed Voltage Reference (FVR)" for more information on the Fixed Voltage Reference module.

See Section 19.0 "Digital-to-Analog Converter (DAC) Module" for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.

Note: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit of the CMxCON0 register, or by switching the comparator on or off with the CxON bit of the CMxCON0 register.

20.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10 \text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

- Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
 - 2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

20.10.1 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 "Alternate Pin Function**" for more information.



FIGURE 20-4: ANALOG INPUT MODEL

24.1 Fundamental Operation

PSMC operation is based on the sequence of three events:

- Period Event Determines the frequency of the active signal.
- Rising Edge Event Determines start of the active pulse. This is also referred to as the phase.
- Falling Edge Event Determines the end of the active pulse. This is also referred to as the duty cycle.





Each of the three types of events is triggered by a user selectable combination of synchronous timed and asynchronous external inputs.

Asynchronous event inputs may come directly from an input pin or through the comparators.

Synchronous timed events are determined from the PSMCxTMR counter, which is derived from internal clock sources. See Section 24.2.5 "PSMC Time Base Clock Sources" for more detail.

The active pulse stream can be further modulated by one of several internal or external sources:

- · Register control bit
- Comparator output
- · CCP output
- Input pin

User selectable deadtime can be inserted in the drive outputs to prevent shoot through of configurations with two devices connected in series between the supply rails.

Applications requiring very small frequency granularity control when the PWM frequency is large can do so with the fractional frequency control available in the variable frequency fixed Duty Cycle modes. PSMC operation can be quickly terminated without software intervention by the auto-shutdown control. Auto-shutdown can be triggered by any combination of the following:

- PSMCxIN pin
- sync_C1OUT
- sync C2OUT
- sync_C3OUT
- sync_C4OUT

The basic waveform generated from these events is shown in Figure 24-2.

FFA number	Output Frequency (kHz)	Step Size (Hz)
0	125.000	0
1	124.970	-30.4
2	124.939	-60.8
3	124.909	-91.2
4	124.878	-121.6
5	124.848	-152.0
6	124.818	-182.4
7	124.787	-212.8
8	124.757	-243.2
9	124.726	-273.6
10	124.696	-304.0
11	124.666	-334.4
12	124.635	-364.8
13	124.605	-395.2
14	124.574	-425.6
15	124.544	-456.0

TABLE 24-4: SAMPLE FFA OUTPUT PERIODS/FREQUENCIES

REGISTER 24-3: PSMC1SYNC: PSMC1 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
P1POFST	P1PRPOL	P1DCPOL	_	—	_	P1SYN	C<1:0>
bit 7				•			bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
u = Bit is unchan	ged	x = Bit is unknow	vn	-n/n = Value at	POR and BOR/Val	ue at all other Re	esets
'1' = Bit is set		'0' = Bit is cleare	d				
bit 7 bit 6 bit 5	P1POFST: PSM 1 = sync_out 0 = sync_out P1PRPOL: PSM 1 = Selected 0 = Selected P1DCPOL: PSM	IC1 Phase Offset source is phase e source is period e //C1 Period Polari asynchronous pe asynchronous pe //C1 Duty-cycle E	Control bit event and latch sevent and latch ty Event Contro riod event inputs riod event inputs vent Polarity Co	set source is syn set source is pha I bit s are inverted s are not inverted ontrol bit	chronous period ev ise event	vent	
	0 = Selected	asynchronous du	ty-cycle event in	iputs are not inve	erted		
bit 4-2	Unimplemente	d: Read as '0'					
bit 1-0	P1SYNC<1:0>: 11 = PSMC1 10 = PSMC1 01 = Reserve 00 = PSMC1	PSMC1 Period S is synchronized v is synchronized v ed - Do not use is synchronized v	ynchronization vith the PSMC3 vith the PSMC2 vith period even	Mode bits module (sync_ir module (sync_ir	a comes from PSM a comes from PSM	C3 sync_out) C2 sync_out)	

REGISTER 24-4: PSMC2SYNC: PSMC2 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
P2POFST	P2PRPOL	P2DCPOL	—	—	—	P2SYNC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	 P2POFST: PSMC2 Phase Offset Control bit 1 = sync_out source is phase event and latch set source is synchronous period event 0 = sync_out source is period event and latch set source is phase event
bit 6	 P2PRPOL: PSMC2 Period Polarity Event Control bit 1 = Selected asynchronous period event inputs are inverted 0 = Selected asynchronous period event inputs are not inverted
bit 5	 P2DCPOL: PSMC2 Duty-cycle Event Polarity Control bit 1 = Selected asynchronous duty-cycle event inputs are inverted 0 = Selected asynchronous duty-cycle event inputs are not inverted
bit 4-2	Unimplemented: Read as '0'
bit 1-0	P2SYNC<1:0>: PSMC2 Period Synchronization Mode bits 11 = PSMC2 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out) 10 = Reserved – Do not use 01 = PSMC2 is synchronized with the PSMC1 module (sync_in comes from PSMC1 sync_out) 00 = PSMC2 is synchronized with period event

REGISTER 24-18: PSMCxTMRL: PSMC TIME BASE COUNTER LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
	PSMCxTMRL<7:0>								
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'			
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets		
'1' = Bit is set		'0' = Bit is clea	ared						

bit 7-0 **PSMCxTMRL<7:0>:** 16-bit PSMCx Time Base Counter Least Significant bits = PSMCxTMR<7:0>

REGISTER 24-19: PSMCxTMRH: PSMC TIME BASE COUNTER HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	
			PSMCxT	MRH<7:0>				
bit 7							bit 0	
Legend:								
R = Readable	Readable bit W = Writable bit U = Unimplemented bit, read a				as '0'			
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value at POR and BOR/Value at all other Resets				

bit 7-0 PSMCxTMRH<7:0>: 16-bit PSMCx Time Base Counter Most Significant bits

'0' = Bit is cleared

= PSMCxTMR<15:8>

'1' = Bit is set

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The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 25-4).

25.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 25-4.

EQUATION 25-4: PWM RESOLUTION

Resolution =
$$\frac{\log[4(PR2 + 1)]}{\log(2)}$$
 bits

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 25-1:	EXAMPLE PWM FREQUENCIES AND RESOLUTIONS ((Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 25-2:	EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 M	Hz)
-------------	---	-----

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

27.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive
	FIFO have framing errors, repeated reads
	of the RCREG will not clear the FERR bit.

27.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

27.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9 bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

27.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

(Configuration Bi	ts		Poud Poto Formula
SYNC	BRG16	BRGH	BRG/EUSART Mode	Bauu Kale Forniula
0	0	0	8-bit/Asynchronous	Fosc/[64 (n+1)]
0	0	1	8-bit/Asynchronous	
0	1	0	16-bit/Asynchronous	FOSC/[16 (n+1)]
0	1	1	16-bit/Asynchronous	
1	0	x	8-bit/Synchronous	Fosc/[4 (n+1)]
1	1	x	16-bit/Synchronous	

TABLE 27-3: BAUD RATE FORMULAS

Legend: x = Don't care, n = value of SPBRGH, SPBRGL register pair

TABLE 27-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN	347
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	346
SPBRGL		BRG<7:0>							
SPBRGH	BRG<15:8>							348	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	345

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for the Baud Rate Generator.

* Page provides register information.

27.5.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

27.5.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see **Section 27.5.1.3 "Synchronous Master Transmission")**, except in the case of the Sleep mode. If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- 1. The first character will immediately transfer to the TSR register and transmit.
- 2. The second word will remain in TXREG register.
- 3. The TXIF bit will not be set.
- After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
- 5. If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.
- 27.5.2.2 Synchronous Slave Transmission Set-up:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the ANSEL bit for the CK pin (if applicable).
- 3. Clear the CREN and SREN bits.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit transmission is desired, set the TX9 bit.
- 6. Enable transmission by setting the TXEN bit.
- 7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
- 8. Start transmission by writing the Least Significant eight bits to the TXREG register.

TABLE 27-9: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	127
BAUDCON	ABDOVF	RCIDL	-	SCKP	BRG16	-	WUE	ABDEN	347
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	346
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
TXREG	EUSART Transmit Data Register							337*	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	345

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous slave transmission.

Page provides register information.

30.5 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS

2. TppS

Т				
F	Frequency	Т	Time	
Lowerd	case letters (pp) and their meanings:			
рр				
сс	CCP1	osc	OSC1	
ck	CLKOUT	rd	RD	
CS	CS	rw	RD or WR	
di	SDI	SC	SCK	
do	SDO	SS	SS	
dt	Data in	tO	T0CKI	
io	I/O PORT	t1	T1CKI	
mc	MCLR	wr	WR	
Upperc	case letters and their meanings:			
S				
F	Fall	P	Period	
Н	High	R	Rise	
I	Invalid (High-impedance)	V	Valid	
L	Low	Z	High-impedance	

FIGURE 30-4: LOAD CONDITIONS



PIC16(L)F1784/6/7

Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 31-97: ADC 12-bit Mode, Single-Ended DNL, VDD = 5.5V, VREF = 5.5V.



FIGURE 31-98: ADC 12-bit Mode, Single-Ended INL, VDD = 5.5V, VREF = 5.5V.



FIGURE 31-99: Temp. Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1784/6/7 Only.



FIGURE 31-100: Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1784/6/7 Only.



FIGURE 31-101: Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1784/6/7 Only.



FIGURE 31-102: Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 5.5V, PIC16F1784/6/7 Only.

PIC16(L)F1784/6/7

Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 31-120: Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values at 25°C, PIC16F1784/6/7 Only.



FIGURE 31-122: Comparator Response Time Over Voltage, NP Mode (CxSP = 1), Typical Measured Values, PIC16LF1784/6/7 Only.

FIGURE 31-124: Comparator Output Filter Delay Time Over Temp., NP Mode (CxSP = 1), Typical Measured Values, PIC16LF1784/6/7 Only.

FIGURE 31-121: Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values From -40°C to 125°C, PIC16F1784/6/7 Only.

FIGURE 31-123: Comparator Response Time Over Voltage, NP Mode (CxSP = 1), Typical Measured Values, PIC16F1784/6/7 Only.

FIGURE 31-125: Comparator Output Filter Delay Time Over Temp., NP Mode (CxSP = 1), Typical Measured Values, PIC16F1784/6/7 Only.

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Ν		S	
Dimensior	MIN	NOM	MAX	
Contact Pitch		0.40 BSC		
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B