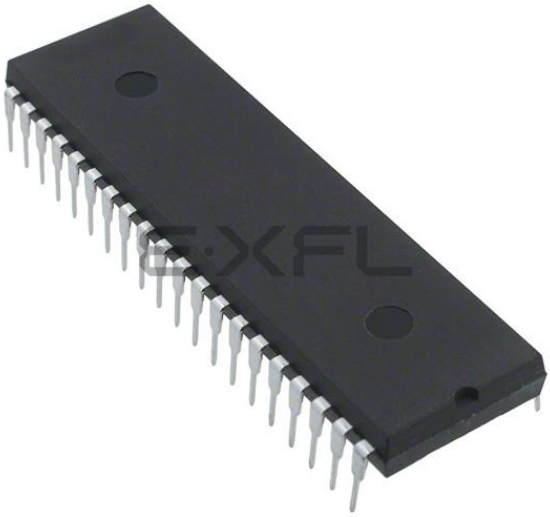

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1787-e-p

TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1784/7) (Continued)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Op Amps	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RC1	16	31	35	35	—	—	—	—	—	T1OSI	PSMC1B	CCP2	—	—	IOC	Y	—
RC2	17	32	36	36	—	—	—	—	—	—	PSMC1C	CCP1	—	—	IOC	Y	
RC3	18	33	37	37	—	—	—	—	—	—	PSMC1D	—	—	SCL SCK	IOC	Y	—
RC4	23	38	42	42	—	—	—	—	—	—	PSMC1E	—	—	SDI SDA	IOC	Y	—
RC5	24	39	43	43	—	—	—	—	—	—	PSMC1F	—	—	SDO	IOC	Y	—
RC6	25	40	44	44	—	—	—	—	—	—	PSMC2A	—	TX CK	—	IOC	Y	—
RC7	26	1	1	1	—	—	—	—	—	—	PSMC2B	—	RX DT	—	IOC	Y	—
RD0	19	34	38	38	—	—	—	OPA3IN+	—	—	—	—	—	—	—	Y	—
RD1	20	35	39	39	AN21	—	C1IN4- C2IN4- C3IN4- C4IN4-	OPA3OUT	—	—	—	—	—	—	—	Y	—
RD2	21	36	40	40	—	—	—	OPA3IN-	—	—	—	—	—	—	—	Y	—
RD3	22	37	41	41	—	—	—	—	—	—	—	—	—	—	—	Y	
RD4	27	2	2	2	—	—	—	—	—	—	PSMC3F	—	—	—	—	Y	—
RD5	28	3	3	3	—	—	—	—	—	—	PSMC3E	—	—	—	—	Y	—
RD6	29	4	4	4	—	—	C3OUT	—	—	—	PSMC3D	—	—	—	—	Y	—
RD7	30	5	5	5	—	—	C4OUT	—	—	—	PSMC3C	—	—	—	—	Y	—
RE0	8	23	25	25	AN5	—	—	—	—	—	—	CCP3	—	—	—	Y	—
RE1	9	24	26	26	AN6	—	—	—	—	—	PSMC3B	—	—	—	—	Y	—
RE2	10	25	27	27	AN7	—	—	—	—	—	PSMC3A	—	—	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$ V_{PP}
V_{DD}	11,32	7,26	7,28	7,8, 28	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
Vss	12,31	6,27	6,29	6,30,	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

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3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 11-15											
x0Ch or x8Ch to x6Fh or xEFh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits

111 = ECH: External Clock, High-Power mode (4-20 MHz): device clock supplied to CLKIN pin
110 = ECM: External Clock, Medium-Power mode (0.5-4 MHz): device clock supplied to CLKIN pin
101 = ECL: External Clock, Low-Power mode (0-0.5 MHz): device clock supplied to CLKIN pin
100 = INTOSC oscillator: I/O function on CLKIN pin
011 = EXTRC oscillator: External RC circuit connected to CLKIN pin
010 = HS oscillator: High-speed crystal/resonator connected between OSC1 and OSC2 pins
001 = XT oscillator: Crystal/resonator connected between OSC1 and OSC2 pins
000 = LP oscillator: Low-power crystal connected between OSC1 and OSC2 pins

Note 1: The entire data EEPROM will be erased when the code protection is turned off during an erase.Once the Data Code Protection bit is enabled, ($\overline{CPD}$ = 0), the Bulk Erase Program Memory Command (through ICSP) can disable the Data Code Protection ($\overline{CPD}$ =1). When a Bulk Erase Program Memory Command is executed, the entire Program Flash Memory, Data EEPROM and configuration memory will be erased.

FIGURE 5-3: RESET START-UP SEQUENCE

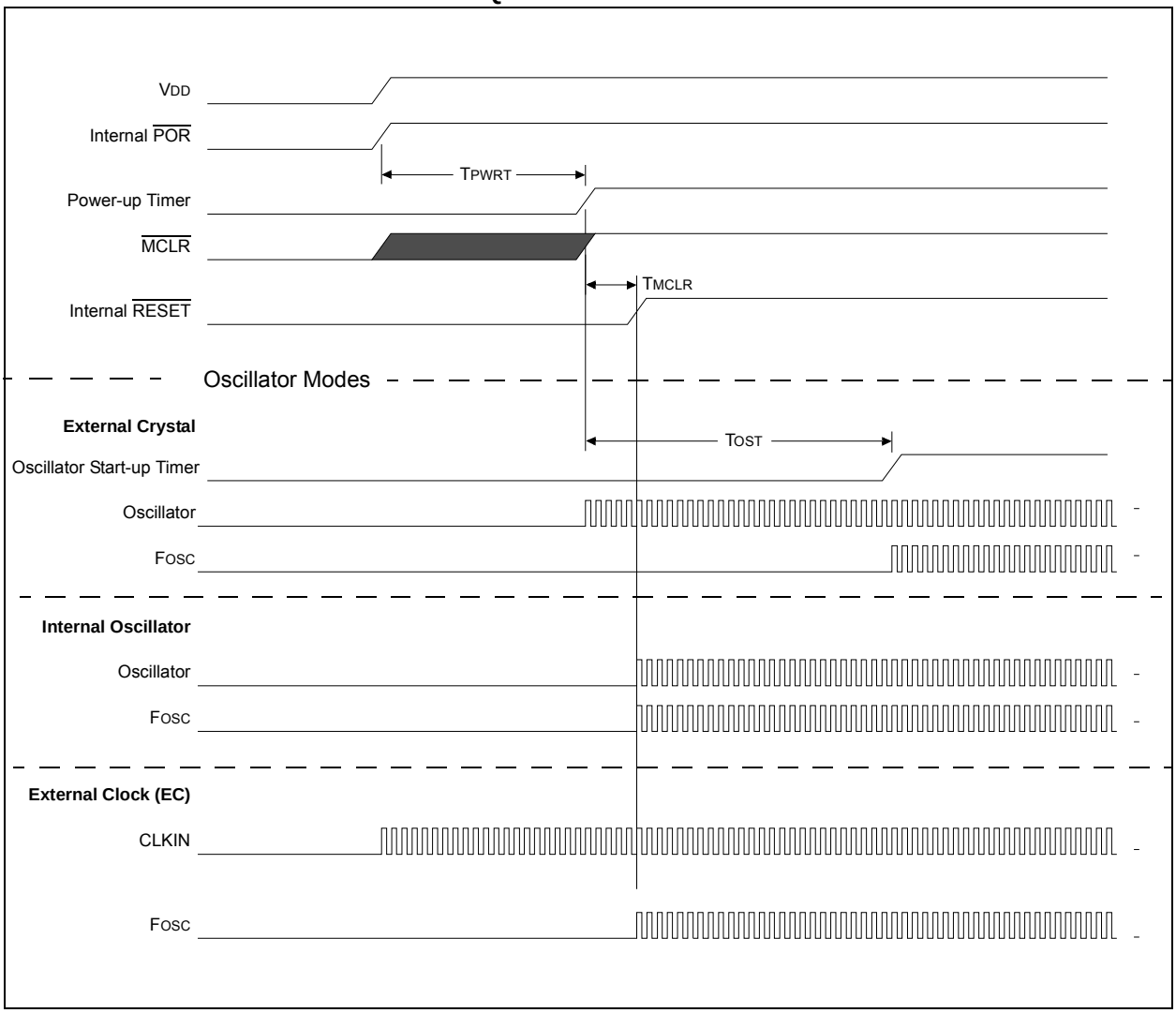

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			198
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	95
PIE3	—	—	—	CCP3IE	—	—	—	—	96
PIE4	—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE	97
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	99
PIR3	—	—	—	CCP3IF	—	—	—	—	100
PIR4	—	PSMC3TIF	PSMC2TIF	PSMC1TIF	—	PSMC3SIF	PSMC2SIF	PSMC1SIF	101

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

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24.3.2 COMPLEMENTARY PWM

The complementary PWM uses the same events as the single PWM, but two waveforms are generated instead of only one.

The two waveforms are opposite in polarity to each other. The two waveforms may also have dead-band control as well.

24.3.2.1 Mode Features and Controls

- Dead-band control available
- PWM primary output can be steered to the following pins:
  - PSMCxA
  - PSMCxC
  - PSMCxE
- PWM complementary output can be steered to the following pins:
  - PSMCxB
  - PSMCxD
  - PSMCxE

24.3.2.2 Waveform Generation

Rising Edge Event

- Complementary output is set inactive
- Optional rising edge dead band is activated
- Primary output is set active

Falling Edge Event

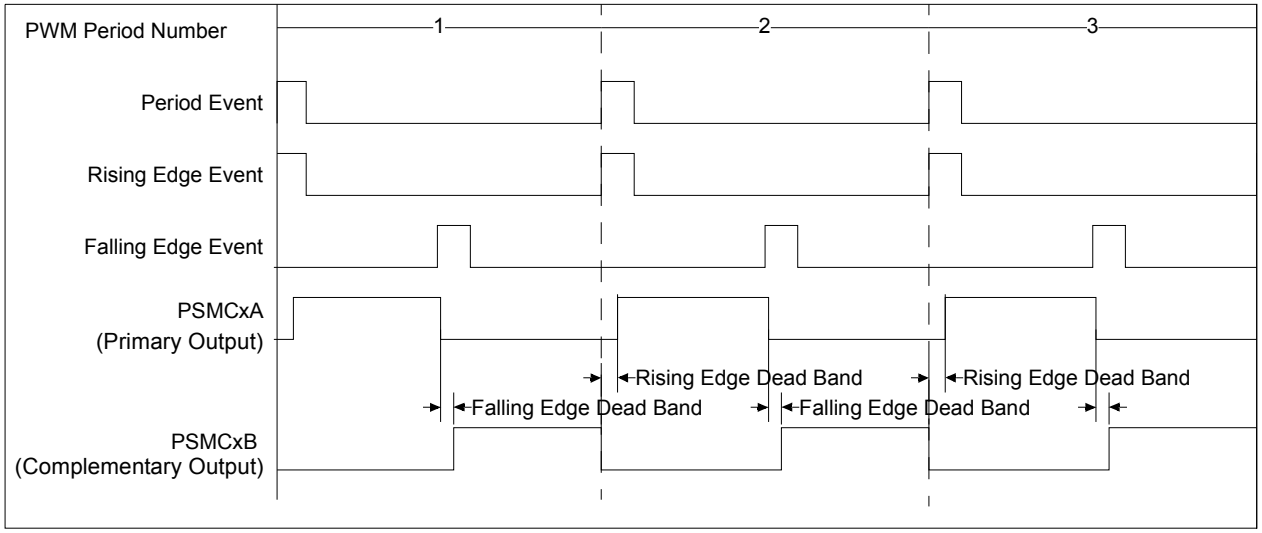
- Primary output is set inactive
- Optional falling edge dead band is activated
- Complementary output is set active

Code for setting up the PSMC generate the complementary single-phase waveform shown in Figure 24-5, and given in Example 24-2.

EXAMPLE 24-2: COMPLEMENTARY SINGLE-PHASE SETUP

```
; Complementary Single-phase PWM PSMC setup
; Fully synchronous operation
; Period = 10 us
; Duty cycle = 50%
; Deadband = 93.75 +15.6/-0 ns
   BANKSEL PSMC1CON
   MOVLW   0x02       ; set period
   MOVWF   PSMC1PRH
   MOVLW   0x7F
   MOVWF   PSMC1PRL
   MOVLW   0x01       ; set duty cycle
   MOVWF   PSMC1DCH
   MOVLW   0x3F
   MOVWF   PSMC1DCL
   CLRF    PSMC1PHH   ; no phase offset
   CLRF    PSMC1PHL
   MOVLW   0x01       ; PSMC clock=64 MHz
   MOVWF   PSMC1CLK
; output on A, normal polarity
   MOVLW   B'00000011'; A and B enables
   MOVWF   PSMC1OEN
   MOVWF   PSMC1STR0
   CLRF    PSMC1POL
; set time base as source for all events
   BSF     PSMC1PRS, P1PRST
   BSF     PSMC1PHS, P1PHST
   BSF     PSMC1DCS, P1DCST
; set rising and falling dead-band times
   MOVLW   D'6'
   MOVWF   PSMC1DBR
   MOVWF   PSMC1DBF
; enable PSMC in Complementary Single Mode
; this also loads steering and time buffers
; and enables rising and falling deadbands
   MOVLW   B'11110001'
   MOVWF   PSMC1CON
   BANKSEL TRISC
   BCF     TRISC, 0   ; enable pin drivers
   BCF     TRISC, 1
```

FIGURE 24-5: COMPLEMENTARY PWM WAVEFORM – PSMCXSTR0 = 03H



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24.3.7 PULSE-SKIPPING PWM

The pulse-skipping PWM is used to generate a series of fixed-length pulses that can be triggered at each period event. A rising edge event will be generated when any enabled asynchronous rising edge input is active when the period event occurs, otherwise no event will be generated.

The rising edge event occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

24.3.7.1 Mode Features

- No dead-band control available
- No steering control available
- PWM is output to only one pin:
  - PSMCxA

24.3.7.2 Waveform Generation

Rising Edge Event

If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:

- PSMCxA is set active

Falling Edge Event

- PSMCxA is set inactive

Note:	To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 24-10: PULSE-SKIPPING PWM WAVEFORM

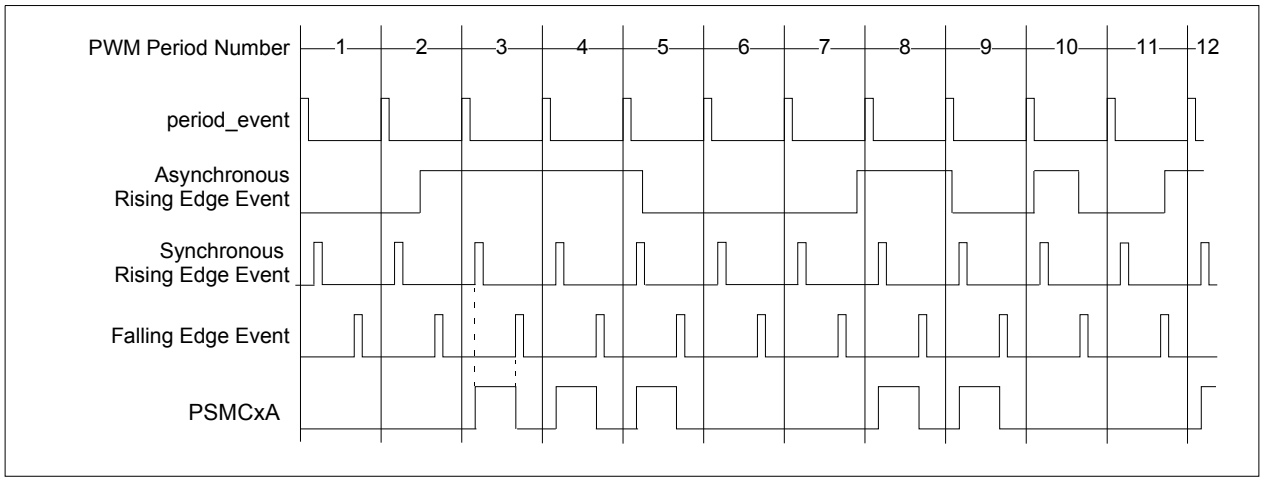
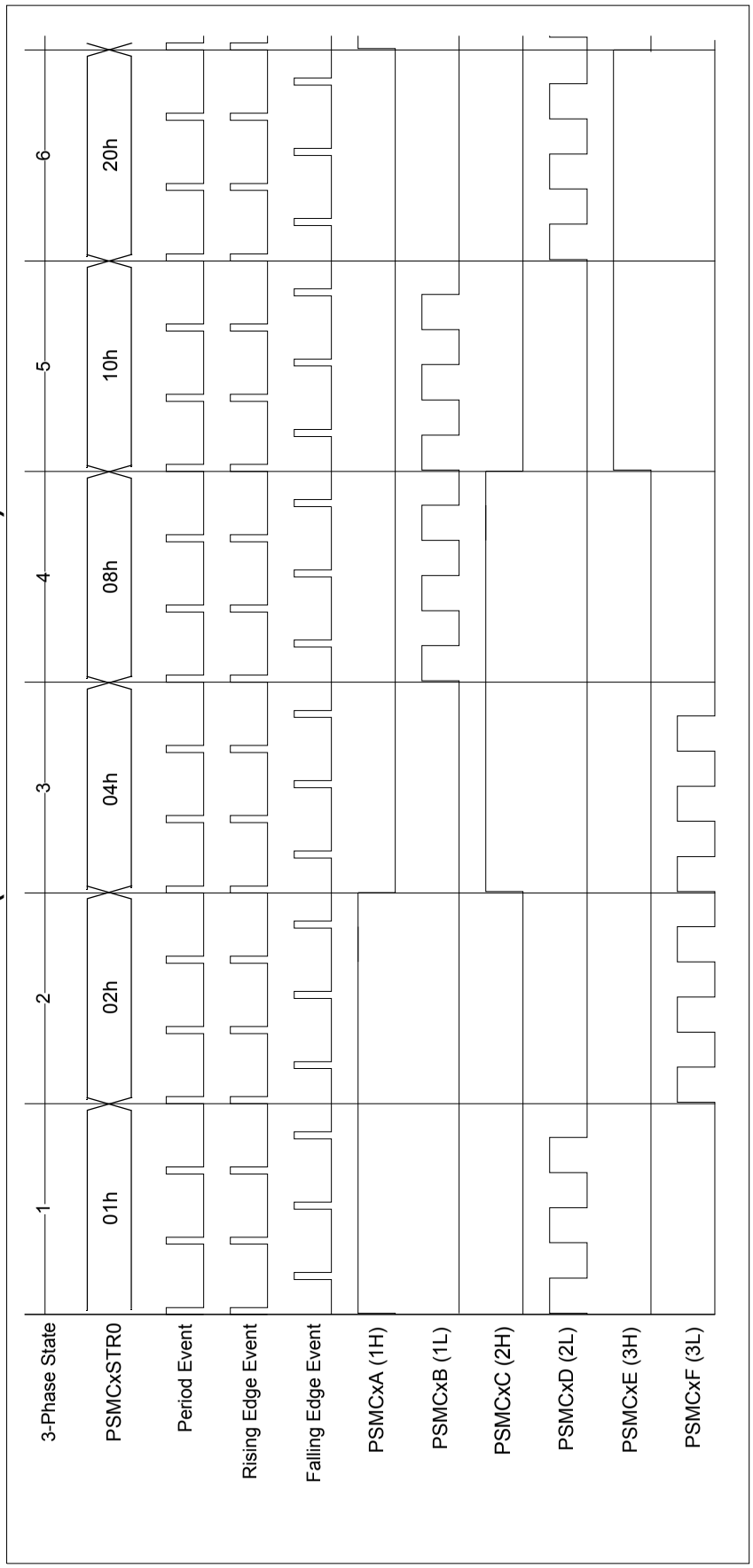


FIGURE 24-15: 3-PHASE PWM STEERING WAVEFORM (PXHSMEN = 0 AND PXLSMEN = 1)



REGISTER 24-12: PSMCxPHS: PSMC PHASE SOURCE REGISTER(1)

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxPHSIN	—	—	PxPHSC4	PxPHSC3	PxPHSC2	PxPHSC1	PxPHST
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxPHSIN:** PSMCx Rising Edge Event occurs on PSMCxIN pin
1 = Rising edge event will occur when PSMCxIN pin goes true
0 = PSMCxIN pin will not cause rising edge event

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxPHSC4:** PSMCx Rising Edge Event occurs on sync_C4OUT output
1 = Rising edge event will occur when sync_C4OUT output goes true
0 = sync_C4OUT will not cause rising edge event

bit 3 **PxPHSC3:** PSMCx Rising Edge Event occurs on sync_C3OUT output
1 = Rising edge event will occur when sync_C3OUT output goes true
0 = sync_C3OUT will not cause rising edge event

bit 2 **PxPHSC2:** PSMCx Rising Edge Event occurs on sync_C2OUT output
1 = Rising edge event will occur when sync_C2OUT output goes true
0 = sync_C2OUT will not cause rising edge event

bit 1 **PxPHSC1:** PSMCx Rising Edge Event occurs on sync_C1OUT output
1 = Rising edge event will occur when sync_C1OUT output goes true
0 = sync_C1OUT will not cause rising edge event

bit 0 **PxPHST:** PSMCx Rising Edge Event occurs on Time Base match
1 = Rising edge event will occur when PSMCxTMR = PSMCxPH
0 = Time base will not cause rising edge event

Note 1: Sources are not mutually exclusive: more than one source can cause a rising edge event.

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The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 25-4).

25.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 25-4.

EQUATION 25-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)} \ bits$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 25-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 25-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

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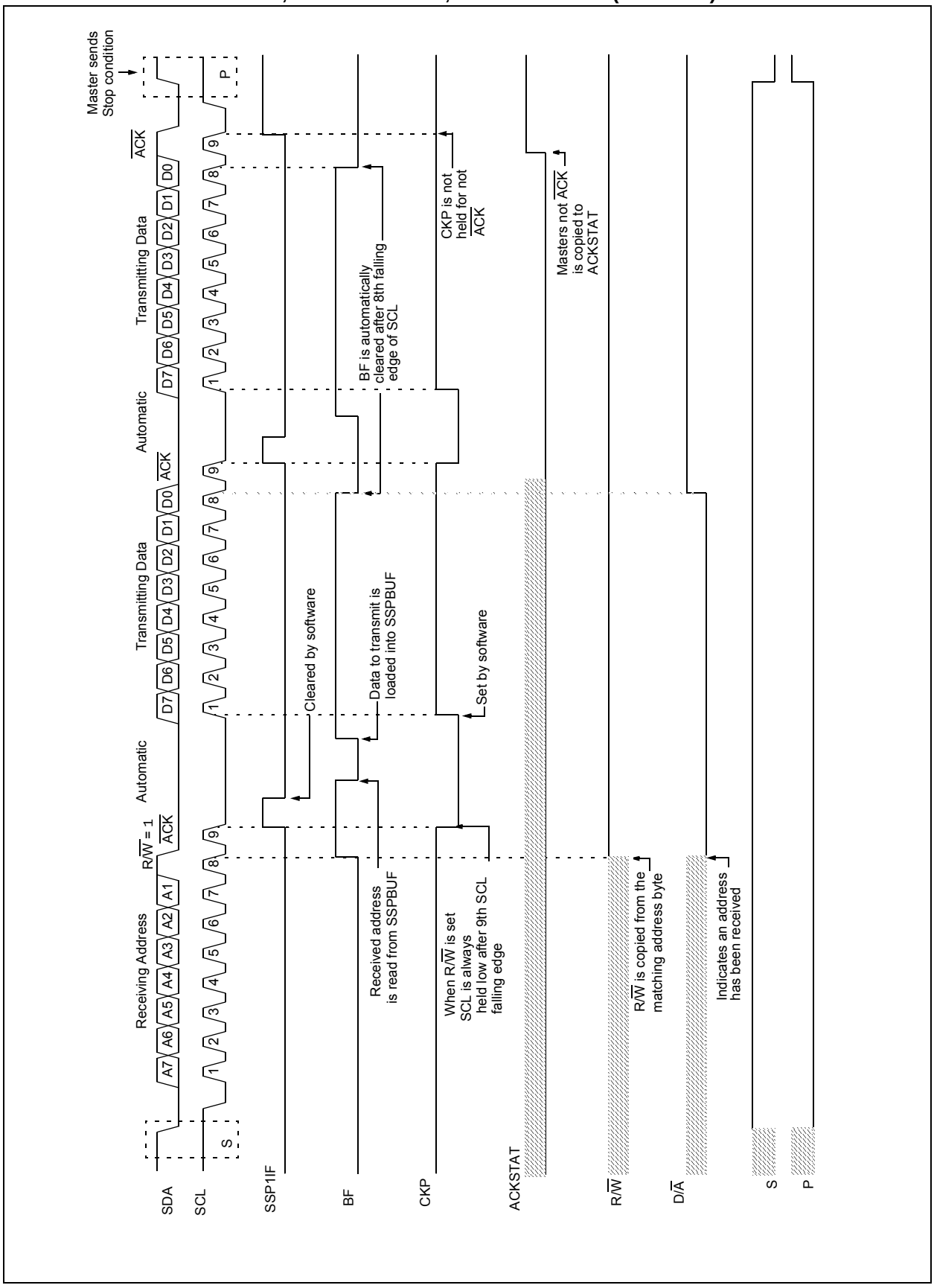
FIGURE 26-18: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)



REGISTER 26-2: SSPCON1: SSP CONTROL REGISTER 1

R/C/HS-0/0	R/C/HS-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets	
'1' = Bit is set	'0' = Bit is cleared	HS = Bit is set by hardware	C = User cleared

bit 7 **WCOL:** Write Collision Detect bit
Master mode:
1 = A write to the SSPBUF register was attempted while the I²C conditions were not valid for a transmission to be started
0 = No collision
Slave mode:
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit(1)
In SPI mode:
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register (must be cleared in software).
0 = No overflow
In I²C mode:
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode (must be cleared in software).
0 = No overflow

bit 5 **SSPEN:** Synchronous Serial Port Enable bit
In both modes, when enabled, these pins must be properly configured as input or output
In SPI mode:
1 = Enables serial port and configures SCK, SDO, SDI and $\overline{SS}$ as the source of the serial port pins(2)
0 = Disables serial port and configures these pins as I/O port pins
In I²C mode:
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins(3)
0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** Clock Polarity Select bit
In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
In I²C Slave mode:
SCL release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
In I²C Master mode:
Unused in this mode

bit 3-0 **SSPM<3:0>:** Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = FOSC/4
0001 = SPI Master mode, clock = FOSC/16
0010 = SPI Master mode, clock = FOSC/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled
0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0110 = I²C Slave mode, 7-bit address
0111 = I²C Slave mode, 10-bit address
1000 = I²C Master mode, clock = FOSC / (4 * (SSPADD+1))(4)
1001 = Reserved
1010 = SPI Master mode, clock = FOSC/(4 * (SSPADD+1))(5)
1011 = I²C firmware controlled Master mode (Slave idle)
1100 = Reserved
1101 = Reserved
1110 = I²C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1111 = I²C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
2: When enabled, these pins must be properly configured as input or output.
3: When enabled, the SDA and SCL pins must be configured as inputs.
4: SSPADD values of 0, 1 or 2 are not supported for I²C mode.
5: SSPADD value of '0' is not supported. Use SSPM = 0000 instead.

REGISTER 26-5: SSPMSK: SSP MASK REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
MSK<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-1 **MSK<7:1>:** Mask bits
1 = The received address bit n is compared to SSPADD<n> to detect I^2C address match
0 = The received address bit n is not used to detect I^2C address match

bit 0 **MSK<0>:** Mask bit for I^2C Slave mode, 10-bit Address
I^2C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):
1 = The received address bit 0 is compared to SSPADD<0> to detect I^2C address match
0 = The received address bit 0 is not used to detect I^2C address match
I^2C Slave mode, 7-bit address, the bit is ignored

REGISTER 26-6: SSPADD: MSSP ADDRESS AND BAUD RATE REGISTER (I^2C MODE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ADD<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

Master mode:

bit 7-0 **ADD<7:0>:** Baud Rate Clock Divider bits
SCL pin clock period = ((ADD<7:0> + 1) *4)/FOSC

10-Bit Slave mode — Most Significant Address Byte:

bit 7-3 **Not used:** Unused for Most Significant Address byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by I^2C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.

bit 2-1 **ADD<2:1>:** Two Most Significant bits of 10-bit address

bit 0 **Not used:** Unused in this mode. Bit state is a "don't care".

10-Bit Slave mode — Least Significant Address Byte:

bit 7-0 **ADD<7:0>:** Eight Least Significant bits of 10-bit address

7-Bit Slave mode:

bit 7-1 **ADD<7:1>:** 7-bit address

bit 0 **Not used:** Unused in this mode. Bit state is a "don't care".

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27.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

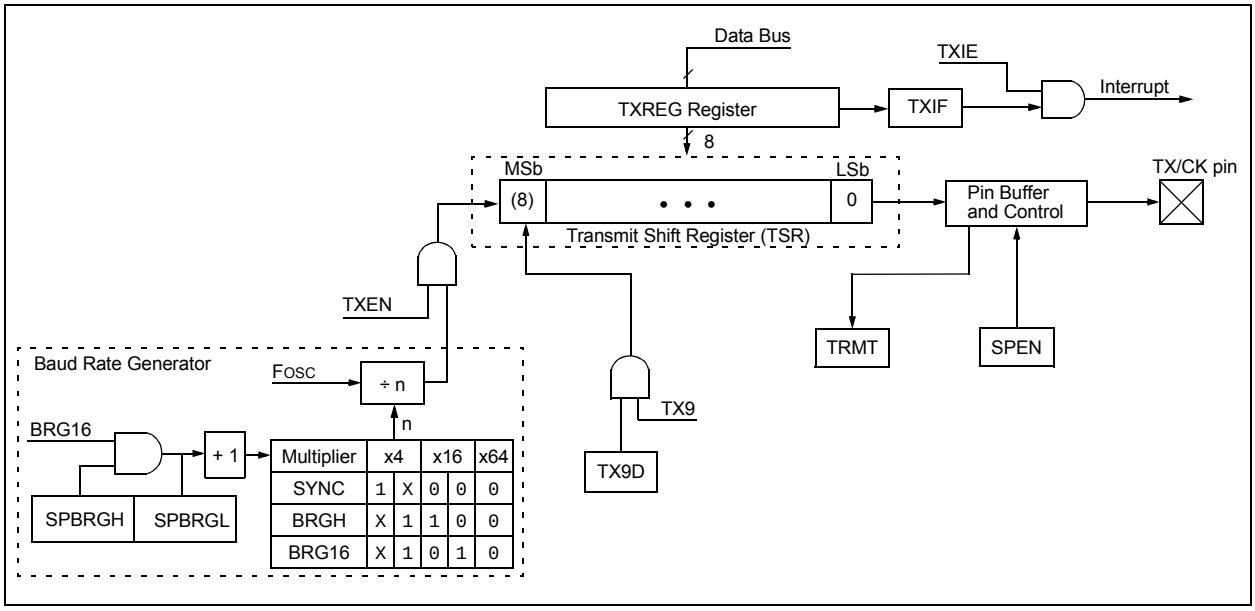
- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 27-1 and Figure 27-2.

FIGURE 27-1: EUSART TRANSMIT BLOCK DIAGRAM



MOVWI	Move W to INDFn
Syntax:	[*label*] MOVWI ++FSRn [*label*] MOVWI --FSRn [*label*] MOVWI FSRn++ [*label*] MOVWI FSRn-- [*label*] MOVWI k[FSRn]
Operands:	$n \in [0,1]$ $mm \in [00,01, 10, 11]$ $-32 \leq k \leq 31$
Operation:	$W \rightarrow INDFn$ Effective address is determined by • FSR + 1 (preincrement) • FSR - 1 (predecrement) • FSR + k (relative offset) After the Move, the FSR value will be either: • FSR + 1 (all increments) • FSR - 1 (all decrements) Unchanged
Status Affected:	None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/ after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h - FFFFh. Incrementing/ decrementing it beyond these bounds will cause it to wrap-around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

OPTION	Load OPTION_REG Register with W
Syntax:	[*label*] OPTION
Operands:	None
Operation:	$(W) \rightarrow$ OPTION_REG
Status Affected:	None
Description:	Move data from W register to OPTION_REG register.

RESET	Software Reset
Syntax:	[*label*] RESET
Operands:	None
Operation:	Execute a device Reset. Resets the $\overline{RI}$ flag of the PCON register.
Status Affected:	None
Description:	This instruction provides a way to execute a hardware Reset by software.

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TABLE 30-3: POWER-DOWN CURRENTS (I_{PD})(1,2,4) (CONTINUED)

PIC16LF1784/6/7		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1784/6/7		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
	Power-down Base Current (I_{PD})(2)							
D029		—	0.05	2	9	μA	1.8	ADC Current **(Note 3)**, no conversion in progress
		—	0.08	3	10	μA	3.0	
D029		—	0.3	4	12	μA	2.3	ADC Current **(Note 3)**, no conversion in progress
		—	0.4	5	13	μA	3.0	
		—	0.5	7	16	μA	5.0	
D030		—	250	—	—	μA	1.8	ADC Current **(Note 3)**, conversion in progress
		—	280	—	—	μA	3.0	
D030		—	230	—	—	μA	2.3	ADC Current **(Note 3, Note 4, Note 5)**, conversion in progress
		—	250	—	—	μA	3.0	
		—	350	—	—	μA	5.0	
D031		—	250	650	—	μA	3.0	Op Amp (High power)
D031			250	650	—	μA	3.0	Op Amp (High power) **(Note 5)**
		—	350	850	—	μA	5.0	
D032		—	250	650	—	μA	1.8	Comparator, Normal-Power mode
		—	300	700	—	μA	3.0	
D032		—	280	650	—	μA	2.3	Comparator, Normal-Power mode **(Note 5)**
		—	300	700	—	μA	3.0	
		—	310	700	—	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC oscillator source is FRC.

4: 0.1 μF capacitor on V_{CAP}.

5: VREGPM = 0.

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Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

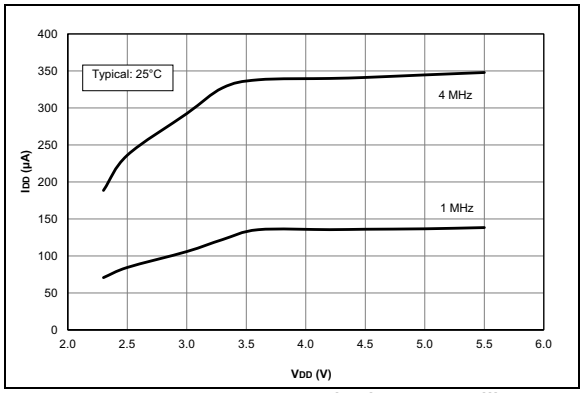

FIGURE 31-13: *IDD Typical, EC Oscillator MP Mode, PIC16F1784/6/7 Only.*

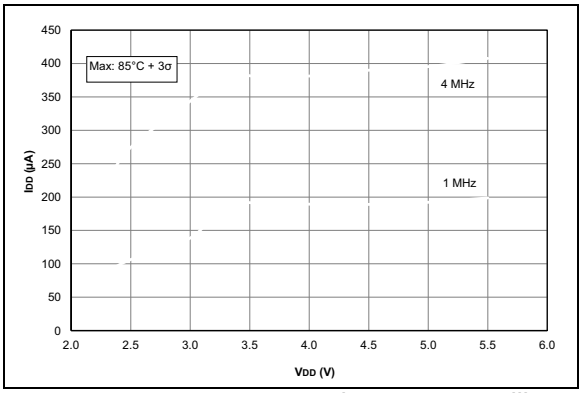

FIGURE 31-14: *IDD Maximum, EC Oscillator MP Mode, PIC16F1784/6/7 Only.*

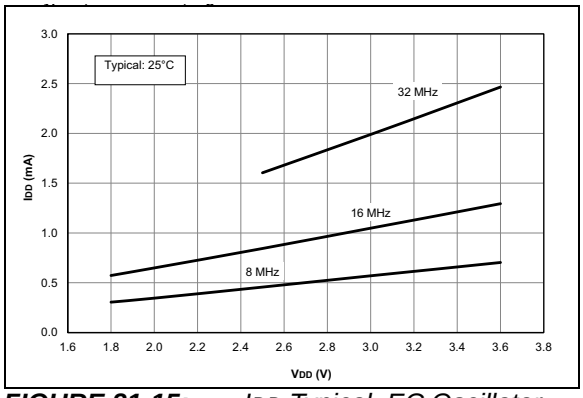

FIGURE 31-15: *IDD Typical, EC Oscillator HP Mode, PIC16LF1784/6/7 Only.*

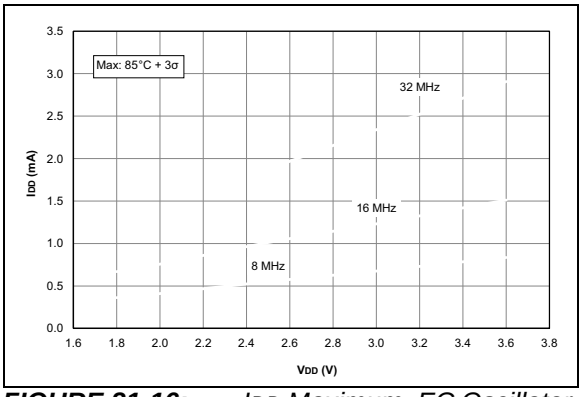

FIGURE 31-16: *IDD Maximum, EC Oscillator HP Mode, PIC16LF1784/6/7 Only.*

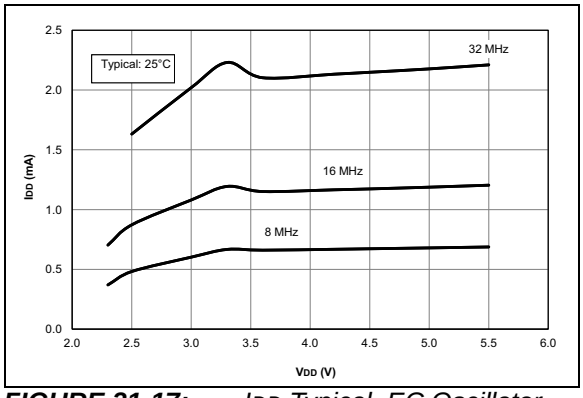

FIGURE 31-17: *IDD Typical, EC Oscillator HP Mode, PIC16F1784/6/7 Only.*

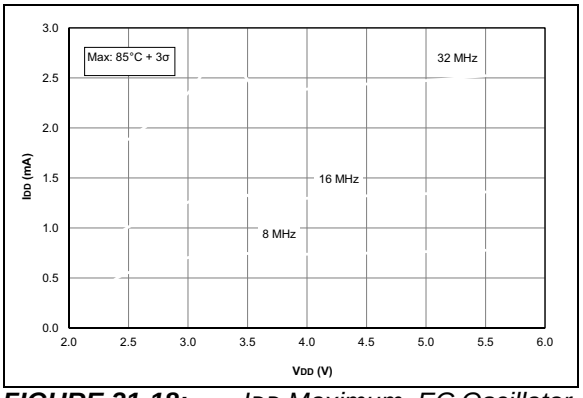

FIGURE 31-18: *IDD Maximum, EC Oscillator HP Mode, PIC16F1784/6/7 Only.*

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Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

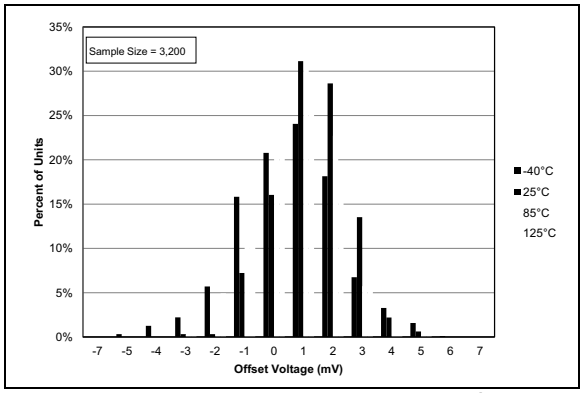

FIGURE 31-109: *Op Amp, Output Voltage Histogram, VDD = 3.0V, VCM = VDD/2.*

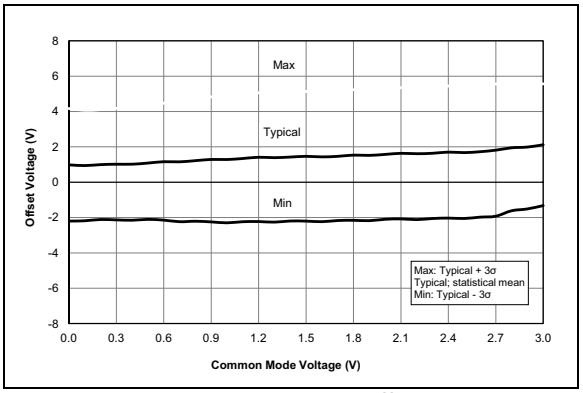

FIGURE 31-110: *Op Amp, Offset Over Common Mode Voltage, VDD = 3.0V, Temp. = 25°C.*

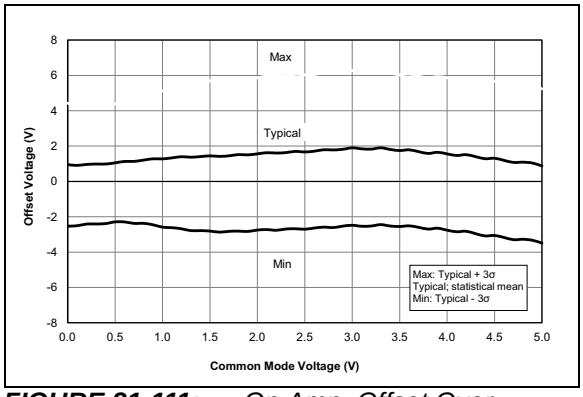

FIGURE 31-111: *Op Amp, Offset Over Common Mode Voltage, VDD = 5.0V, Temp. = 25°C, PIC16F1784/6/7 Only.*

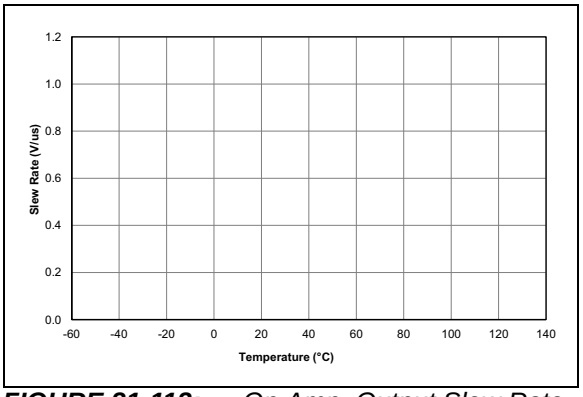

FIGURE 31-112: *Op Amp, Output Slew Rate, Rising Edge, PIC16LF1784/6/7 Only.*

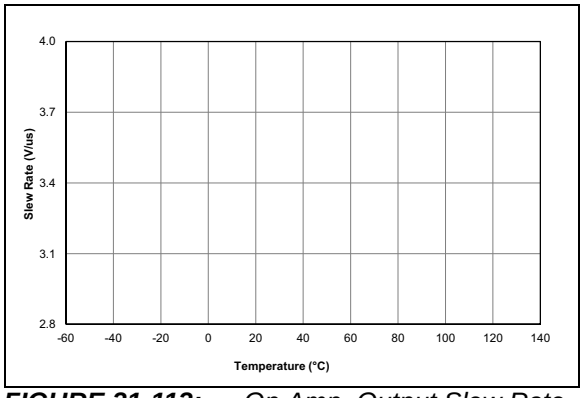

FIGURE 31-113: *Op Amp, Output Slew Rate, Falling Edge, PIC16LF1784/6/7 Only.*

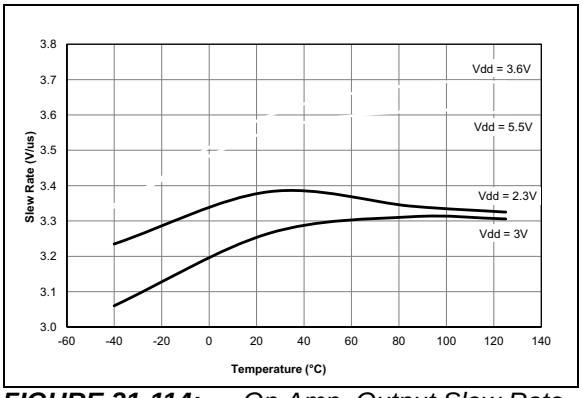

FIGURE 31-114: *Op Amp, Output Slew Rate, Rising Edge, PIC16F1784/6/7 Only.*

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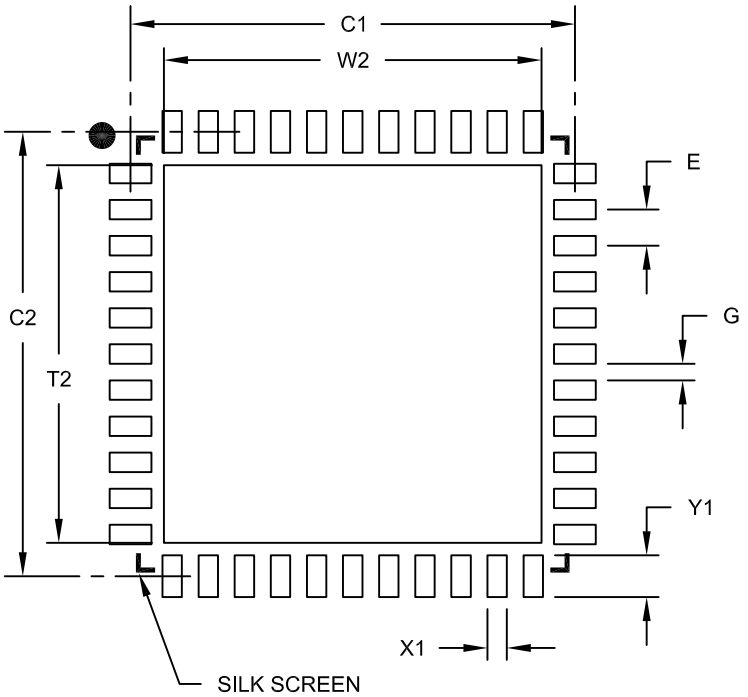
44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B