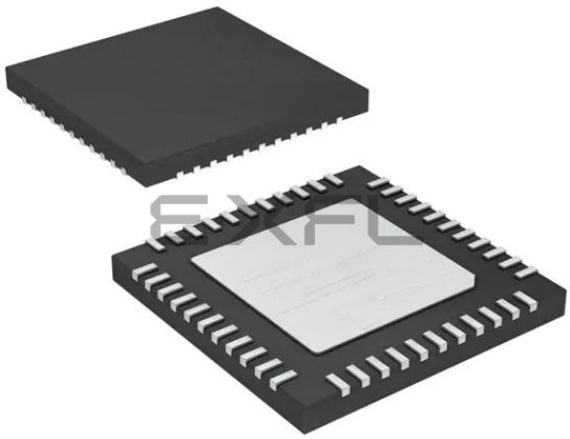

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1787t-i-ml

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 2											
10Ch	LATA	PORTA Data Latch								xxxx xxxx	uuuu uuuu
10Dh	LATB	PORTB Data Latch								xxxx xxxx	uuuu uuuu
10Eh	LATC	PORTC Data Latch								xxxx xxxx	uuuu uuuu
10Fh	LATD(3)	PORTD Data Latch								xxxx xxxx	uuuu uuuu
110h	LATE(3)	—	—	—	—	—	LATE2	LATE1	LATE0	---- -111	---- -111
111h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	0000 0100	0000 0100
112h	CM1CON1	C1INTP	C1INTN	C1PCH<2:0>			C1NCH<2:0>			0000 0000	0000 0000
113h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	0000 0100	0000 0100
114h	CM2CON1	C2INTP	C2INTN	C2PCH<2:0>			C2NCH<2:0>			0000 0000	0000 0000
115h	CMOUT	—	—	—	—	MC4OUT(3)	MC3OUT	MC2OUT	MC1OUT	---- 0000	---- 0000
116h	BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	1x-- ---q	uu-- ---u
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		0q00 0000	0q00 0000
118h	DAC1CON0	DAC1EN	---	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		---	DAC1NSS	0-00 00-0	0-00 00-0
119h	DAC1CON1	DAC1R<7:0>								0000 0000	0000 0000
11Ah	CM4CON0	C4ON	C4OUT	C4OE	C4POL	C4ZLF	C4SP	C4HYS	C4SYNC	0000 0100	0000 0100
11Bh	CM4CON1	C4INTP	C4INTN	C4PCH<1:0>		—	—	C4NCH<1:0>		0000 --00	0000 --00
11Ch	APFCON2	—	—	—	—	—	—	—	CCP3SEL	---- ---0	---- ---0
11Dh	APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	0000 0000	0000 0000
11Eh	CM3CON0	C3ON	C3OUT	C3OE	C3POL	C3ZLF	C3SP	C3HYS	C3SYNC	0000 0100	0000 0100
11Fh	CM3CON1	C3INTP	C3INTN	C3PCH<2:0>			C3NCH<2:0>			0000 0000	0000 0000
Bank 3											
18Ch	ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	1-11 1111	1-11 1111
18Dh	ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	-111 1111	-111 1111
18Eh	Unimplemented								—	—	—
18Fh	ANSELD(3)	—	—	—	—	—	ANSD2	ANSD1	ANSD0	---- -111	---- -111
190h	ANSELE(3)	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	---- -111
191h	EEADRL	EEPROM / Program Memory Address Register Low Byte								0000 0000	0000 0000
192h	EEADRH	—(2)	EEPROM / Program Memory Address Register High Byte							1000 0000	1000 0000
193h	EEDATL	EEPROM / Program Memory Read Data Register Low Byte								xxxx xxxx	uuuu uuuu
194h	EEDATH	—	—	EEPROM / Program Memory Read Data Register High Byte						--xx xxxx	--uu uuuu
195h	EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 x000	0000 q000
196h	EECON2	EEPROM / Program Memory Control Register 2								0000 0000	0000 0000
197h	VREGCON(4)	—	—	—	—	—	—	VREGPM	Reserved	---- --01	---- --01
198h	—	Unimplemented								—	—
199h	RCREG	EUSART Receive Data Register								0000 0000	0000 0000
19Ah	TXREG	EUSART Transmit Data Register								0000 0000	0000 0000
19Bh	SPBRG	BRG<7:0>								0000 0000	0000 0000
19Ch	SPBRGH	BRG<15:8>								0000 0000	0000 0000
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
19Fh	BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

3.6.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

FIGURE 3-10: TRADITIONAL DATA MEMORY MAP

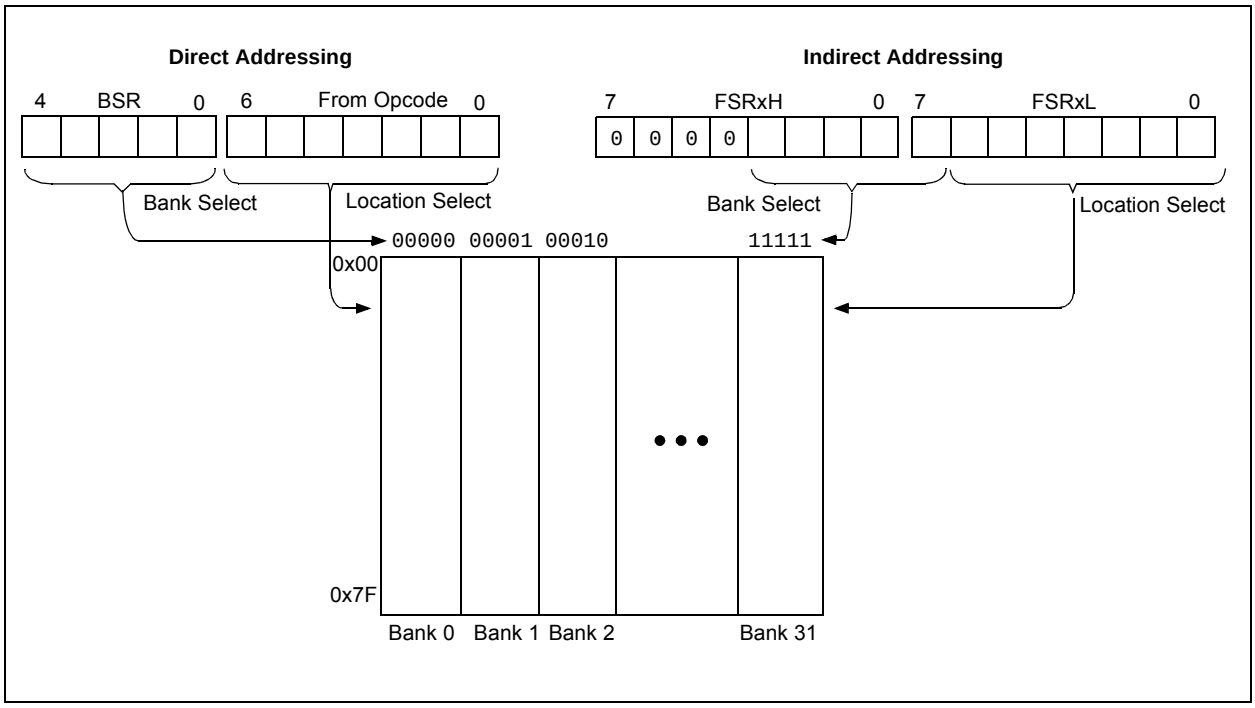
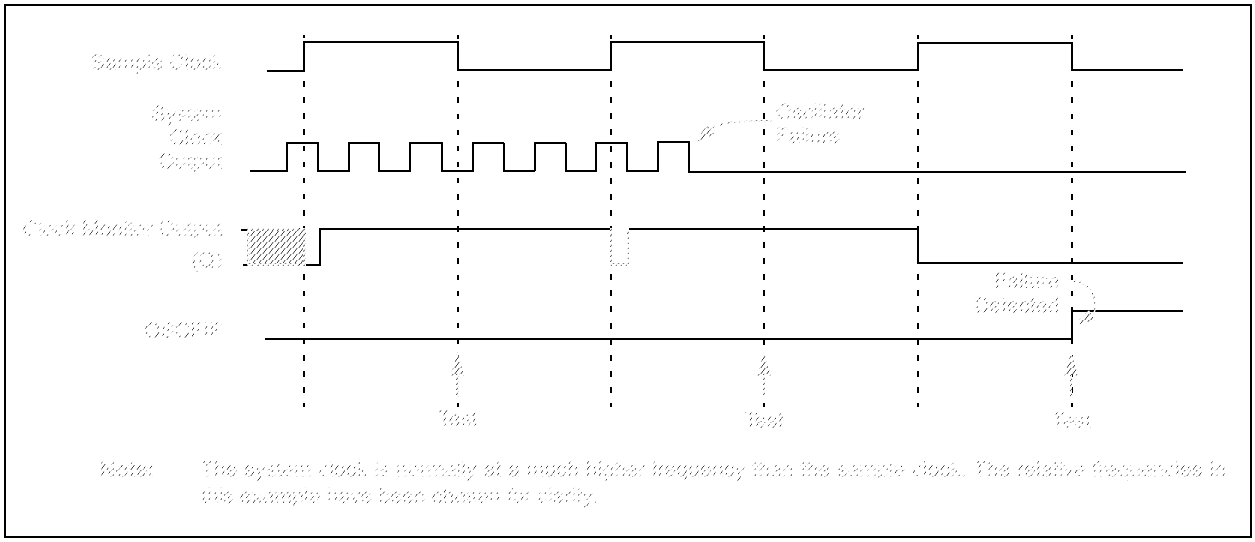


FIGURE 6-10: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

REGISTER 8-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6 **PSMC3TIE:** PSMC3 Time Base Interrupt Enable bit
- 1 = Enables PSMC3 time base generated interrupts
- 0 = Disables PSMC3 time base generated interrupts

bit 5 **PSMC2TIE:** PSMC2 Time Base Interrupt Enable bit
- 1 = Enables PSMC2 time base generated interrupts
- 0 = Disables PSMC2 time base generated interrupts

bit 4 **PSMC1TIE:** PSMC1 Time Base Interrupt Enable bit
- 1 = Enables PSMC1 time base generated interrupts
- 0 = Disables PSMC1 time base generated interrupts

bit 3 **Unimplemented:** Read as '0'

bit 2 **PSMC3SIE:** PSMC3 Auto-Shutdown Interrupt Enable bit
- 1 = Enables PSMC3 auto-shutdown interrupts
- 0 = Disables PSMC3 auto-shutdown interrupts

bit 1 **PSMC2SIE:** PSMC2 Auto-Shutdown Interrupt Enable bit
- 1 = Enables PSMC2 auto-shutdown interrupts
- 0 = Disables PSMC2 auto-shutdown interrupts

bit 0 **PSMC1SIE:** PSMC1 Auto-Shutdown Interrupt Enable bit
- 1 = Enables PSMC1 auto-shutdown interrupts
- 0 = Disables PSMC1 auto-shutdown interrupts

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

13.4 Register Definitions: PORTA

REGISTER 13-3: PORTA: PORTA REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **RA<7:0>**: PORTA I/O Value bits(1)
1 = Port pin is ≥ V_{IH}
0 = Port pin is ≤ V_{IL}

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 13-4: TRISA: PORTA TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TRISA<7:0>:** PORTA Tri-State Control bits
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

REGISTER 13-5: LATA: PORTA DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **LATA<7:0>**: PORTA Output Latch Value bits(1)

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

TABLE 13-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELD	—	—	—	—	—	ANSD2	ANSD1	ANSD0	147
INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	148
LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	146
ODCOND	ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0	148
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	146
SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	148
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	146
WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	147

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

FIGURE 22-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE

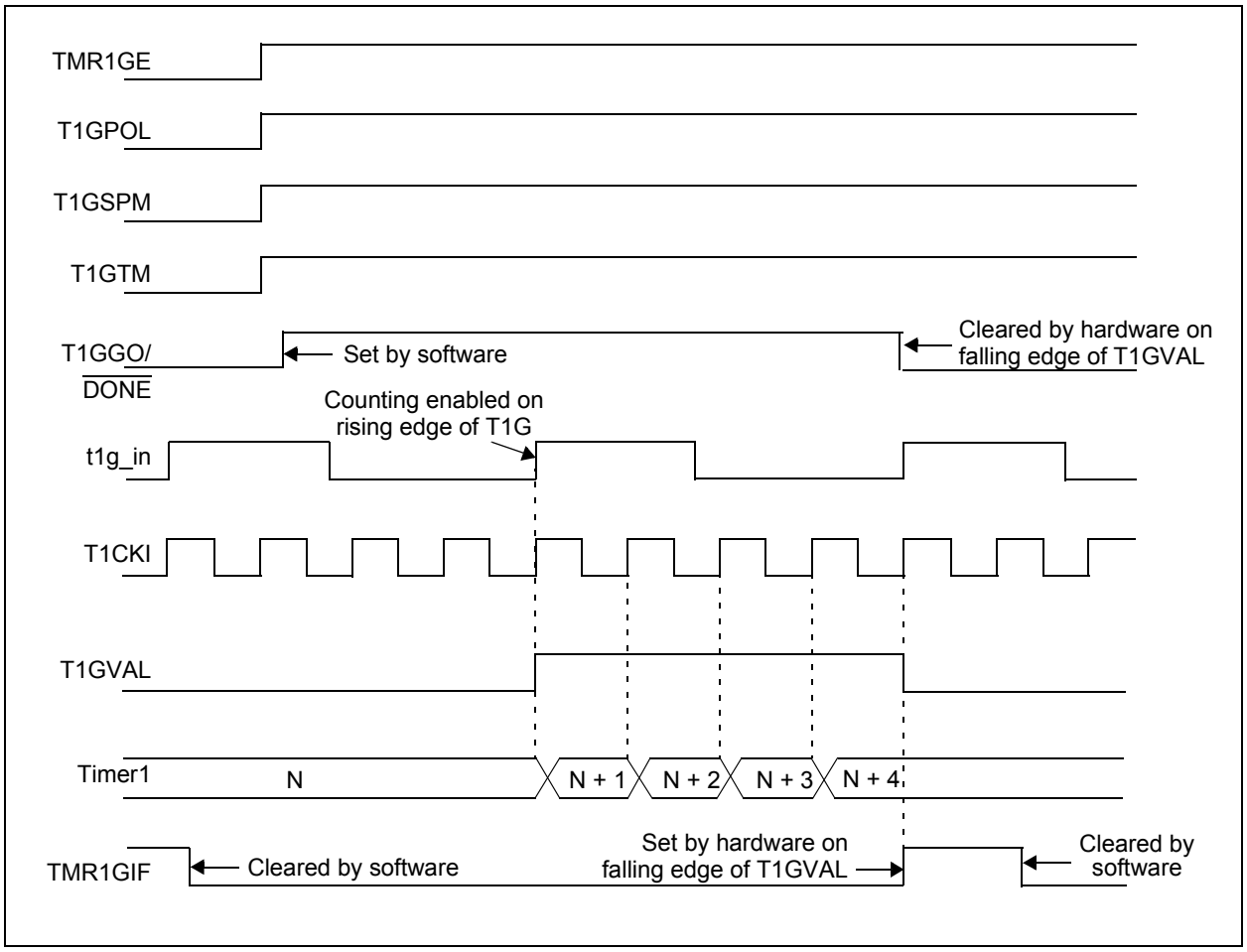


TABLE 22-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	138
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				280
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				280
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								199*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								199*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	137
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	207
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ $\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		208

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

* Page provides register information.

TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				280
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PR2	Timer2 Module Period Register								210*
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		212
TMR2	Holding Register for the 8-bit TMR2 Register								210*

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

* Page provides register information.

24.3.7 PULSE-SKIPPING PWM

The pulse-skipping PWM is used to generate a series of fixed-length pulses that can be triggered at each period event. A rising edge event will be generated when any enabled asynchronous rising edge input is active when the period event occurs, otherwise no event will be generated.

The rising edge event occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

24.3.7.1 Mode Features

- No dead-band control available
- No steering control available
- PWM is output to only one pin:
  - PSMCxA

24.3.7.2 Waveform Generation

Rising Edge Event

If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:

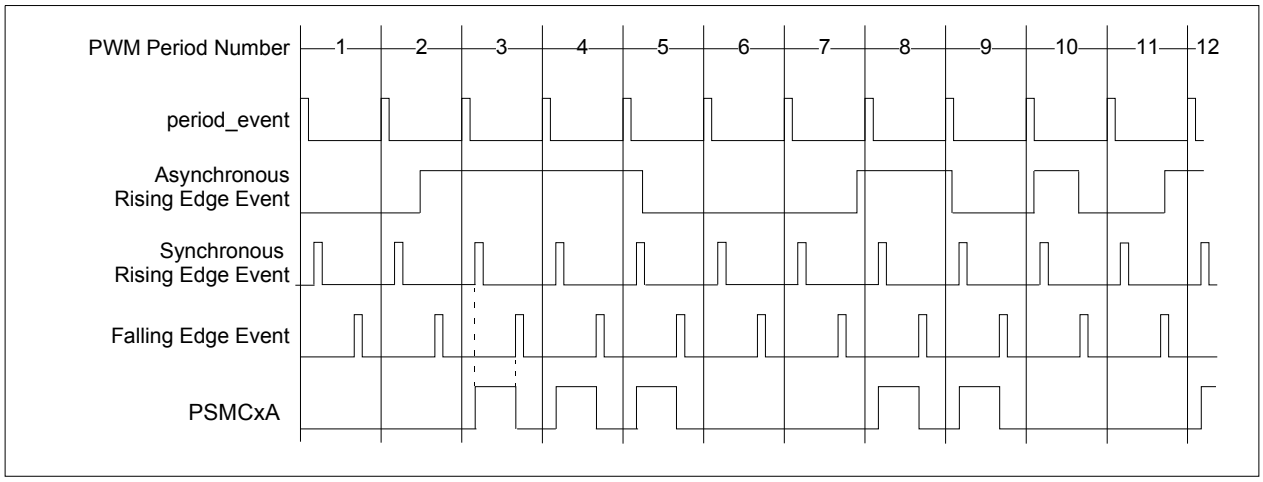
- PSMCxA is set active

Falling Edge Event

- PSMCxA is set inactive

Note:	To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 24-10: PULSE-SKIPPING PWM WAVEFORM



24.3.9 ECCP COMPATIBLE FULL-BRIDGE PWM

This mode of operation is designed to match the Full-Bridge mode from the ECCP module. It is called ECCP compatible as the term “full-bridge” alone has different connotations in regards to the output waveforms.

Full-Bridge Compatible mode uses the same waveform events as the single PWM mode to generate the output waveforms.

There are both Forward and Reverse modes available for this operation, again to match the ECCP implementation. Direction is selected with the mode control bits.

24.3.9.1 Mode Features

- Dead-band control available on direction switch
  - Changing from forward to reverse uses the falling edge dead-band counters.
  - Changing from reverse to forward uses the rising edge dead-band counters.
- No steering control available
- PWM is output on the following four pins only:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD

24.3.9.2 Waveform Generation - Forward

In this mode of operation, three of the four pins are static. PSMCxA is the only output that changes based on rising edge and falling edge events.

Static Signal Assignment

- Outputs set to active state
  - PSMCxD
- Outputs set to inactive state
  - PSMCxB
  - PSMCxC

Rising Edge Event

- PSMCxA is set active

Falling Edge Event

- PSMCxA is set inactive

24.3.9.3 Waveform Generation – Reverse

In this mode of operation, three of the four pins are static. Only PSMCxB toggles based on rising edge and falling edge events.

Static Signal Assignment

- Outputs set to active state
  - PSMCxC
- Outputs set to inactive state
  - PSMCxA
  - PSMCxD

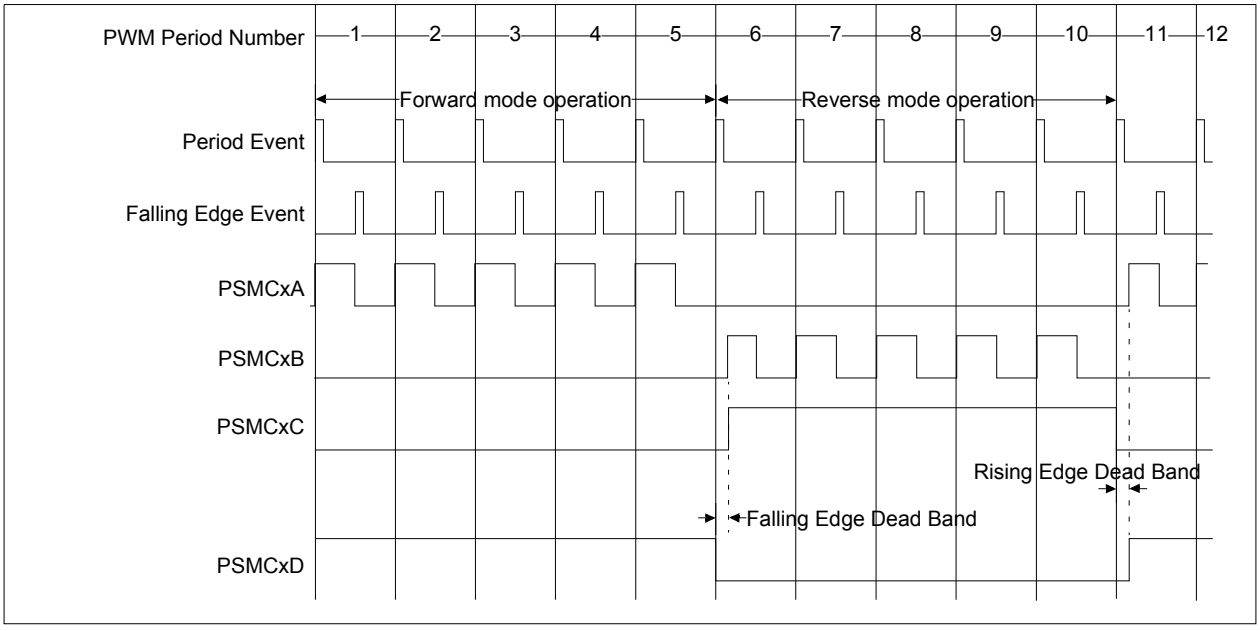
Rising Edge Event

- PSMCxB is set active

Falling Edge Event

- PSMCxB is set inactive

FIGURE 24-12: ECCP COMPATIBLE FULL-BRIDGE PWM WAVEFORM – PSMCXSTR0 = 0FH



24.7 Auto-Shutdown

Auto-shutdown is a method to immediately override the PSMC output levels with specific overrides that allow for safe shutdown of the application.

Auto-shutdown includes a mechanism to allow the application to restart under different conditions.

Auto-shutdown is enabled with the PxASDEN bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15). All auto-shutdown features are enabled when PxASDEN is set and disabled when cleared.

24.7.1 SHUTDOWN

There are two ways to generate a shutdown event:

- Manual
- External Input

24.7.1.1 Manual Override

The auto-shutdown control register can be used to manually override the pin functions. Setting the PxASE bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15) generates a software shut-down event.

The auto-shutdown override will persist as long as PxASE remains set.

24.7.1.2 External Input Source

Any of the given sources that are available for event generation are also available for system shut-down. This is so that external circuitry can monitor and force a shutdown without any software overhead. Auto-shutdown sources are selected with the PSMC Auto-shutdown Source (PSMCxASDS) register (Register 24-17).

When any of the selected external auto-shutdown sources go high, the PxASE bit is set and an auto-shutdown interrupt is generated.

Note:	The external shutdown sources are level sensitive, not edge sensitive. The shutdown condition will persist as long as the circuit is driving the appropriate logic level.

24.7.2 PIN OVERRIDE LEVELS

The logic levels driven to the output pins during an auto-shutdown event are determined by the PSMC Auto-shutdown Output Level (PSMCxASDL) register (Register 24-16).

24.7.2.1 PIN Override Enable

Setting the PxASDOV bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15) will also force the override levels onto the pins, exactly like what happens when the auto-shutdown is used. However, whereas setting PxASE causes an auto-shutdown interrupt, setting PxASDOV does not generate an interrupt.

24.7.3 RESTART FROM AUTO-SHUTDOWN

After an auto-shutdown event has occurred, there are two ways for the module to resume operation:

- Manual restart
- Automatic restart

The restart method is selected with the PxARSEN bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15).

24.7.3.1 Manual Restart

When PxARSEN is cleared, and once the PxASDE bit is set, it will remain set until cleared by software.

The PSMC will restart on the period event after PxASDE bit is cleared in software.

24.7.3.2 Auto-Restart

When PxARSEN is set, the PxASDE bit will clear automatically when the source causing the Reset and no longer asserts the shut-down condition.

The PSMC will restart on the next period event after the auto-shutdown condition is removed.

Examples of manual and automatic restart are shown in Figure 24-20.

Note:	Whether manual or auto-restart is selected, the PxASDE bit cannot be cleared in software when the auto-shutdown condition is still present.

REGISTER 24-6: PSMCxCLK: PSMC CLOCK CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	PxCPRE<1:0>		—	—	PxCSRC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **PxCPRE<1:0>:** PSMCx Clock Prescaler Selection bits
11 = PSMCx Clock frequency/8
10 = PSMCx Clock frequency/4
01 = PSMCx Clock frequency/2
00 = PSMCx Clock frequency/1

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **PxCSRC<1:0>:** PSMCx Clock Source Selection bits
11 = Reserved
10 = PSMCxCLK pin
01 = 64 MHz clock in from PLL
00 = FOSC system clock

REGISTER 24-7: PSMCxOEN: PSMC OUTPUT ENABLE CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	PxOEF(1)	PxOEE(1)	PxOED(1)	PxOEC(1)	PxOEB	PxOEA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **PxOEy:** PSMCx Output y Enable bit(1)
1 = PWM output is active on PSMCx output y pin
0 = PWM output is not active, normal port functions in control of pin

Note 1: These bits are not implemented on PSMC2.

REGISTER 24-14: PSMCxPRS: PSMC PERIOD SOURCE REGISTER(1)

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxPRSIN	—	—	PxPRSC4	PxPRSC3	PxPRSC2	PxPRSC1	PxPRST
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxPRSIN:** PSMCx Period Event occurs on PSMCxIN pin
- 1 = Period event will occur and PSMCxTMR will reset when PSMCxIN pin goes true
- 0 = PSMCxIN pin will not cause period event

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxPRSC4:** PSMCx Period Event occurs on sync_C4OUT output
- 1 = Period event will occur and PSMCxTMR will reset when sync_C4OUT output goes true
- 0 = sync_C4OUT will not cause period event

bit 3 **PxPRSC3:** PSMCx Period Event occurs on sync_C3OUT output
- 1 = Period event will occur and PSMCxTMR will reset when sync_C3OUT output goes true
- 0 = sync_C3OUT will not cause period event

bit 2 **PxPRSC2:** PSMCx Period Event occurs on sync_C2OUT output
- 1 = Period event will occur and PSMCxTMR will reset when sync_C2OUT output goes true
- 0 = sync_C2OUT will not cause period event

bit 1 **PxPRSC1:** PSMCx Period Event occurs on sync_C1OUT output
- 1 = Period event will occur and PSMCxTMR will reset when sync_C1OUT output goes true
- 0 = sync_C1OUT will not cause period event

bit 0 **PxPRST:** PSMCx Period Event occurs on Time Base match
- 1 = Period event will occur and PSMCxTMR will reset when PSMCxTMR = PSMCxPR
- 0 = Time base will not cause period event

Note 1: Sources are not mutually exclusive: more than one source can force the period event and reset the PSMCxTMR.

26.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 26-29).

26.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

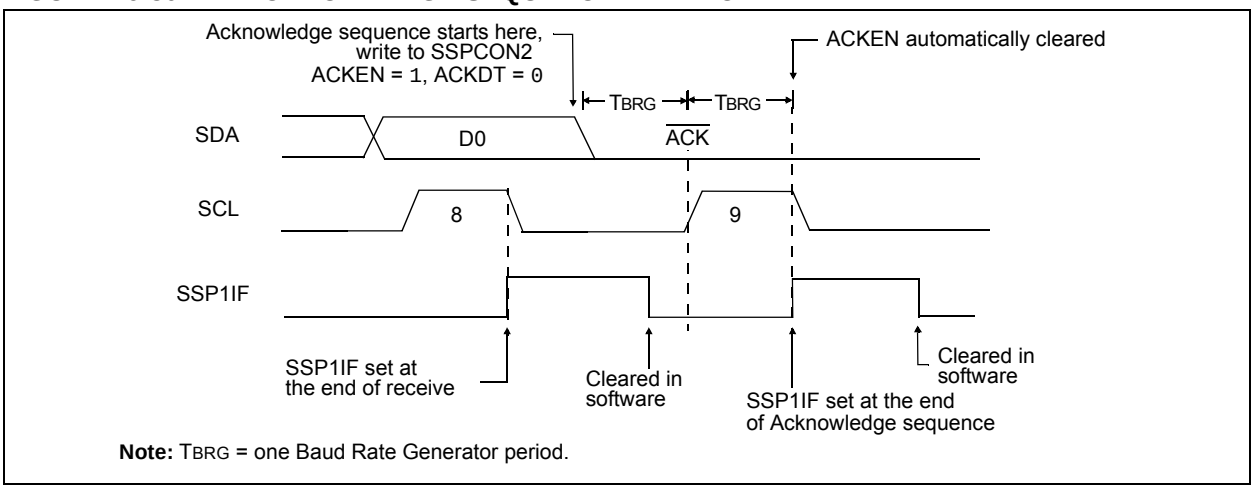
26.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 26-30).

26.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 26-30: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

26.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPADD register (Register 26-6). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

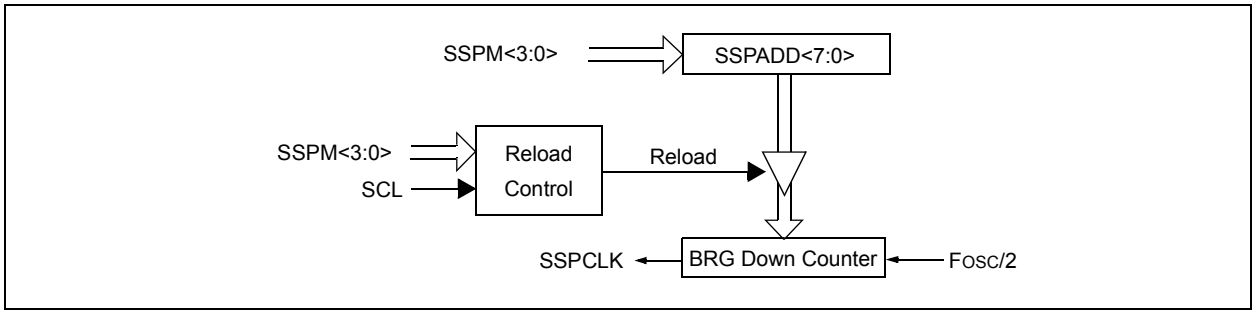
An internal signal “Reload” in Figure 26-39 triggers the value from SSPADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 26-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

EQUATION 26-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSPxADD + 1)(4)}$$

FIGURE 26-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

TABLE 26-4: MSSP CLOCK RATE W/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz(1)
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz(1)
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note 1: The I^2C interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

27.1.1.5 TSR Status

The TRMT bit of the TXSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

27.1.1.6 Transmitting 9-Bit Characters

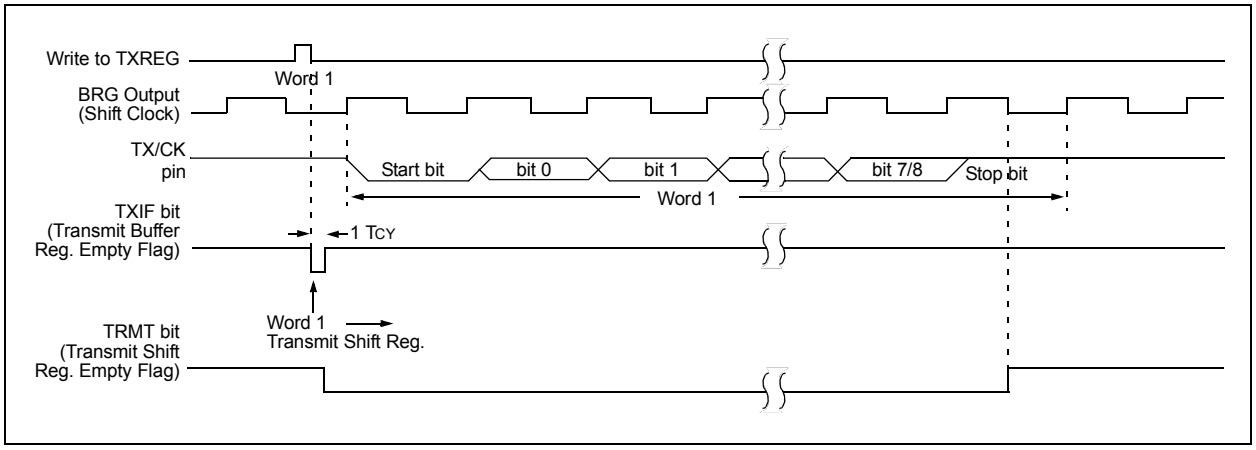
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXSTA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXSTA register is the ninth, and Most Significant, data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 27.1.2.7 "Address Detection"** for more information on the address mode.

27.1.1.7 Asynchronous Transmission Set-up:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 27.4 "EUSART Baud Rate Generator (BRG)"**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
6. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXREG register. This will start the transmission.

FIGURE 27-3: ASYNCHRONOUS TRANSMISSION



REGISTER 27-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6 **RX9:** 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
Don't care
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave
Don't care

bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enable interrupt and load the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 8-bit (RX9 = 0):
Don't care

bit 2 **FERR:** Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D:** Ninth bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

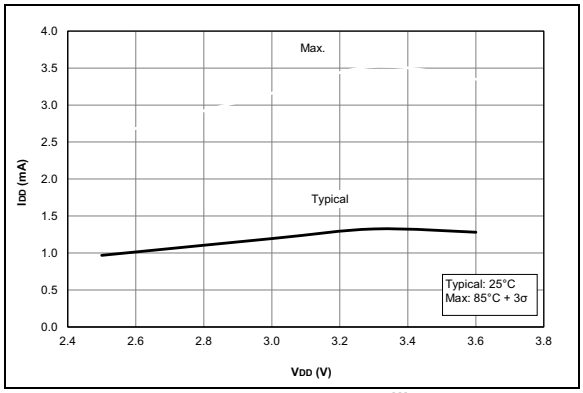


FIGURE 31-31: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16LF1784/6/7 Only.*

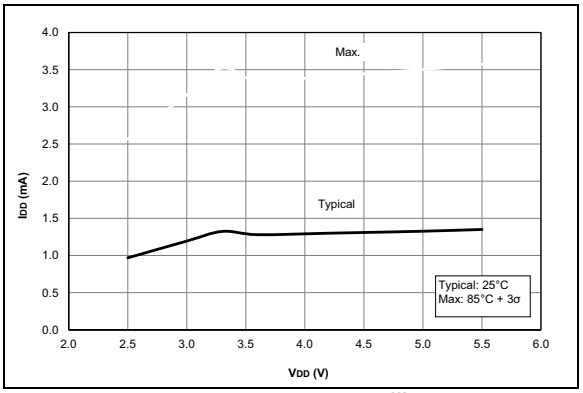


FIGURE 31-32: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1784/6/7 Only.*

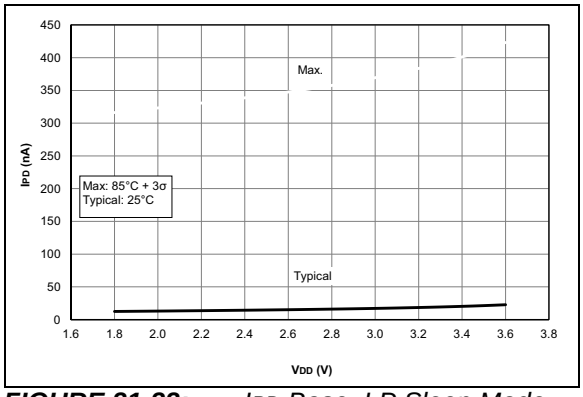


FIGURE 31-33: *IPD Base, LP Sleep Mode, PIC16LF1784/6/7 Only.*

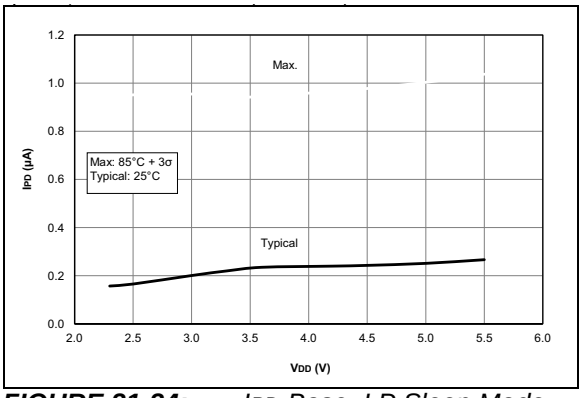


FIGURE 31-34: *IPD Base, LP Sleep Mode (VREGPM = 1), PIC16F1784/6/7 Only.*

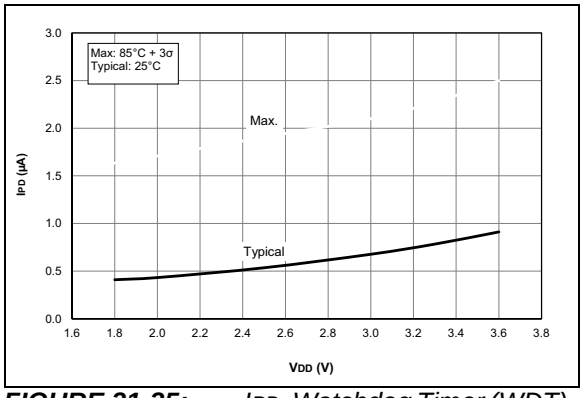


FIGURE 31-35: *IPD, Watchdog Timer (WDT), PIC16LF1784/6/7 Only.*

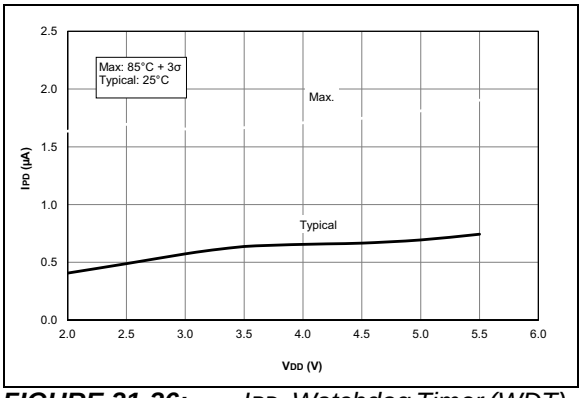


FIGURE 31-36: *IPD, Watchdog Timer (WDT), PIC16F1784/6/7 Only.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

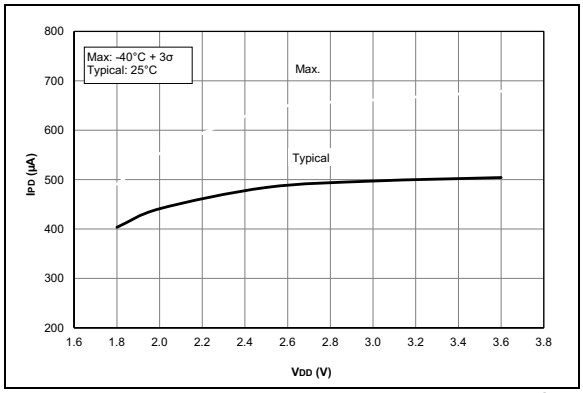


FIGURE 31-49: *IPD, Comparator, NP Mode (CxSP = 1), PIC16LF1784/6/7 Only.*

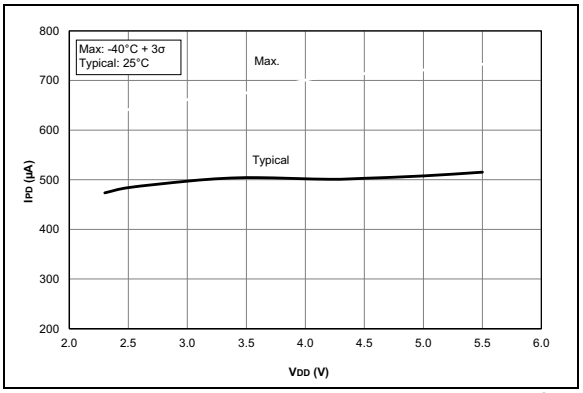


FIGURE 31-50: *IPD, Comparator, NP Mode (CxSP = 1), PIC16F1784/6/7 Only.*

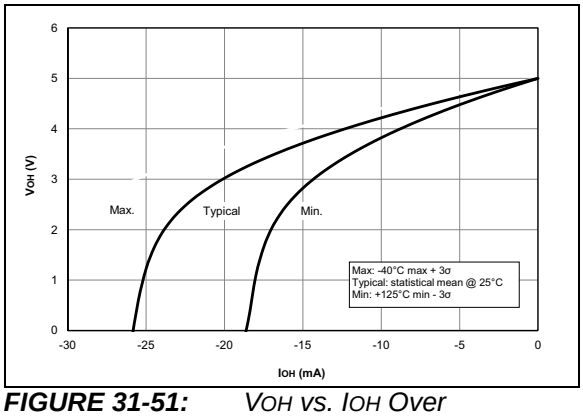


FIGURE 31-51: *VOH vs. IOH Over Temperature, VDD = 5.0V, PIC16F1784/6/7 Only.*

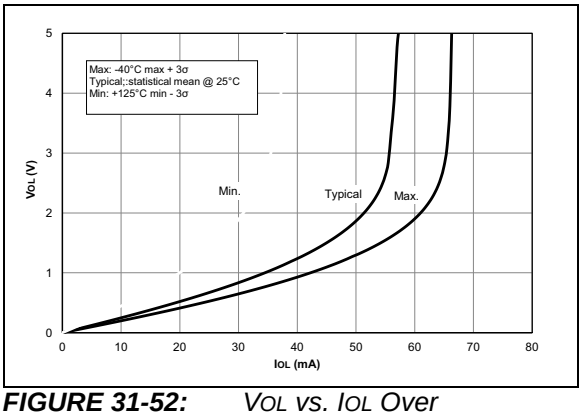


FIGURE 31-52: *VOL vs. IOL Over Temperature, VDD = 5.0V, PIC16F1784/6/7 Only.*

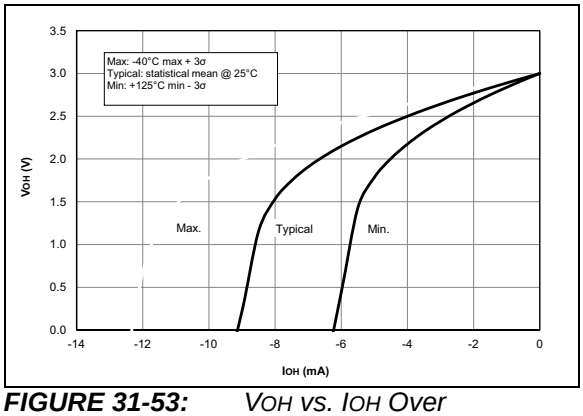


FIGURE 31-53: *VOH vs. IOH Over Temperature, VDD = 3.0V.*

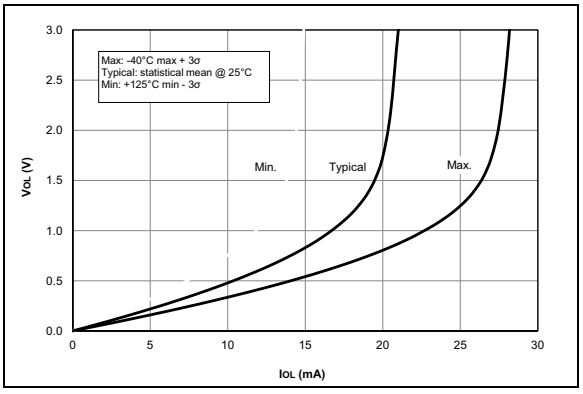


FIGURE 31-54: *VOL vs. IOL Over Temperature, VDD = 3.0V.*