

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1784-e-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
 - Configuration Words
 - Device ID
 - User ID
 - Flash Program Memory
- Data Memory
 - Core Registers
 - Special Function Registers
 - General Purpose RAM
 - Common RAM
- Data EEPROM memory⁽¹⁾

	Program Memory Control".								
	Sectio	on 12.0	"Data El	EPRON	l and Fl	lash			
	the E	ECON	register	s is de	escribed	d in			
	metho	d to ac	cess Flas	h mem	ory thro	ough			
Note 1:	The D	Data E	EPROM	Memo	ry and	the			

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1784/6/7 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address		
PIC16(L)F1784	4,096	0FFFh		
PIC16(L)F1786/7	8,192	1FFFh		

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.6** "**Indirect Addressing**" for more information.

Data memory uses a 12-bit address. The upper 5 bits of the address define the Bank address and the lower 7 bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-11.

TABLE 3-2: CORE REGISTER	S
--------------------------	---

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

6.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

A fast startup oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

6.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

6.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 6-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

6.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a multiplexer (see Figure 6-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See Section 6.2.2.7 "Internal Oscillator Clock Switch Timing" for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low-Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.

13.3.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-2.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input functions, such as ADC, and comparator inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown in the priority list.

Pin Name	Function Priority ⁽¹⁾
RA0	RA0
RA1	OPA1OUT RA1
RA2	DAC1OUT1 RA2
RA3	RA3
RA4	C1OUT RA4
RA5	C2OUT RA5
RA6	CLKOUT C2OUT RA6
RA7	RA7

TABLE 13-2: PORTA OUTPUT PRIORITY

Note 1: Priority listed from highest to lowest.

19.6 Register Definitions: DAC Control

REGISTER 19-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
DAC1EN	_	DAC10E1	DAC10E2	DAC1F	PSS<1:0>	_	DAC1NSS
bit 7		•					bit 0
Legend:							
R = Readable b	it	W = Writable b	oit	U = Unimplen	nented bit, read a	is '0'	
u = Bit is uncha	nged	x = Bit is unkno	own	-n/n = Value a	t POR and BOR	Value at all oth	er Resets
'1' = Bit is set		'0' = Bit is clea	red				
bit 7	DAC1EN: DAC 1 = DAC1 is e 0 = DAC1 is d	C1 Enable bit enabled lisabled					
bit 6	Unimplement	ed: Read as '0'					
bit 5	DAC1OE1: DA 1 = DAC1 volt 0 = DAC1 volt	AC1 Voltage Ou tage level is als tage level is dis	tput 1 Enable I o an output on connected fror	bit the DAC1OUT n the DAC1OU	1 pin T1 pin		
bit 4	DAC1OE2: DA 1 = DAC1 volt 0 = DAC1 volt	AC1 Voltage Ou tage level is als tage level is dis	tput 2 Enable I o an output on connected fror	bit the DAC1OUT n the DAC1OU	2 pin T2 pin		
bit 3-2	DAC1PSS<1:0 11 = Reserve 10 = FVR But 01 = VREF+ p 00 = VDD	D>: DAC1 Positi ed, do not use ffer2 output in	ve Source Sel	ect bits			
bit 1	Unimplement	ed: Read as '0'					
bit 0	DAC1NSS: DA 1 = VREF- pin 0 = VSS	AC1 Negative S	ource Select b	its			

REGISTER 19-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
			DAC1	R<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit	:	W = Writable bit	t	U = Unimplem	nented bit, read a	as '0'	

bit 7-0	DAC1R<7:0>: DAC1 Voltage Output Select bits

x = Bit is unknown

'0' = Bit is cleared

TABLE 19-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	′R<1:0>	ADFVI	R<1:0>	162
DAC1CON0	DAC1EN	_	DAC10E1	DAC10E2	DAC1PSS<1:0>		—	DAC1NSS	186
DAC1CON1		DAC1R<7:0>							186

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the DAC module.

u = Bit is unchanged

'1' = Bit is set

-n/n = Value at POR and BOR/Value at all other Resets

PIC16(L)F1784/6/7

FIGURE 22-6:	TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE	
TMR1GE		
T1GPOL		
T1GSPM		
T1GTM		
T1GG <u>O/</u> DONE	← Set by software Cleared by hardware falling edge of T1GVA Counting enabled on	on \L
t1g_in		
Т1СКІ		
T1GVAL		
Timer1	N N + 1 N + 2 N + 3 N + 4	
TMR1GIF	Set by hardware on Cleared by Software falling edge of T1GVAL> Cleared by Software	у

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0
PxASE	PxASDEN	PxARSEN	—	—	—	_	PxASDOV
bit 7	- -	•					bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other R						other Resets	
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	PxASE: PWN	I Auto-Shutdov	vn Event Statu	us bit ⁽¹⁾			
	1 = A shutdo	own event has	occurred, PW	M outputs are	inactive and in f	heir shutdown	states
	0 = PWM or	utputs are oper	ating normally	/			
bit 6	PxASDEN: P	WM Auto-Shut	down Enable	bit			
	1 = Auto-sh	utdown is enab	led. If any of t	he sources in I	PSMCxASDS a	ssert a logic '1	', then the out-
	puts will	go into their au	uto-shutdown	state and PSN	ICxSIF flag will	be set.	
bit 5	Dy ADSENI		neu art Enabla bit				
DIL 5		otorto automati		a abutdown oo	adition is romay	od	
	1 = FWWWWWWWWWWWWWWWWWWWWWWWWWWWWWWWWWWW	SE bit must be	cleared in fir	mware to resta	art PWM after th	eu. e auto-shutdov	wn condition is
	cleared.						
bit 4-1	Unimplemen	ted: Read as '	כי				
bit 0	PxASDOV: P	WM Auto-Shut	down Overrid	e bit			
	PxASDEN =	<u>L:</u>					
	1 = Force P	xASDL[n] level	s on the PSM	Cx[n] pins with	out causing a P	SMCxSIF inte	rrupt
	0 = Normal	PWM and auto	-shutdown ex	ecution			
	PxASDEN = (<u>):</u>					
	NO effect						
Note 1: PAS	SE bit may be s	et in software.	When this oc	curs the function	onality is the sar	ne as that cau	sed by
har	dware.						

REGISTER 24-15: PSMCxASDC: PSMC AUTO-SHUTDOWN CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	
_	_	PxSTRF ⁽²⁾	PxSTRE ⁽²⁾	PxSTRD ⁽²⁾	PxSTRC ⁽²⁾	PxSTRB	PxSTRA	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	W = Writable bit U = Unimplemented bit, read as '0'					
u = Bit is uncha	anged	x = Bit is unkr	ther Resets					
'1' = Bit is set		'0' = Bit is clea	'0' = Bit is cleared					
bit 7-6	Unimplemen	tad: Pead as '	،					
bit 5		M Steering PSI		Enable hit(2)				
bit 5		:0> = 0000 (Si	nale-nhase Pl					
	1 = Single P	WM output is a	active on pin P	/ <u>/////.</u> /SMCxF				
	0 = Single P	WM output is r	not active on p	in PSMCxF. P	WM drive is in in	active state		
	If PxMODE<3	:0> = 0001 (C	omplementary	Single-phase	<u>PWM):</u>			
	1 = Complexistence 1 = Complex	mentary PWM	output is active	e on pin PSM(ctive on pin P	CXF SMCxOUT5_PW	/M drive is in i	nactive state	
	IF PxMODE<	3.0 > = 1100 (3)	-nhase Steerij	ייייע און				
	1 = PSMCx[D and PSMCxE	are high. PS	MCxA, PMSC	xB, PSMCxC and	d PMSCxF are	e low.	
	0 = 3-phase	= 3-phase output combination is not active						
bit 4	PxSTRE: PW	M Steering PS	MCxE Output	Enable bit ⁽²⁾				
	If PxMODE<3	: <u>0> = 000x (si</u>	<u>ngle-phase PV</u>	VM or Comple	mentary PWM):			
	1 = Single P 0 = Single P	WM output is a	not active on pin P	INCXE	WM drive is in ir	nactive state		
	IF PxMODE<	3:0> = 1100 (3	-phase Steerii	na): ⁽¹⁾				
	1 = PSMCxE	3 and PSMCxE	are high. PSI	MCxA, PMSC>	C, PSMCxD and	d PMSCxF are	e low.	
	0 = 3-phase	output combin	ation is not ac	tive				
bit 3	PxSTRD: PW	M Steering PS	MCxD Output	Enable bit ⁽²⁾				
	$\frac{\text{If PxMODE}<3}{1 = \text{Single P}}$: <u>:0> = 0000 (Si</u> WM output is a	<u>ngle-phase Pl</u> active on pin P	<u>//M):</u> /SMCxD				
	0 = Single P	WM output is r	not active on pin r	in PSMCxD. F	PWM drive is in ir	nactive state		
	If PxMODE<3	:0> = 0001 (Ce	omplementary	single-phase	<u>PWM):</u>			
	1 = Compler	mentary PWM	output is active	e on pin PSMC				
			putput is not a	ctive on pin Pa	SINCXD. PVVIVI di	rive is in inacti	ve state	
	1 = PSMCxE	$3.0^{2} = 1100$ (3) B and PSMCx(are high. PS	<u>ig).</u> MCxA. PMSC:	xD. PSMCxE and	d PMSCxF are	e low.	
	0 = 3-phase	output combin	ation is not ac	tive	,			
bit 2	PxSTRC: PW	M Steering PS	MCxC Output	Enable bit ⁽²⁾				
	If PxMODE<3	:0> = 000x (Si	ngle-phase P\	NM or Comple	ementary PWM):			
	1 = Single P	WM output is a	active on pin P		N/M drivo is in ir	pactivo stato		
		$\frac{1}{3.0} = 1100$	nhase Steerin	יוו רטויוטגט. ד _{ממ} ן.(1)		Idelive Slale		
	1 = PSMCx(C and PSMCxF	are high. PSI	ري. MCxA, PMSC>	B, PSMCxD and	d PMSCxE are	e low.	
	0 = 3-phase	output combin	ation is not ac	tive				

REGISTER 24-31: PSMCxSTR0: PSMC STEERING CONTROL REGISTER 0

25.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 25-3 shows a typical waveform of the PWM signal.

25.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- · PR2 registers
- · T2CON registers
- · CCPRxL registers
- · CCPxCON registers

Figure 25-4 shows a simplified block diagram of PWM operation.

- Note 1: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
 - 2: Clearing the CCPxCON register will relinquish control of the CCPx pin.

FIGURE 25-3: CCP PWM OUTPUT SIGNAL





SIMPLIFIED PWM BLOCK DIAGRAM



26.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 26-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and Status bits appropriately set). The clock polarity is selected by appropriately programming the CKP bit of the SSPCON1 register and the CKE bit of the SSPSTAT register. This then, would give waveforms for SPI communication as shown in Figure 26-6, Figure 26-8 and Figure 26-9, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 * Tcy)
- Fosc/64 (or 16 * Tcy)
- Timer2 output/2
- Fosc/(4 * (SSPADD + 1))

Figure 26-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 26-6: SPI MODE WAVEFORM (MASTER MODE)



26.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 26-29).

26.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

26.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 26-30).

26.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 26-30: ACKNOWLEDGE SEQUENCE WAVEFORM



27.4.1 AUTO-BAUD DETECT

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII "U") which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDCON register starts the auto-baud calibration sequence (Figure 27-6). While the ABD sequence takes place, the EUSART state machine is held in idle. On the first rising edge of the receive line, after the Start bit, the SPBRG begins counting up using the BRG counter clock as shown in Table 27-6. The fifth rising edge will occur on the RX pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPBRGH, SPBRGL register pair, the ABDEN bit is automatically cleared and the RCIF interrupt flag is set. The value in the RCREG needs to be read to clear the RCIF interrupt. RCREG content should be discarded. When calibrating for modes that do not use the SPBRGH register the user can verify that the SPBRGL register did not overflow by checking for 00h in the SPBRGH register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 27-6. During ABD, both the SPBRGH and SPBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPBRGH and SPBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

- Note 1: If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see Section 27.4.3 "Auto-Wake-up on Break").
 - 2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.
 - 3: During the auto-baud process, the auto-baud counter starts counting at 1. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPBRGH:SPBRGL register pair.

TABLE 27-6: BRG COUNTER CLOCK RATES

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
0	0	Fosc/64	Fosc/512
0	1	Fosc/16	Fosc/128
1	0	Fosc/16	Fosc/128
1	1	Fosc/4	Fosc/32

Note: During the ABD sequence, SPBRGL and SPBRGH registers are both used as a 16-bit counter, independent of BRG16 setting.

0000h XXXXh 001Ch **BRG** Value Edge #5 Edge #1 Edge #2 Edge #3 Edge #4 bit 0 bit 1 bit 2 bit 3 bit 4 bit 5 bit 6 bit 7 RX pin Start Stop bit Auto Cleared Set by User ABDEN bit RCIDL RCIF bit (Interrupt) Read RCREG SPBRGL XXh 1Ch XXh 00h SPBRGH Note 1: The ABD sequence requires the EUSART module to be configured in Asynchronous mode.

FIGURE 27-6: AUTOMATIC BAUD RATE CALIBRATION

27.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

27.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 27-7), and asynchronously if the device is in Sleep mode (Figure 27-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

27.4.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

PIC16(L)F1784/6/7

RX/DT pin TX/CK pin (SCKP = 0)	bit 0 bit 1 bit 2 bit 3 bit 4 bit 5 bit 6 bit 7	
TX/CK pin (SCKP = 1) Write to bit SREN		
SREN bit	L	<u>'0'</u>
RCIF bit (Interrupt) ——— Read RCREG ———		
Note: Timi	ng diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0 .	

FIGURE 27-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)

TABLE 27-8: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	127
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	347
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCREG	EUSART Receive Data Register								340*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	346
SPBRGL	BRG<7:0>							348	
SPBRGH	BRG<15:8>							348	
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	345

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master reception.

* Page provides register information.

29.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- · Byte Oriented
- · Bit Oriented
- · Literal and Control

The literal and control category contains the most varied instruction word format.

Table 29-3 lists the instructions recognized by the MPASM $^{\rm TM}$ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)

TABLE 29-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Pre-post increment-decrement mode selection

TABLE 29-2: ABBREVIATION DESCRIPTIONS

Field	Description				
PC	Program Counter				
TO	Time-Out bit				
С	Carry bit				
DC	Digit Carry bit				
Z	Zero bit				
PD	Power-Down bit				

 One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

29.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

30.0 ELECTRICAL SPECIFICATIONS

30.1 Absolute Maximum Ratings^(†)

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on pins with respect to Vss	
on VDD pin	
PIC16F1784/6/7	0.3V to +6.5V
PIC16LF1784/6/7	0.3V to +4.0V
on MCLR pin	0.3V to +9.0V
on all other pins0.3	3V to (VDD + 0.3V)
Maximum current	
on Vss pin ⁽¹⁾	
-40°C \leq Ta \leq +85°C \ldots	340 mA
-40°C \leq Ta \leq +125°C	140 mA
on VDD pin ⁽¹⁾	
-40°C \leq Ta \leq +85°C (PIC16(L)F1786 only)	170 mA
-40°C \leq Ta \leq +125°C (PIC16(L)F1786 only)	70 mA
-40°C \leq Ta \leq +85°C \ldots	340 mA
-40°C \leq Ta \leq +125°C	140 mA
on any I/O pin	±25 mA
Clamp current, IK (VPIN < 0 or VPIN > VDD)	±20 mA

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Section 30.4 "Thermal Considerations" to calculate device specifications.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

otanidai								
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions	
		Program Memory Programming Specifications						
D110	Vінн	Voltage on MCLR/VPP/RE3 pin	8.0	_	9.0	V	(Note 3)	
D111	IDDP	Supply Current during Programming	—	_	10	mA		
D112		VDD for Bulk Erase	2.7	_	VDDMAX	V		
D113	VPEW	VDD for Write or Row Erase	VDDMIN	—	VDDMAX	V		
D114	IPPPGM	Current on MCLR/VPP during Erase/Write	_	—	1.0	mA		
D115	IDDPGM	Current on VDD during Erase/Write	_		5.0	mA		
		Data EEPROM Memory						
D116	ED	Byte Endurance	100K	—	_	E/W	-40°C to +85°C	
D117	VDRW	VDD for Read/Write	VDDMIN	—	VDDMAX	V		
D118	TDEW	Erase/Write Cycle Time	—	4.0	5.0	ms		
D119	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated	
D120	TREF	Number of Total Erase/Write Cycles before Refresh ⁽²⁾	100k	—	—	E/W	-40°C to +85°C	
		Program Flash Memory						
D121	EР	Cell Endurance	10K	—	-	E/W	-40°C to +85°C (Note 1)	
D122	Vpr	VDD for Read	VDDMIN	—	VDDMAX	V		
D123	Tiw	Self-timed Write Cycle Time	—	2	2.5	ms		
D124	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated	

Standard Operating Conditions (unless otherwise stated)

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Refer to Section 12.2 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.

PIC16(L)F1784/6/7

Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 31-79: ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 1μ S, 25° C.



FIGURE 31-80: ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 4μ S, 25° C.



FIGURE 31-81: ADC 10-bit Mode, Single-Ended DNL, VDD = 3.0V, VREF = 3.0V.



FIGURE 31-83: ADC 10-bit Mode, Single-Ended DNL, VDD = 3.0V, $TAD = 1 \mu S$.



FIGURE 31-82: ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, VREF = 3.0V.



Single-Ended INL, VDD = 3.0V, $TaD = 1 \ \mu$ S.

PIC16(L)F1784/6/7

Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 31-85: ADC 12-bit Mode, Single-Ended DNL, VDD = 3.0V, TAD = 1μ S, 25° C.



FIGURE 31-86: ADC 12-bit Mode, Single-Ended DNL, VDD = 3.0V, TAD = 4μ S, 25° C.



FIGURE 31-87: ADC 12-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 1μ S, 25° C.



FIGURE 31-88: ADC 12-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 4μ S, 25° C.



Single-Ended DNL, VDD = 3.0V, VREF = 3.0V.





44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

·						
	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Contact Pitch	E	0.80 BSC				
Contact Pad Spacing	C1		11.40			
Contact Pad Spacing	C2		11.40			
Contact Pad Width (X44)	X1			0.55		
Contact Pad Length (X44)	Y1			1.50		
Distance Between Pads	G	0.25				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B