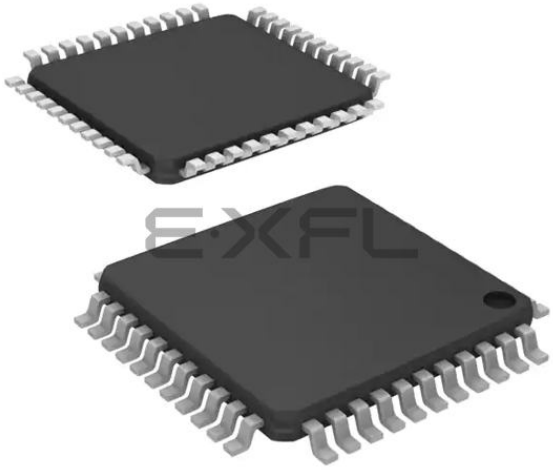

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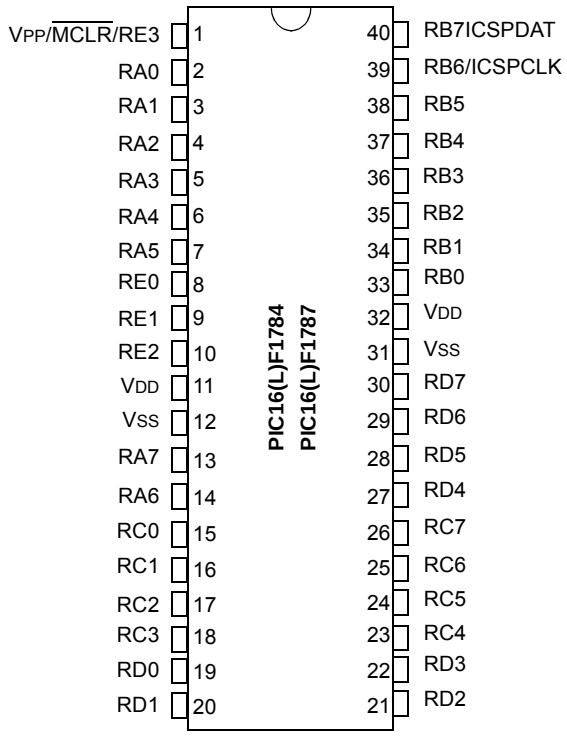
Applications of "Embedded - Microcontrollers"

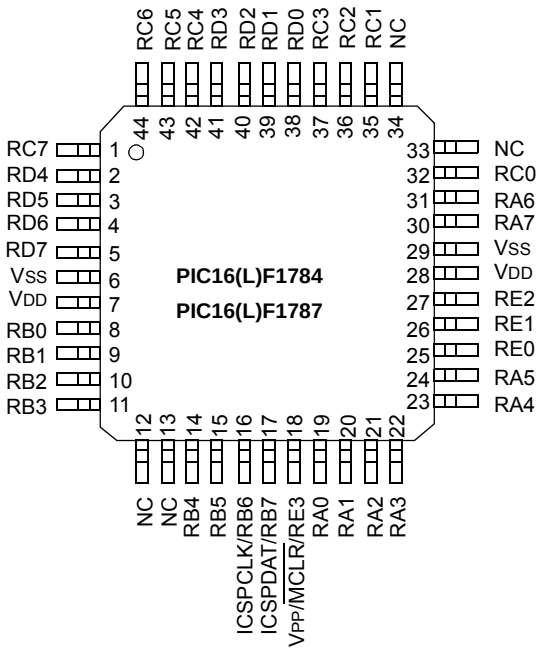
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1784-i-pt

Pin Diagram – 40-Pin PDIP



Note: See Table 2 for the location of all peripheral functions.

Pin Diagram – 44-Pin TQFP



Note: See Table 2 for the location of all peripheral functions.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ C3IN0-/C4IN0-	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	C3IN0-	AN	—	Comparator C3 negative input.
	C4IN0-	AN	—	Comparator C4 negative input.
RA1/AN1/C1IN1-/C2IN1-/ C3IN1-/C4IN1-/OPA1OUT	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	C3IN1-	AN	—	Comparator C3 negative input.
	C4IN1-	AN	—	Comparator C4 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
RA2/AN2/C1IN0+/C2IN0+/ C3IN0+/C4IN0+/DAC1OUT1/ V_{REF}-/DAC1V_{REF}-/OPA1IN-	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	C2IN0+	AN	—	Comparator C2 positive input.
	C3IN0+	AN	—	Comparator C3 positive input.
	C4IN0+	AN	—	Comparator C4 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	V_{REF}-	AN	—	ADC Negative Voltage Reference input.
	DAC1V_{REF}-	AN	—	Digital-to-Analog Converter negative reference.
RA3/AN3/V_{REF}+/C1IN1+/ DAC1V_{REF}+	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	V_{REF}+	AN	—	ADC Voltage Reference input.
	C1IN1+	AN	—	Comparator C1 positive input.
	DAC1V_{REF}+	AN	—	Digital-to-Analog Converter positive reference.
RA4/C1OUT/OPA1IN+/T0CKI	RA4	TTL/ST	CMOS	General purpose I/O.
	C1OUT	—	CMOS	Comparator C1 output.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/C2OUT(1)/OPA1IN-/ $\overline{SS}$	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	C2OUT	—	CMOS	Comparator C2 output.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	$\overline{SS}$	ST	—	Slave Select input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

TABLE 3-10: PIC16(L)F1784/6/7 MEMORY MAP (BANK 16 DETAILS)

	BANK 16		BANK 16		BANK 16
811h	PSMC1CON	831h	PSMC2CON	851h	PSMC3CON
812h	PSMC1MDL	832h	PSMC2MDL	852h	PSMC3MDL
813h	PSMC1SYNC	833h	PSMC2SYNC	853h	PSMC3SYNC
814h	PSMC1CLK	834h	PSMC2CLK	854h	PSMC3CLK
815h	PSMC1OEN	835h	PSMC2OEN	855h	PSMC3OEN
816h	PSMC1POL	836h	PSMC2POL	856h	PSMC3POL
817h	PSMC1BLNK	837h	PSMC2BLNK	857h	PSMC3BLNK
818h	PSMC1REBS	838h	PSMC2REBS	858h	PSMC3REBS
819h	PSMC1FEBS	839h	PSMC2FEBS	859h	PSMC3FEBS
81Ah	PSMC1PHS	83Ah	PSMC2PHS	85Ah	PSMC3PHS
81Bh	PSMC1DCS	83Bh	PSMC2DCS	85Bh	PSMC3DCS
81Ch	PSMC1PRS	83Ch	PSMC2PRS	85Ch	PSMC3PRS
81Dh	PSMC1ASDC	83Dh	PSMC2ASDC	85Dh	PSMC3ASDC
81Eh	PSMC1ASDD	83Eh	PSMC2ASDD	85Eh	PSMC3ASDD
81Fh	PSMC1ASDS	83Fh	PSMC2ASDS	85Fh	PSMC3ASDS
820h	PSMC1INT	840h	PSMC2INT	860h	PSMC3INT
821h	PSMC1PHL	841h	PSMC2PHL	861h	PSMC3PHL
822h	PSMC1PHH	842h	PSMC2PHH	862h	PSMC3PHH
823h	PSMC1DCL	843h	PSMC2DCL	863h	PSMC3DCL
824h	PSMC1DCH	844h	PSMC2DCH	864h	PSMC3DCH
825h	PSMC1PRL	845h	PSMC2PRL	865h	PSMC3PRL
826h	PSMC1PRH	846h	PSMC2PRH	866h	PSMC3PRH
827h	PSMC1TMRL	847h	PSMC2TMRL	867h	PSMC3TMRL
828h	PSMC1TMRH	848h	PSMC2TMRH	868h	PSMC3TMRH
829h	PSMC1DBR	849h	PSMC2DBR	869h	PSMC3DBR
82Ah	PSMC1DBF	84Ah	PSMC2DBF	86Ah	PSMC3DBF
82Bh	PSMC1BLKR	84Bh	PSMC2BLKR	86Bh	PSMC3BLKR
82Ch	PSMC1BLKF	84Ch	PSMC2BLKF	86Ch	PSMC3BLKF
82Dh	PSMC1FFA	84Dh	PSMC2FFA	86Dh	PSMC3FFA
82Eh	PSMC1STR0	84Eh	PSMC2STR0	86Eh	PSMC3STR0
82Fh	PSMC1STR1	84Fh	PSMC2STR1	86Fh	PSMC3STR1
830h	—	850h	—	870h	—

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0											
00Ch	PORTA	PORTA Data Latch when written: PORTA pins when read								xxxx xxxx	uuuu uuuu
00Dh	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
00Eh	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
00Fh	PORTD(3)	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
010h	PORTE	—	—	—	—	RE3	RE2(3)	RE1(3)	RE0(3)	---- xxxx	---- uuuu
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	0000 0-00	0000 0-00
13h	PIR3	—	—	—	CCP3IF	—	—	—	—	---0 ----	0000 0000
014h	PIR4	—	PSMC3TIF	PSMC2TIF	PSMC1TIF	—	PSMC3SIF	PSMC2SIF	PSMC1SIF	-000 -000	-000 -000
015h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
016h	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
017h	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
018h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		0000 0x00	uuuu uxuu
016h	TMR2	Holding Register for the Least Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
017h	PR2	Holding Register for the Most Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
018h	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
01Dh to 01Fh	—	Unimplemented								—	—
Bank 1											
08Ch	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
08Dh	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
08Eh	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
08Fh	TRISD(3)	PORTD Data Direction Register								1111 1111	1111 1111
090h	TRISE	—	—	—	—	—(2)	TRISE2(3)	TRISE1(3)	TRISE0(3)	---- 1111	---- 1111
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
092h	PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	0000 0-00	0000 0-00
093h	PIE3	—	—	—	CCP3IE	—	—	—	—	---0 ----	0000 0000
094h	PIE4	—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE	-000 -000	-000 -000
095h	OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	00-1 11qq	qq-q qquu
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
098h	OSCTUNE	—	—	TUN<5:0>						--00 0000	--00 0000
099h	OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		0011 1-00	0011 1-00
09Ah	OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	00q0 --00	qqqq --0q
09Bh	ADRESL	A/D Result Register Low								xxxx xxxx	uuuu uuuu
09Ch	ADRESH	A/D Result Register High								xxxx xxxx	uuuu uuuu
09Dh	ADCON0	ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
09Eh	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
09Fh	ADCON2	TRIGSEL<3:0>				CHSN<3:0>				000- -000	000- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 16 (Continued)											
851h	PSMC3CON	PSMC3EN	PSMC3LD	P3DBFE	P3DBRE	P3MODE<3:0>				0000 0000	0000 0000
852h	PSMC3MDL	P3MDLEN	P3MDLPOL	P3MDLBIT	—	P3MSRC<3:0>				000- 0000	000- 0000
853h	PSMC3SYNC	P3POFST	P3PRPOL	P3DCPOL	—	—	—	P3SYNC<1:0>		000- --00	000- --00
854h	PSMC3CLK	—	—	P3CPRE<1:0>		—	—	P3CSRC<1:0>		--00 --00	--00 --00
855h	PSMC3OEN	—	—	—	—	—	—	P3OEB	P3OEA	---- --00	---- --00
856h	PSMC3POL	—	P3INPOL	—	—	—	—	P3POLB	P3POLA	-0-- --00	-0-- --00
857h	PSMC3BLNK	—	—	P3FEBM<1:0>		—	—	P3REBM<1:0>		--00 --00	--00 --00
858h	PSMC3REBS	P3REBSIN	—	—	P3REBSC4	P3REBSC3	P3REBSC2	P3REBSC1	—	0--0 000-	0--0 000-
859h	PSMC3FEBS	P3FEBSIN	—	—	P3FEBSC4	P3FEBSC3	P3FEBSC2	P3FEBSC1	—	0--0 000-	0--0 000-
85Ah	PSMC3PHS	P3PHSIN	—	—	P3PHSC4	P3PHSC3	P3PHSC2	P3PHSC1	P3PHST	0--0 0000	0--0 0000
85Bh	PSMC3DCS	P3DCSIN	—	—	P3DCSC4	P3DCSC3	P3DCSC2	P3DCSC1	P3DCST	0--0 0000	0--0 0000
85Ch	PSMC3PRS	P3PRSIN	—	—	P3PRSC4	P3PRSC3	P3PRSC2	P3PRSC1	P3PRST	0--0 0000	0--0 0000
85Dh	PSMC3ASDC	P3ASE	P3ASDEN	P3ARSEN	—	—	—	—	P3ASDOV	000- ---0	000- ---0
85Eh	PSMC3ASDL	—	—	—	—	—	—	P3ASDLB	P3ASDLA	---- --00	---- --00
85Fh	PSMC3ASDS	P3ASDSIN	—	—	P3ASDSC4	P3ASDSC3	P3ASDSC2	P3ASDSC1	—	0--0 000-	0--0 000-
860h	PSMC3INT	P3TOVIE	P3TPHIE	P3TDCIE	P3TPRIE	P3TOVIF	P3TPHIF	P3TDCIF	P3TPRIF	0000 0000	0000 0000
861h	PSMC3PHL	Phase Low Count								0000 0000	0000 0000
862h	PSMC3PHH	Phase High Count								0000 0000	0000 0000
863h	PSMC3DCL	Duty Cycle Low Count								0000 0000	0000 0000
864h	PSMC3DCH	Duty Cycle High Count								0000 0000	0000 0000
865h	PSMC3PRL	Period Low Count								0000 0000	0000 0000
866h	PSMC3PRH	Period High Count								0000 0000	0000 0000
867h	PSMC3TMRL	Time base Low Counter								0000 0001	0000 0001
868h	PSMC3TMRH	Time base High Counter								0000 0000	0000 0000
869h	PSMC3DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
86Ah	PSMC3DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
86Bh	PSMC3BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
86Ch	PSMC3BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
86Dh	PSMC3FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
86Eh	PSMC3STR0	—	—	—	—	—	—	P3STRB	P3STRA	---- --01	---- --01
86Fh	PSMC3STR1	P3SSYNC	—	—	—	—	—	P3LSMEN	P3HSMEN	0--- --00	0--- --00
Bank 17-30											
x0Ch or x8Ch to x1Fh or x9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

4.2 Register Definitions: Configuration Words

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		$\overline{\text{CPD}}$
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor and internal/external switchover are both enabled.
0 = Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
If FOSC configuration bits are set to LP, XT, HS modes:
This bit is ignored, CLKOUT function is disabled. Oscillator function on the CLKOUT pin.
All other FOSC modes:
1 = CLKOUT function is disabled. I/O function on the CLKOUT pin.
0 = CLKOUT function is enabled on the CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the BORCON register
00 = BOR disabled

bit 8 **$\overline{\text{CPD}}$:** Data Code Protection bit(1)
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 7 **$\overline{\text{CP}}$:** Code Protection bit
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/V_{PP} Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{\text{MCLR}}$/V_{PP} pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/V_{PP} pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUE3 bit.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

REGISTER 8-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6 **PSMC3TIE:** PSMC3 Time Base Interrupt Enable bit
- 1 = Enables PSMC3 time base generated interrupts
- 0 = Disables PSMC3 time base generated interrupts

bit 5 **PSMC2TIE:** PSMC2 Time Base Interrupt Enable bit
- 1 = Enables PSMC2 time base generated interrupts
- 0 = Disables PSMC2 time base generated interrupts

bit 4 **PSMC1TIE:** PSMC1 Time Base Interrupt Enable bit
- 1 = Enables PSMC1 time base generated interrupts
- 0 = Disables PSMC1 time base generated interrupts

bit 3 **Unimplemented:** Read as '0'

bit 2 **PSMC3SIE:** PSMC3 Auto-Shutdown Interrupt Enable bit
- 1 = Enables PSMC3 auto-shutdown interrupts
- 0 = Disables PSMC3 auto-shutdown interrupts

bit 1 **PSMC2SIE:** PSMC2 Auto-Shutdown Interrupt Enable bit
- 1 = Enables PSMC2 auto-shutdown interrupts
- 0 = Disables PSMC2 auto-shutdown interrupts

bit 0 **PSMC1SIE:** PSMC1 Auto-Shutdown Interrupt Enable bit
- 1 = Enables PSMC1 auto-shutdown interrupts
- 0 = Disables PSMC1 auto-shutdown interrupts

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

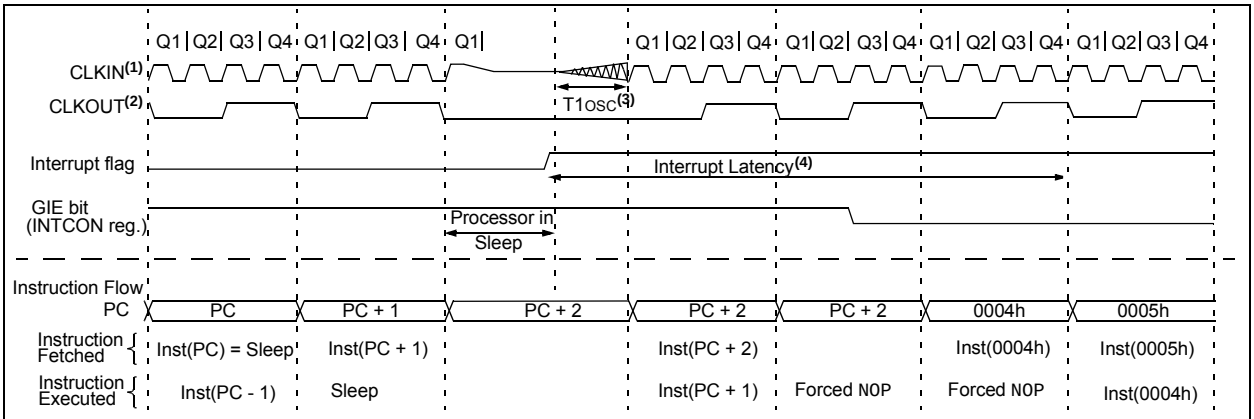
9.1.1 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction
  - SLEEP instruction will execute as a NOP.
  - WDT and WDT prescaler will not be cleared
  - $\overline{TO}$ bit of the STATUS register will not be set
  - $\overline{PD}$ bit of the STATUS register will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction
  - SLEEP instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - $\overline{TO}$ bit of the STATUS register will be set
  - $\overline{PD}$ bit of the STATUS register will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

FIGURE 9-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: External clock. High, Medium, Low mode assumed.
2: CLKOUT is shown here for timing reference.
3: T1OSC; See **Section 30.0 "Electrical Specifications"**.
4: GIE = 1 assumed. In this case after wake-up, the processor calls the ISR at 0004h. If GIE = 0, execution will continue in-line.

12.7 Register Definitions: EEPROM and Flash Control

REGISTER 12-1: EEDATL: EEPROM DATA LOW BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
EEDAT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **EEDAT<7:0>**: Read/write value for EEPROM data byte or Least Significant bits of program memory

REGISTER 12-2: EEDATH: EEPROM DATA HIGH BYTE REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	EEDAT<13:8>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **EEDAT<13:8>**: Read/write value for Most Significant bits of program memory

REGISTER 12-3: EEADRL: EEPROM ADDRESS REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EEADR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **EEADR<7:0>**: Specifies the Least Significant bits for program memory address or EEPROM address

REGISTER 12-4: EEADRH: EEPROM ADDRESS HIGH BYTE REGISTER

U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—(1)	EEADR<14:8>						
bit 7							bit 0

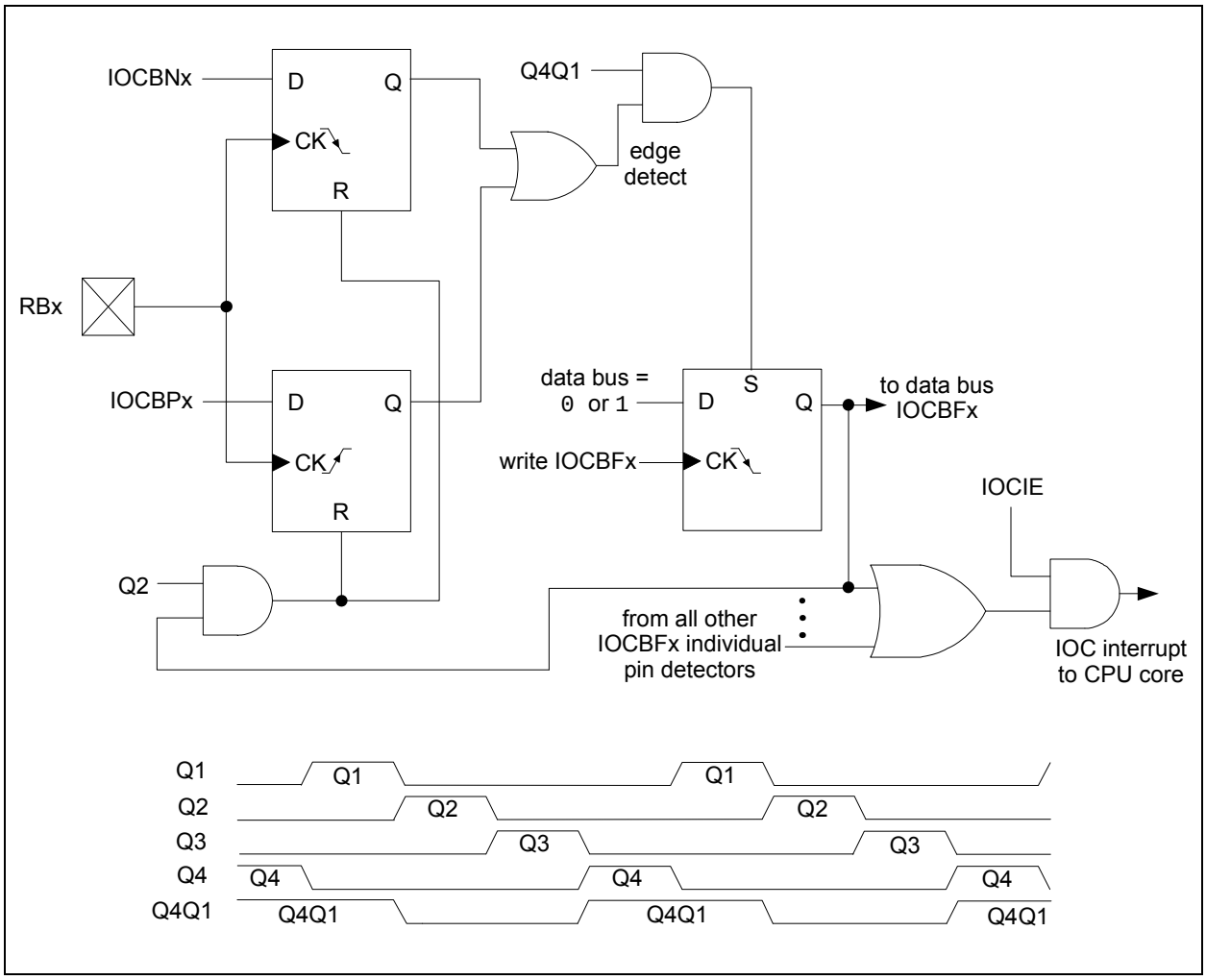
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '1'

bit 6-0 **EEADR<14:8>**: Specifies the Most Significant bits for program memory address or EEPROM address

Note 1: Unimplemented, read as '1'.

FIGURE 14-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM



17.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2:	The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

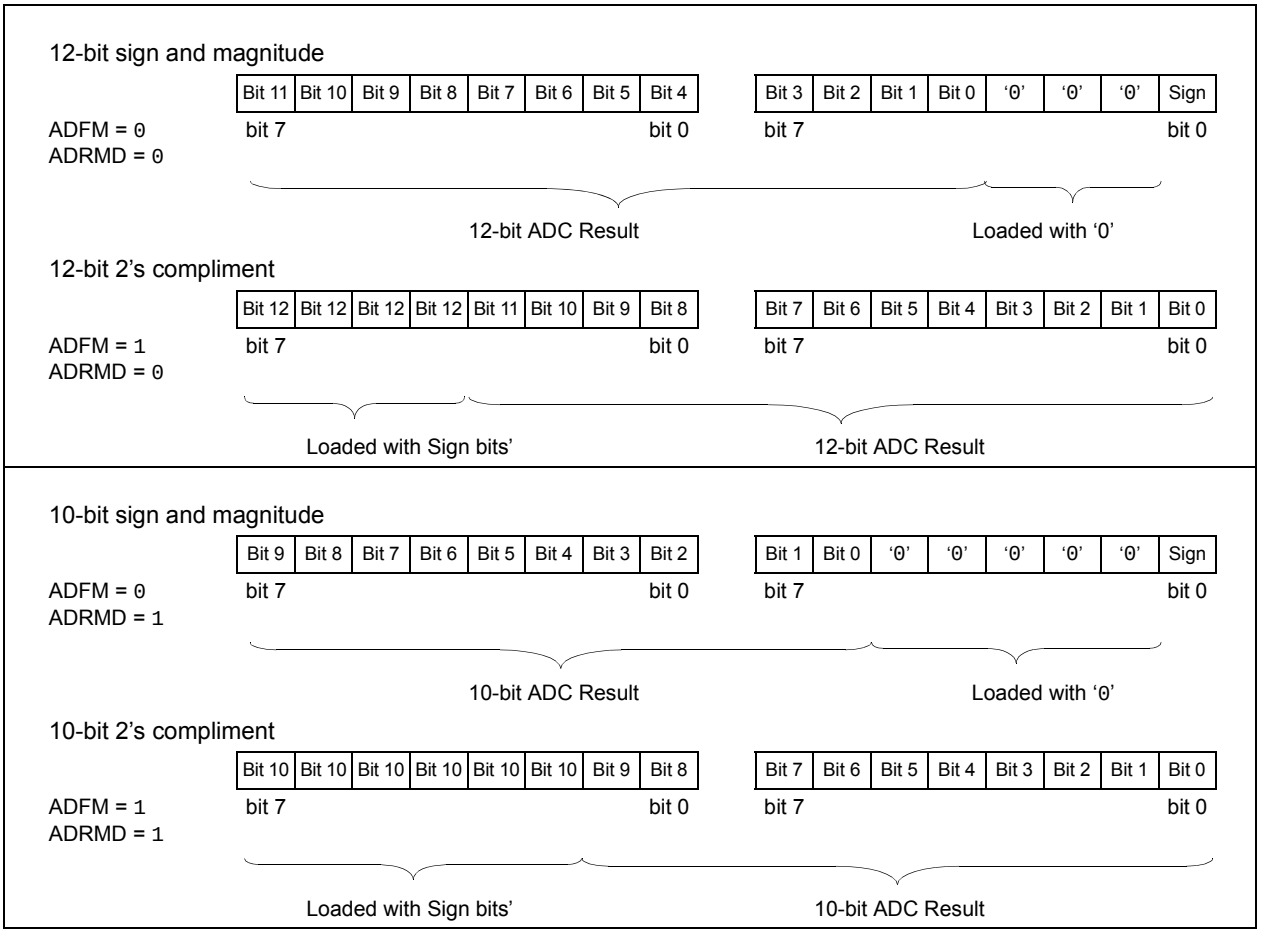
17.1.6 RESULT FORMATTING

The 10-bit and 12-bit ADC conversion results can be supplied in two formats: 2's complement or sign-magnitude. The ADFM bit of the ADCON1 register controls the output format. Sign magnitude is left justified with the sign bit in the LSb position. Negative numbers are indicated when the sign bit is '1'.

Two's complement is right justified with the sign extended into the Most Significant bits.

Figure 17-3 shows the two output formats. Table 17-2 shows conversion examples.

FIGURE 17-3: ADC CONVERSION RESULT FORMAT



20.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

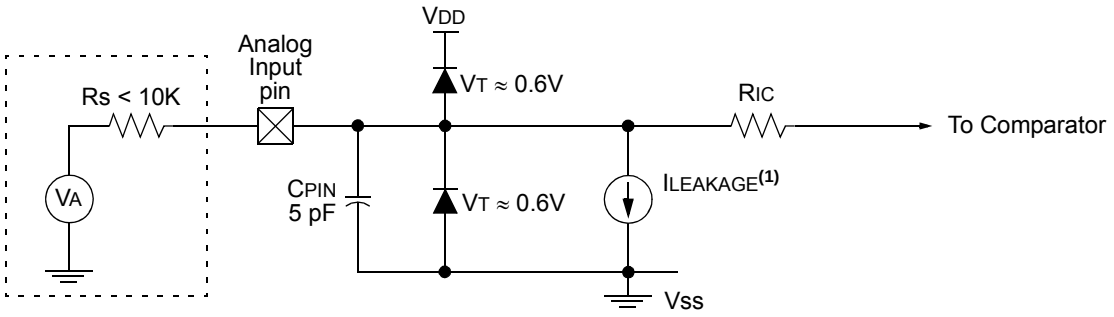
A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1:	When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
2:	Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

20.10.1 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 "Alternate Pin Function"** for more information.

FIGURE 20-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

Note 1: See **Section 30.0 "Electrical Specifications"**

FIGURE 22-5: TIMER1 GATE SINGLE-PULSE MODE

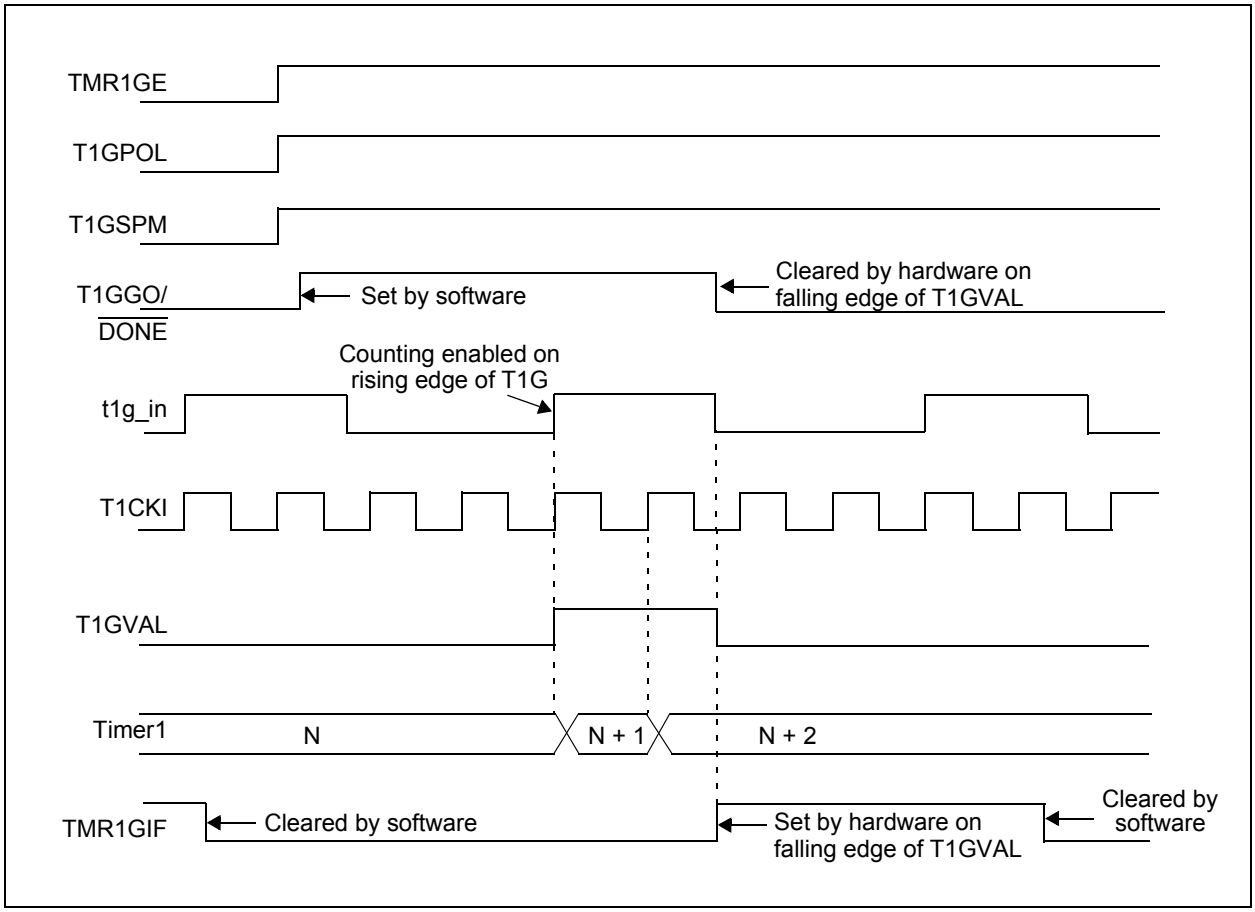


TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				280
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PR2	Timer2 Module Period Register								210*
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		212
TMR2	Holding Register for the 8-bit TMR2 Register								210*

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

* Page provides register information.

24.3.5 PUSH-PULL PWM WITH FOUR FULL-BRIDGE OUTPUTS

The full-bridge push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge.

24.3.5.1 Mode Features

- No Dead-band control
- No Steering control available
- PWM is output on the following four pins only:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD

Note: PSMCxA and PSMCxC are identical waveforms, and PSMCxB and PSMCxD are identical waveforms.

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See **Section 24.3.6 "Push-Pull PWM with Four Full-Bridge and Complementary Outputs"**.

24.3.5.2 Waveform generation

Push-pull waveforms generate alternating outputs on the output pairs. Therefore, there are two sets of rising edge events and two sets of falling edge events.

Odd numbered period rising edge event:

- PSMCxOUT0 and PSMCxOUT2 is set active

Odd numbered period falling edge event:

- PSMCxOUT0 and PSMCxOUT2 is set inactive

Even numbered period rising edge event:

- PSMCxOUT1 and PSMCxOUT3 is set active

Even numbered period falling edge event:

- PSMCxOUT1 and PSMCxOUT3 is set inactive

FIGURE 24-8: PUSH-PULL PWM WITH 4 FULL-BRIDGE OUTPUTS

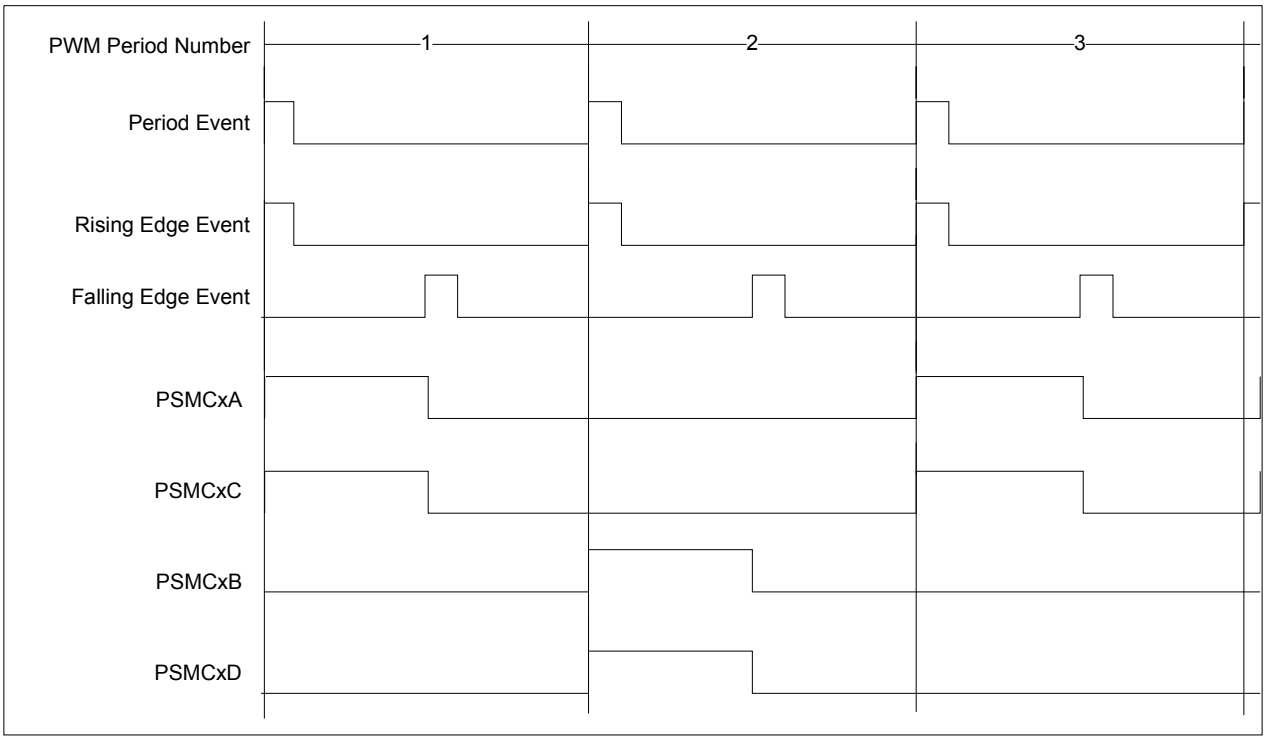


TABLE 30-2: SUPPLY VOLTAGE (I_{DD})(1,2)

PIC16LF1784/6/7			Standard Operating Conditions (unless otherwise stated)				
PIC16F1784/6/7							
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						V_{DD}	Note
D009	LDO Regulator	—	75	—	µA	—	High Power mode, normal operation
		—	15	—	µA	—	Sleep VREGCON<1> = 0
		—	0.3	—	µA	—	Sleep VREGCON<1> = 1
D010		—	8	20	µA	1.8	F_{OSC} = 32 kHz LP Oscillator mode **(Note 4)**, -40°C ≤ T_A ≤ +85°C
		—	12	24	µA	3.0	
D010		—	18	63	µA	2.3	F_{OSC} = 32 kHz LP Oscillator mode **(Note 4, 5)**, -40°C ≤ T_A ≤ +85°C
		—	20	74	µA	3.0	
		—	22	79	µA	5.0	
D012		—	160	650	µA	1.8	F_{OSC} = 4 MHz XT Oscillator mode
		—	320	1000	µA	3.0	
D012		—	260	700	µA	2.3	F_{OSC} = 4 MHz XT Oscillator mode **(Note 5)**
		—	330	1100	µA	3.0	
		—	380	1300	µA	5.0	

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

4: FVR and BOR are disabled.

5: 0.1 µF capacitor on V_{CAP}.

6: 8 MHz crystal oscillator with 4x PLL enabled.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

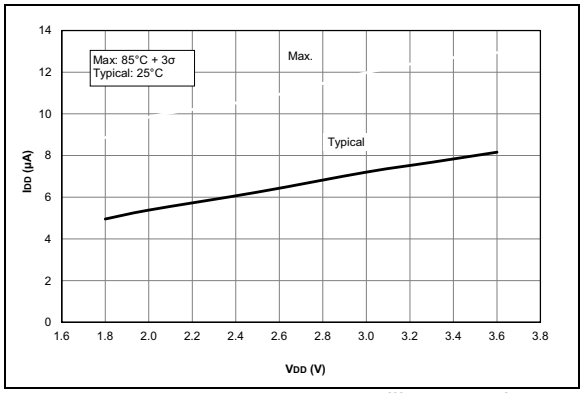


FIGURE 31-1: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16LF1784/6/7 Only.*

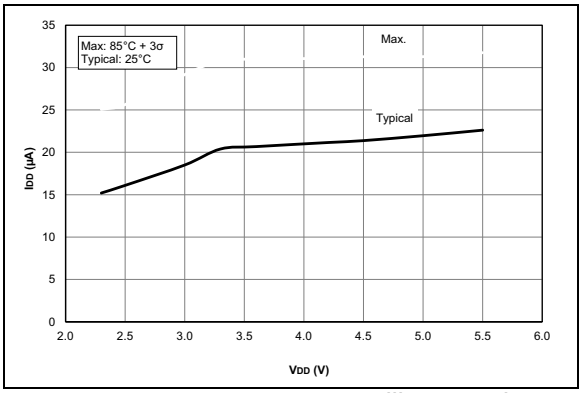


FIGURE 31-2: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16F1784/6/7 Only.*

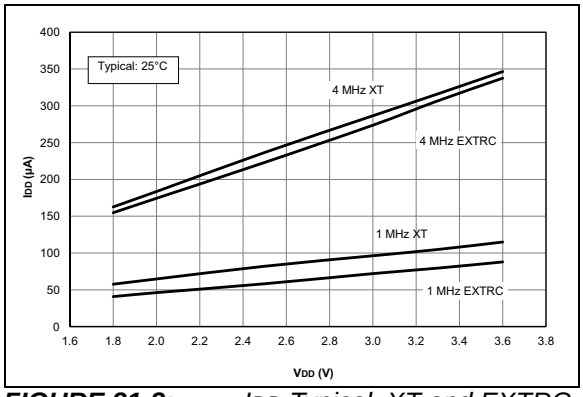


FIGURE 31-3: *IDD Typical, XT and EXTRC Oscillator, PIC16LF1784/6/7 Only.*

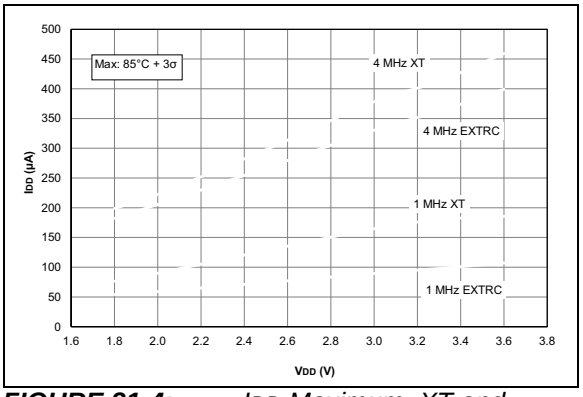


FIGURE 31-4: *IDD Maximum, XT and EXTRC Oscillator, PIC16LF1784/6/7 Only.*

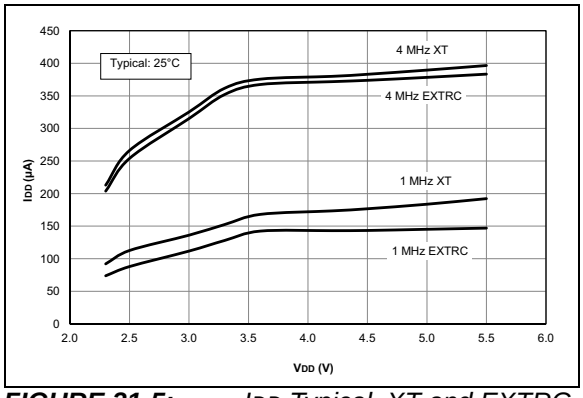


FIGURE 31-5: *IDD Typical, XT and EXTRC Oscillator, PIC16F1784/6/7 Only.*

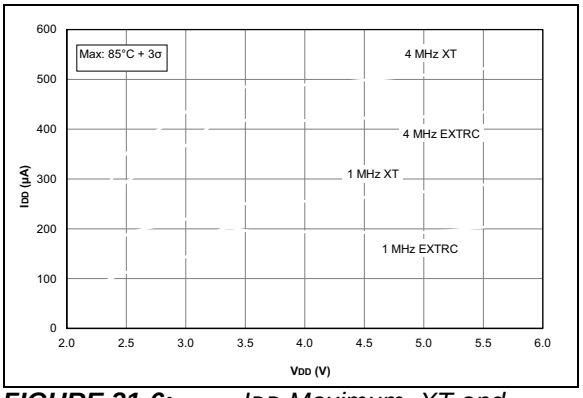


FIGURE 31-6: *IDD Maximum, XT and EXTRC Oscillator, PIC16F1784/6/7 Only.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

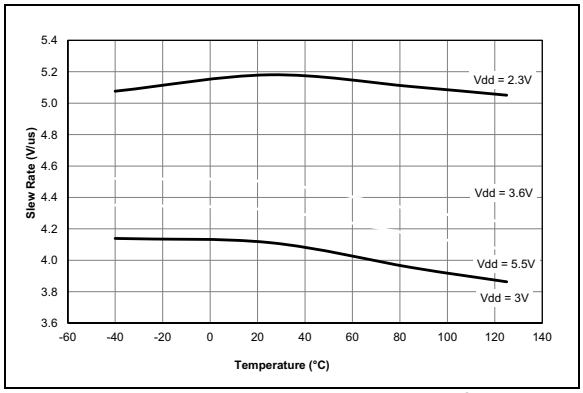


FIGURE 31-115: *Op Amp, Output Slew Rate, Falling Edge, PIC16F1784/6/7 Only.*

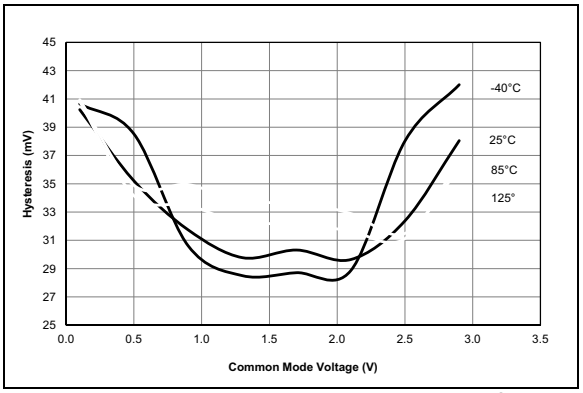


FIGURE 31-116: *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values.*

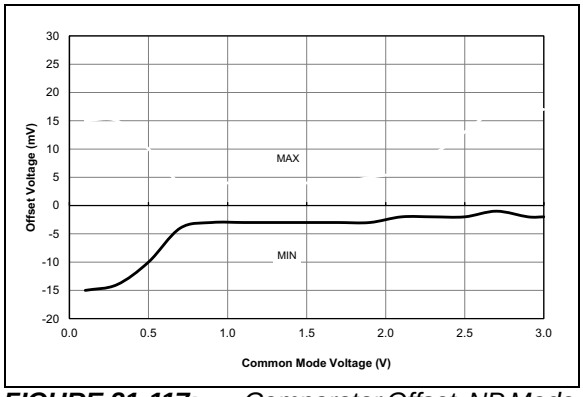


FIGURE 31-117: *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values at 25°C.*

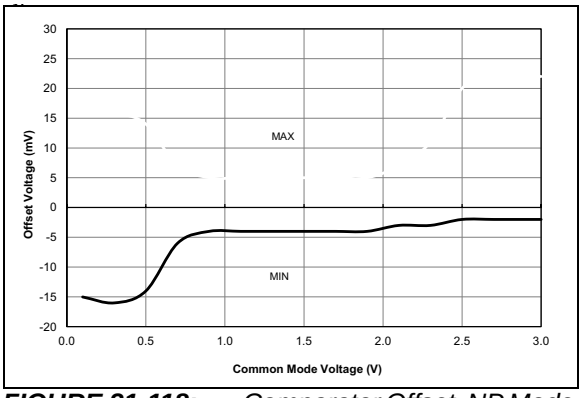


FIGURE 31-118: *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values From -40°C to 125°C.*

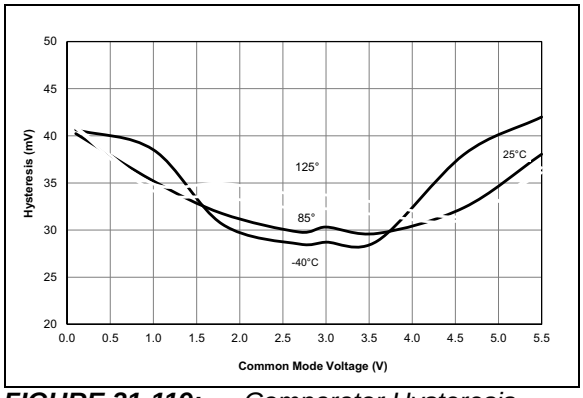
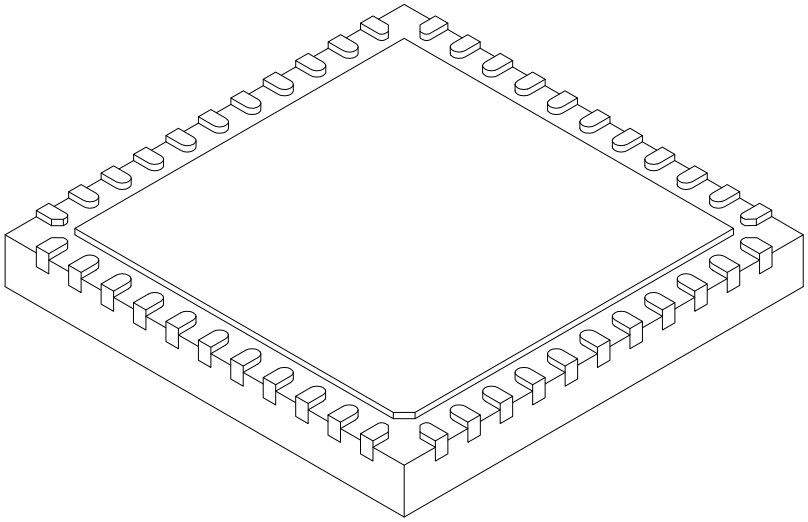


FIGURE 31-119: *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 5.5V, Typical Measured Values, PIC16F1784/6/7 Only.*

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2