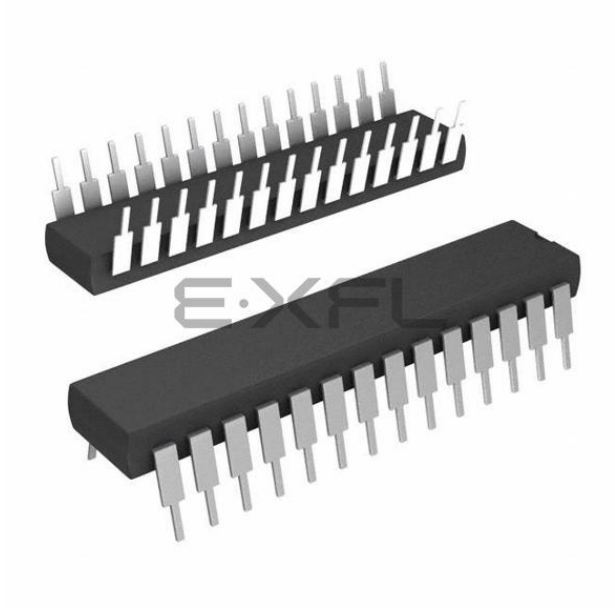

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1786-i-sp

TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1784/7)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Op Amps	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	17	19	19	AN0	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	—	IOC	Y	—
RA1	3	18	20	20	AN1	—	C1IN1- C2IN1- C3IN1- C4IN1-	OPA1OUT	—	—	—	—	—	—	IOC	Y	—
RA2	4	19	21	21	AN2	DAC1VREF- VREF-	C1IN0+ C2IN0+ C3IN0+ C4IN0+		DAC1OUT1	—	—	—	—	—	IOC	Y	—
RA3	5	20	22	22	AN3	DAC1VREF+ VREF+	C1IN1+	—	—	—	—	—	—	—	IOC	Y	—
RA4	6	21	23	23	—	—	C1OUT	OPA1IN+	—	T0CKI	—	—	—	—	IOC	Y	—
RA5	7	22	24	24	AN4	—	C2OUT	OPA1IN-	—	—	—	—	—	$\overline{SS}$	IOC	Y	—
RA6	14	29	31	33	—	—	C2OUT(1)	—	—	—	—	—	—	—	IOC	Y	VCAP CLKOUT OSC2
RA7	13	28	30	32	—	—	—	—	—	—	PSMC1CLK PSMC2CLK PSMC3CLK	—	—	—	IOC	Y	CLKIN OSC1
RB0	33	8	8	9	AN12	—	C2IN1+	—	—	—	PSMC1IN PSMC2IN PSMC3IN	CCP1(1)	—	—	INT IOC	Y	—
RB1	34	9	9	10	AN10	—	C1IN3- C2IN3- C3IN3- C4IN3-	OPA2OUT	—	—	—	—	—	—	IOC	Y	—
RB2	35	10	10	11	AN8	—	—	OPA2IN-	—	—	—	—	—	—	IOC	Y	CLKR
RB3	36	11	11	12	AN9	—	C1IN2- C2IN2- C3IN2-	OPA2IN+	—	—	—	CCP2(1)	—	—	IOC	Y	—
RB4	37	12	14	14	AN11	—	C3IN1+	—	—	—	—	—	—	—	IOC	Y	—
RB5	38	13	15	15	AN13	—	C4IN2-	—	—	T1G	—	CCP3(1)	—	SDO(1)	IOC	Y	—
RB6	39	14	16	16	—	—	C4IN1+	—	—	—	—	—	TX(1) CK(1)	SDA(1) SDI(1)	IOC	Y	ICSPCLK
RB7	40	15	17	17	—	—	—	—	DAC1OUT2	—	—	—	RX(1) DT(1)	SCL(1) SCK(1)	IOC	Y	ICSPDAT
RC0	15	30	32	34	—	—	—	—	—	T1CKI T1OSO	PSMC1A	—	—	—	IOC	Y	—

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0											
00Ch	PORTA	PORTA Data Latch when written: PORTA pins when read								xxxx xxxx	uuuu uuuu
00Dh	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
00Eh	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
00Fh	PORTD(3)	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
010h	PORTE	—	—	—	—	RE3	RE2(3)	RE1(3)	RE0(3)	---- xxxx	---- uuuu
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	0000 0-00	0000 0-00
13h	PIR3	—	—	—	CCP3IF	—	—	—	—	---0 ----	0000 0000
014h	PIR4	—	PSMC3TIF	PSMC2TIF	PSMC1TIF	—	PSMC3SIF	PSMC2SIF	PSMC1SIF	-000 -000	-000 -000
015h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
016h	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
017h	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
018h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		0000 0x00	uuuu uxuu
016h	TMR2	Holding Register for the Least Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
017h	PR2	Holding Register for the Most Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
018h	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
01Dh to 01Fh	—	Unimplemented								—	—
Bank 1											
08Ch	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
08Dh	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
08Eh	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
08Fh	TRISD(3)	PORTD Data Direction Register								1111 1111	1111 1111
090h	TRISE	—	—	—	—	—(2)	TRISE2(3)	TRISE1(3)	TRISE0(3)	---- 1111	---- 1111
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
092h	PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	0000 0-00	0000 0-00
093h	PIE3	—	—	—	CCP3IE	—	—	—	—	---0 ----	0000 0000
094h	PIE4	—	PSMC3TIE	PSMC2TIE	PSMC1TIE	—	PSMC3SIE	PSMC2SIE	PSMC1SIE	-000 -000	-000 -000
095h	OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	00-1 11qq	qq-q qquu
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
098h	OSCTUNE	—	—	TUN<5:0>						--00 0000	--00 0000
099h	OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		0011 1-00	0011 1-00
09Ah	OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	00q0 --00	qqqq --0q
09Bh	ADRESL	A/D Result Register Low								xxxx xxxx	uuuu uuuu
09Ch	ADRESH	A/D Result Register High								xxxx xxxx	uuuu uuuu
09Dh	ADCON0	ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
09Eh	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
09Fh	ADCON2	TRIGSEL<3:0>				CHSN<3:0>				000- -000	000- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 16											
80Ch — 810h	—	Unimplemented								—	—
811h	PSMC1CON	PSMC1EN	PSMC1LD	PSMC1DBFE	PSMC1DBRE	P1MODE<3:0>				0000 0000	0000 0000
812h	PSMC1MDL	P1MDLEN	P1MDLPOL	P1MDLBIT	—	P1MSRC<3:0>				000- 0000	000- 0000
813h	PSMC1SYNC	P1POFST	P1PRPOL	P1DCPOL	—	—	—	P1SYNC<1:0>		000- --00	000- --00
814h	PSMC1CLK	—	—	P1CPRE<1:0>		—	—	P1CSRC<1:0>		--00 --00	--00 --00
815h	PSMC1OEN	—	—	P1OEF	P1OEE	P1OED	P1OEC	P1OEB	P1OEA	--00 0000	--00 0000
816h	PSMC1POL	—	P1INPOL	P1POLF	P1POLE	P1POLD	P1POLC	P1POLB	P1POLA	-000 0000	-000 0000
817h	PSMC1BLNK	—	—	P1FEBM<1:0>		—	—	P1REBM<1:0>		--00 --00	--00 --00
818h	PSMC1REBS	P1REBIN	—	—	P1REBSC4	P1REBSC3	P1REBSC2	P1REBSC1	—	0--0 000-	0--0 000-
819h	PSMC1FEBS	P1FEBIN	—	—	P1FEBSC4	P1FEBSC3	P1FEBSC2	P1FEBSC1	—	0--0 000-	0--0 000-
81Ah	PSMC1PHS	P1PHSIN	—	—	P1PHSC4	P1PHSC3	P1PHSC2	P1PHSC1	P1PHST	0--0 0000	0--0 0000
81Bh	PSMC1DCS	P1DCSIN	—	—	P1DCSC4	P1DCSC3	P1DCSC2	P1DCSC1	P1DCST	0--0 0000	0--0 0000
81Ch	PSMC1PRS	P1PRSIN	—	—	P1PRSC4	P1PRSC3	P1PRSC2	P1PRSC1	P1PRST	0--0 0000	0--0 0000
81Dh	PSMC1ASDC	P1ASE	P1ASDEN	P1ARSEN	—	—	—	—	P1ASDOV	000- ---0	000- ---0
81Eh	PSMC1ASDL	—	—	P1ASDLF	P1ASDLE	P1ASDLD	P1ASDLC	P1ASDLB	P1ASDLA	--00 0000	--00 0000
81Fh	PSMC1ASDS	P1ASDSIN	—	—	P1ASDSC4	P1ASDSC3	P1ASDSC2	P1ASDSC1	—	0--0 000-	0--0 000-
820h	PSMC1INT	P1TOVIE	P1TPHIE	P1TDCIE	P1TPRIE	P1TOVIF	P1TPHIF	P1TDCIF	P1TPRIF	0000 0000	0000 0000
821h	PSMC1PHL	Phase Low Count								0000 0000	0000 0000
822h	PSMC1PHH	Phase High Count								0000 0000	0000 0000
823h	PSMC1DCL	Duty Cycle Low Count								0000 0000	0000 0000
824h	PSMC1DCH	Duty Cycle High Count								0000 0000	0000 0000
825h	PSMC1PRL	Period Low Count								0000 0000	0000 0000
826h	PSMC1PRH	Period High Count								0000 0000	0000 0000
827h	PSMC1TMRL	Time base Low Counter								0000 0001	0000 0001
828h	PSMC1TMRH	Time base High Counter								0000 0000	0000 0000
829h	PSMC1DBR	rising Edge Dead-band Counter								0000 0000	0000 0000
82Ah	PSMC1DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
82Bh	PSMC1BLKR	rising Edge Blanking Counter								0000 0000	0000 0000
82Ch	PSMC1BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
82Dh	PSMC1FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
82Eh	PSMC1STR0	—	—	P1STRF	P1STRE	P1STRD	P1STRC	P1STRB	P1STRA	--00 0001	--00 0001
82Fh	PSMC1STR1	P1SYNC	—	—	—	—	—	P1LSMEN	P1HSMEN	0--- --00	0--- --00
830h	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 16 (Continued)											
831h	PSMC2CON	PSMC2EN	PSMC2LD	PSMC2DBFE	PSMC2DBRE	P2MODE<3:0>				0000 0000	0000 0000
832h	PSMC2MDL	P2MDLEN	P2MDLPOL	P2MDLBIT	—	P2MSRC<3:0>				000- 0000	000- 0000
833h	PSMC2SYNC	P2POFST	P2PRPOL	P2DCPOL	—	—	—	P2SYNC<1:0>		000- --00	000- --00
834h	PSMC2CLK	—	—	P2CPRE<1:0>		—	—	P2CSRC<1:0>		--00 --00	--00 --00
835h	PSMC2OEN	—	—	—	—	—	—	P2OEB	P2OEA	---- --00	---- --00
836h	PSMC2POL	—	P2INPOL	—	—	—	—	P2POLB	P2POLA	-0-- --00	-0-- --00
837h	PSMC2BLNK	—	—	P2FEBM<1:0>		—	—	P2REBM<1:0>		--00 --00	--00 --00
838h	PSMC2REBS	P2REBIN	—	—	P2REBSC4	P2REBSC3	P2REBSC2	P2REBSC1	—	0--0 000-	0--0 000-
839h	PSMC2FEBS	P2FEBIN	—	—	P2FEBSC4	P2FEBSC3	P2FEBSC2	P2FEBSC1	—	0--0 000-	0--0 000-
83Ah	PSMC2PHS	P2PHSIN	—	—	P2PHSC4	P2PHSC3	P2PHSC2	P2PHSC1	P2PHST	0--0 0000	0--0 0000
83Bh	PSMC2DCS	P2DCSIN	—	—	P2DCSC4	P2DCSC3	P2DCSC2	P2DCSC1	P2DCST	0--0 0000	0--0 0000
83Ch	PSMC2PRS	P2PRSIN	—	—	P2PRSC4	P2PRSC3	P2PRSC2	P2PRSC1	P2PRST	0--0 0000	0--0 0000
83Dh	PSMC2ASDC	P2ASE	P2ASDEN	P2ARSEN	—	—	—	—	P2ASDOV	000- ---0	000- ---0
83Eh	PSMC2ASDL	—	—	P2ASDLF	P2ASDLE	P2ASDLD	P2ASDLC	P2ASDLB	P2ASDLA	--00 0000	--00 0000
83Fh	PSMC2ASDS	P2ASDSIN	—	—	P2ASDSC4	P2ASDSC3	P2ASDSC2	P2ASDSC1	—	0--0 000-	0--0 000-
840h	PSMC2INT	P2TOVIE	P2TPHIE	P2TDCIE	P2TPRIE	P2TOVIF	P2TPHIF	P2TDCIF	P2TPRIF	0000 0000	0000 0000
841h	PSMC2PHL	Phase Low Count								0000 0000	0000 0000
842h	PSMC2PHH	Phase High Count								0000 0000	0000 0000
843h	PSMC2DCL	Duty Cycle Low Count								0000 0000	0000 0000
844h	PSMC2DCH	Duty Cycle High Count								0000 0000	0000 0000
845h	PSMC2PRL	Period Low Count								0000 0000	0000 0000
846h	PSMC2PRH	Period High Count								0000 0000	0000 0000
847h	PSMC2TMRL	Time base Low Counter								0000 0001	0000 0001
848h	PSMC2TMRH	Time base High Counter								0000 0000	0000 0000
849h	PSMC2DBR	rising Edge Dead-band Counter								0000 0000	0000 0000
84Ah	PSMC2DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
84Bh	PSMC2BLKR	rising Edge Blanking Counter								0000 0000	0000 0000
84Ch	PSMC2BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
84Dh	PSMC2FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
84Eh	PSMC2STR0	—	—	—	—	—	—	P2STRB	P2STRA	---- --01	---- --01
84Fh	PSMC2STR1	P2SYNC	—	—	—	—	—	P2LSMEN	P2HSMEN	0--- --00	0--- --00
850h	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

11.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1 ms. See **Section 30.0 "Electrical Specifications"** for the LFINTOSC tolerances.

11.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 11-1.

11.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to '11', the WDT is always on.

WDT protection is active during Sleep.

11.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to '10', the WDT is on, except in Sleep.

WDT protection is not active during Sleep.

11.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.

WDT protection is unchanged by Sleep. See Table 11-1 for more details.

TABLE 11-1: WDT OPERATING MODES

WDTE<1:0>	SWDTEN	Device Mode	WDT Mode
11	X	X	Active
10	X	Awake	Active
		Sleep	Disabled
01	1	X	Active
	0		Disabled
00	X	X	Disabled

11.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

11.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- Any Reset
- CLRWDT instruction is executed
- Device enters Sleep
- Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
- Oscillator Start-up TImer (OST) is running

See Table 11-2 for more information.

11.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again. The WDT remains clear until the OST, if enabled, completes. See **Section 6.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the event. See **Section 3.0 "Memory Organization"** and Status Register (Register 3-1) for more information.

TABLE 11-2: WDT CLEARING CONDITIONS

Conditions	WDT
WDTE<1:0> = 00	Cleared
WDTE<1:0> = 01 and SWDTEN = 0	
WDTE<1:0> = 10 and enter Sleep	
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST
Change INTOSC divider (IRCF bits)	Unaffected

13.0 I/O PORTS

Each port has three standard registers for its operation. These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELx (analog select)
- WPUx (weak pull-up)

In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

TABLE 13-1: PORT AVAILABILITY PER DEVICE

Device	PORTA	PORTB	PORTC	PORTD	PORTE
PIC16(L)F1786	•	•	•		•
PIC16(L)F1784/7	•	•	•	•	•

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 13-1.

FIGURE 13-1: GENERIC I/O PORT OPERATION

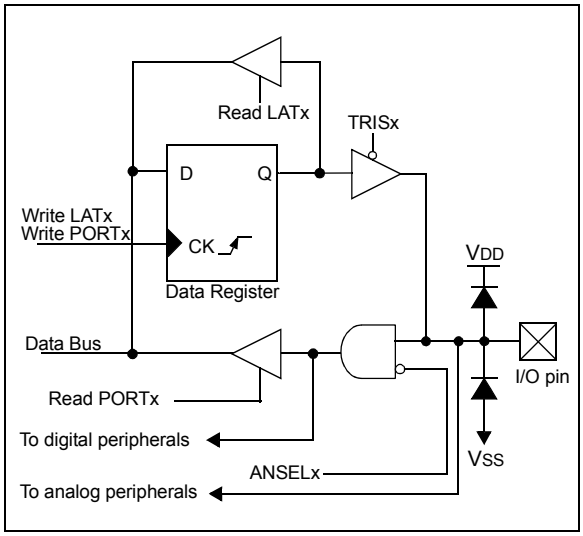


TABLE 13-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELD	—	—	—	—	—	ANSD2	ANSD1	ANSD0	147
INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	148
LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	146
ODCOND	ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0	148
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	146
SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	148
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	146
WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	147

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

14.6 Register Definitions: Interrupt-on-Change Control

REGISTER 14-1: IOCxP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCxP7	IOCxP6	IOCxP5	IOCxP4	IOCxP3	IOCxP2	IOCxP1	IOCxP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **IOCxP<7:0>:** Interrupt-on-Change Positive Edge Enable bits(1)

1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

Note 1: For IOCEP register, bit 3 (IOCEP3) is the only implemented bit in the register.

REGISTER 14-2: IOCxN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCxN7	IOCxN6	IOCxN5	IOCxN4	IOCxN3	IOCxN2	IOCxN1	IOCxN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **IOCxN<7:0>:** Interrupt-on-Change Negative Edge Enable bits(1)

1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

Note 1: For IOCEN register, bit 3 (IOCEN3) is the only implemented bit in the register.

15.4 Register Definitions: FVR Control

REGISTER 15-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY(1)	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **FVREN:** Fixed Voltage Reference Enable bit
1 = Fixed Voltage Reference is enabled
0 = Fixed Voltage Reference is disabled

bit 6 **FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
1 = Fixed Voltage Reference output is ready for use
0 = Fixed Voltage Reference output is not ready or not enabled

bit 5 **TSEN:** Temperature Indicator Enable bit(3)
1 = Temperature Indicator is enabled
0 = Temperature Indicator is disabled

bit 4 **TSRNG:** Temperature Indicator Range Selection bit(3)
1 = $V_{OUT} = V_{DD} - 4V_T$ (High Range)
0 = $V_{OUT} = V_{DD} - 2V_T$ (Low Range)

bit 3-2 CDAFVR<1:0>: Comparator and DAC Fixed Voltage Reference Selection bit
11 = Comparator and DAC Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)
10 = Comparator and DAC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
01 = Comparator and DAC Fixed Voltage Reference Peripheral output is 1x (1.024V)
00 = Comparator and DAC Fixed Voltage Reference Peripheral output is off.

bit 1-0 **ADFVR<1:0>:** ADC Fixed Voltage Reference Selection bit
11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)
10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V)
00 = ADC Fixed Voltage Reference Peripheral output is off.

Note 1: FVRRDY is always '1' on "F" devices only.
2: Fixed Voltage Reference output cannot exceed V_{DD}.
3: See **Section 16.0 "Temperature Indicator Module"** for additional information.

TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		162

Legend: Shaded cells are not used with the Fixed Voltage Reference.

16.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, "*Use and Calibration of the Internal Temperature Indicator*" (DS01333) for more details regarding the calibration process.

16.1 Circuit Operation

Figure 16-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 16-1 describes the output characteristics of the temperature indicator.

EQUATION 16-1: VOUT RANGES

High Range: $V_{OUT} = V_{DD} - 4V_T$

Low Range: $V_{OUT} = V_{DD} - 2V_T$

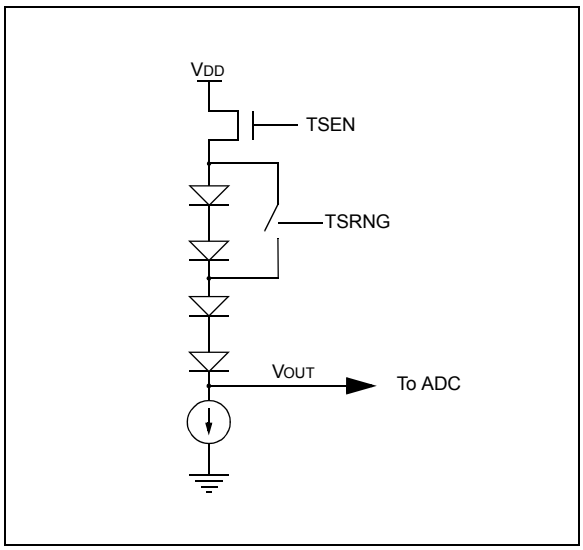
The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 15.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low-voltage operation.

FIGURE 16-1: TEMPERATURE CIRCUIT DIAGRAM



16.2 Minimum Operating VDD

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 16-1 shows the recommended minimum VDD vs. range setting.

TABLE 16-1: RECOMMENDED VDD VS. RANGE

Min. VDD, TSRNG = 1	Min. VDD, TSRNG = 0
3.6V	1.8V

16.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 17.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

16.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.

17.4 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 17-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 17-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 17-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 17-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ *5.0V* V_{DD}

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} \quad ;[1]\ V_{CHOLD}\ \text{charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad ;[2]\ V_{CHOLD}\ \text{charge response to}\ V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \quad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for T_C*:*

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/8191)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.000122)$$
$$= 1.62\mu s$$

Therefore:

$$T_{ACQ} = 2\mu s + 1.62\mu s + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 4.87\mu s$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: Maximum source impedance feeding the input pin should be considered so that the pin leakage does not cause a voltage divider, thereby limiting the absolute accuracy.

18.4 Register Definitions: Op Amp Control

REGISTER 18-1: OPAxCON: OPERATIONAL AMPLIFIERS (OPAx) CONTROL REGISTERS

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
OPAxEN	OPAxSP	—	—	—	—	OPAxCH<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **OPAxEN:** Op Amp Enable bit
1 = Op amp is enabled
0 = Op amp is disabled and consumes no active power

bit 6 **OPAxSP:** Op Amp Speed/Power Select bit
1 = Comparator operates in high GBWP mode
0 = Reserved. Do not use.

bit 5-2 **Unimplemented:** Read as '0'

bit 1-0 **OPAxCH<1:0>:** Non-inverting Channel Selection bits
11 = Non-inverting input connects to FVR Buffer 2 output
10 = Non-inverting input connects to DAC_output
0x = Non-inverting input connects to OPAxIN+ pin

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH OP AMPS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	132
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	138
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	186
DAC1CON1	DAC1R<7:0>								186
OPA1CON	OPA1EN	OPA1SP	—	—	—	—	OPA1PCH<1:0>		182
OPA2CON	OPA2EN	OPA2SP	—	—	—	—	OPA2PCH<1:0>		182
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	131
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	137
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by op amps.
Note 1: PIC16(L)F1784/7 only

20.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

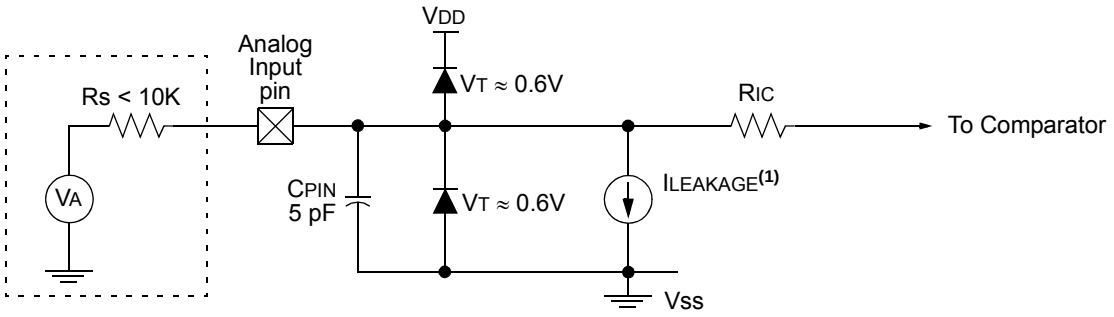
A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1:	When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
2:	Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

20.10.1 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 "Alternate Pin Function"** for more information.

FIGURE 20-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

Note 1: See **Section 30.0 "Electrical Specifications"**

FIGURE 22-3: TIMER1 GATE ENABLE MODE

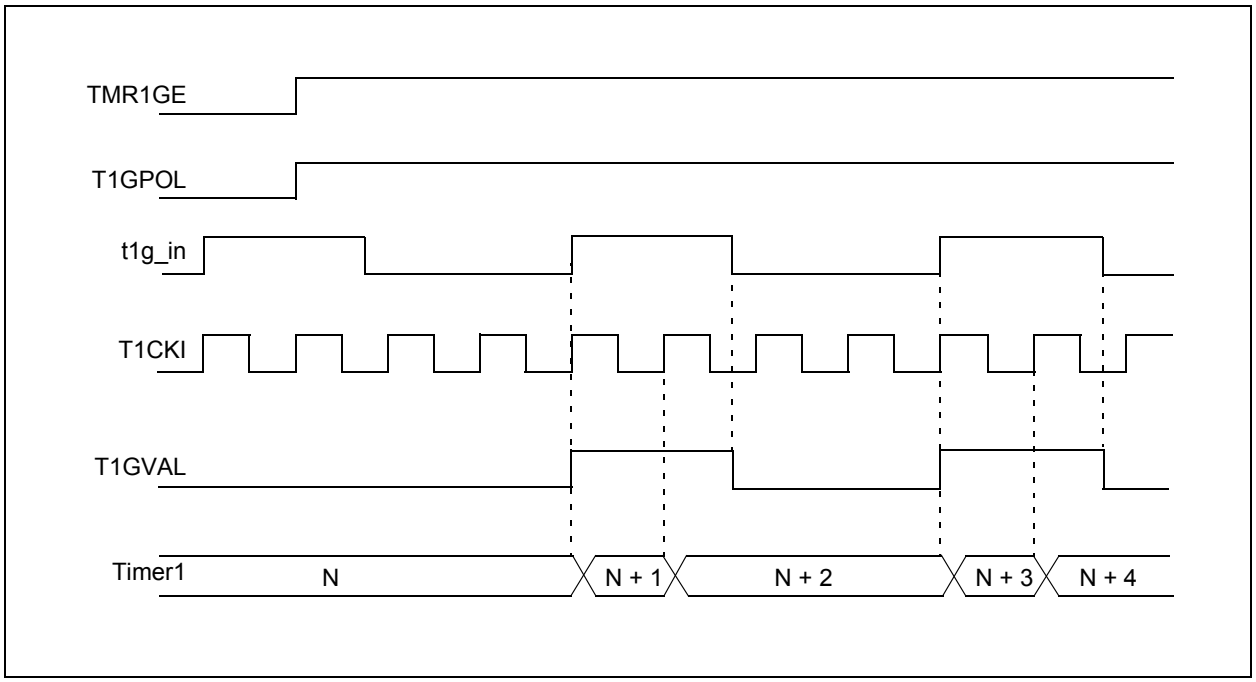
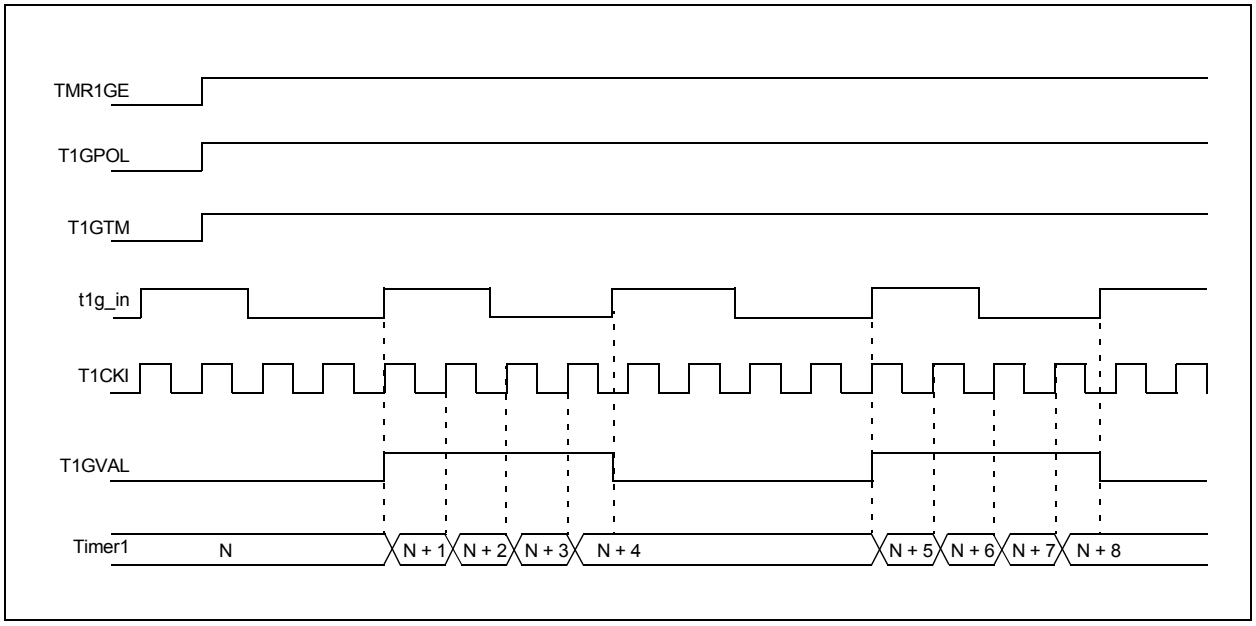


FIGURE 22-4: TIMER1 GATE TOGGLE MODE



24.3.8 PULSE-SKIPPING PWM WITH COMPLEMENTARY OUTPUTS

The pulse-skipping PWM is used to generate a series of fixed-length pulses that may or not be triggered at each period event. If any of the sources enabled to generate a rising edge event are high when a period event occurs, a pulse will be generated. If the rising edge sources are low at the period event, no pulse will be generated.

The rising edge occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

24.3.8.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM is output on only PSMCxA.
- Complementary PWM is output on only PSMCxB.

24.3.8.2 Waveform Generation

Rising Edge Event

If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:

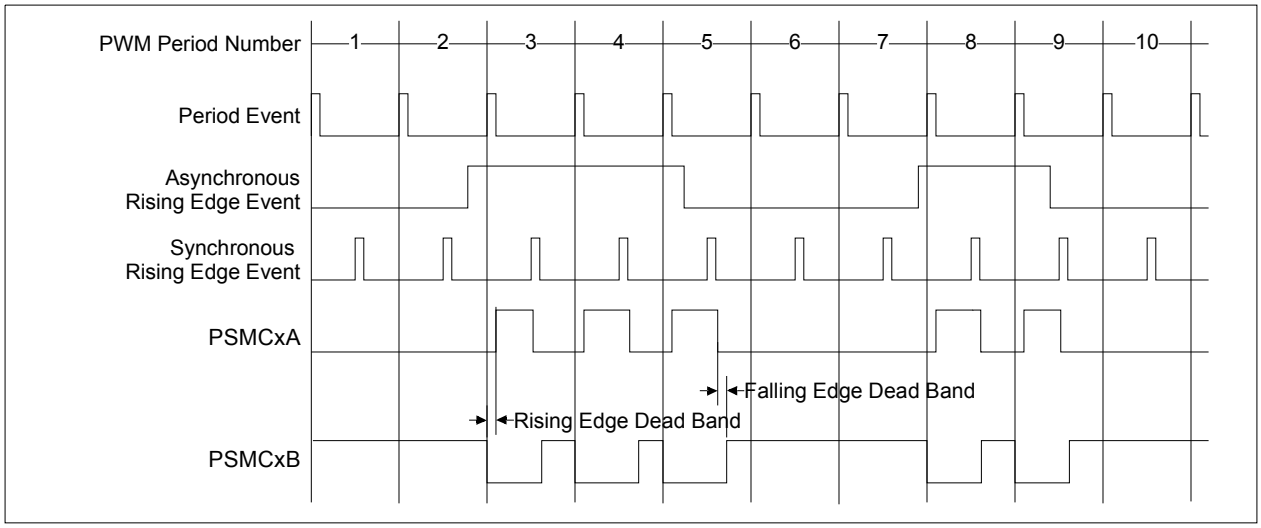
- Complementary output is set inactive
- Dead-band rising is activated (if enabled)
- Primary output is set active

Falling Edge Event

- Primary output is set inactive
- Dead-band falling is activated (if enabled)
- Complementary output is set active

Note:	To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 24-11: PULSE-SKIPPING WITH COMPLEMENTARY OUTPUT PWM WAVEFORM



24.10 Register Updates

There are 10 double-buffered registers that can be updated “on the fly”. However, due to the asynchronous nature of the potential updates, a special hardware system is used for the updates.

There are two operating cases for the PSMC:

- module is enabled
- module is disabled

24.10.1 DOUBLE BUFFERED REGISTERS

The double-buffered registers that are affected by the special hardware update system are:

- PSMCxPRL
- PSMCxPRH
- PSMCxDCL
- PSMCxDCH
- PSMCxPHL
- PSMCxPHH
- PSMCxDBR
- PSMCxDBF
- PSMCxBLKR
- PSMCxBLKF
- PSMCxSTR0 (when the PxSSYNC bit is set)

24.10.2 MODULE DISABLED UPDATES

When the PSMC module is disabled (PSMCxEN = 0), any write to one of the buffered registers will also write directly to the buffer. This means that all buffers are loaded and ready for use when the module is enabled.

24.10.3 MODULE ENABLED UPDATES

When the PSMC module is enabled (PSMCxEN = 1), the PSMCxLD bit of the PSMC Control (PSMCxCON) register (Register 24-1) must be used.

When the PSMCxLD bit is set, the transfer from the register to the buffer occurs on the next period event. The PSMCxLD bit is automatically cleared by hardware after the transfer to the buffers is complete.

The reason that the PSMCxLD bit is required is that depending on the customer application and operation conditions, all 10 registers may not be updated in one PSMC period. If the buffers are loaded at different times (i.e., DCL gets updated, but DCH does not OR DCL and DCL are updated by PRH and PRL are not), then unintended operation may occur.

The sequence for loading the buffer registers when the PSMC module is enabled is as follows:

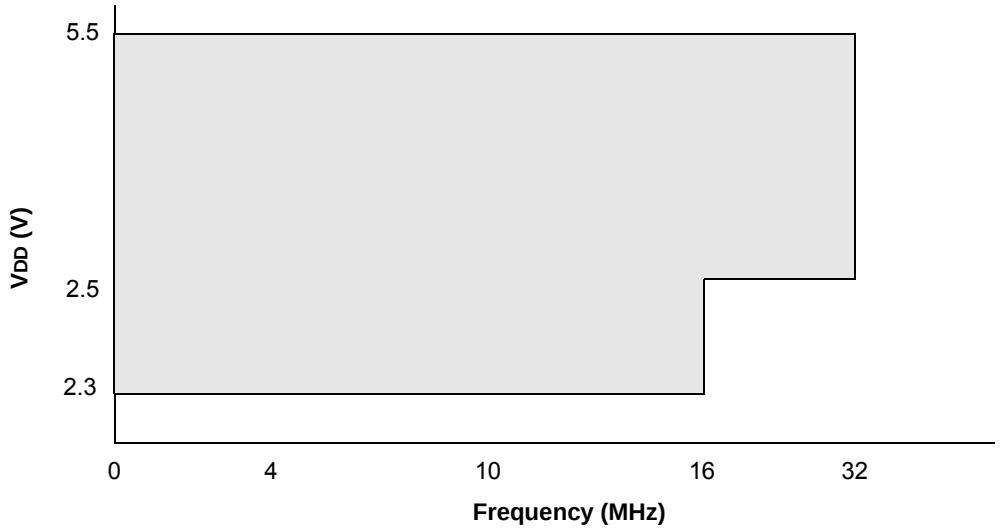
1. Software updates all registers.
2. Software sets the PSMCxLD bit.
3. Hardware updates all buffers on the next period event.
4. Hardware clears PSMCxLD bit.

24.11 Operation During Sleep

The PSMC continues to operate in Sleep with the following clock sources:

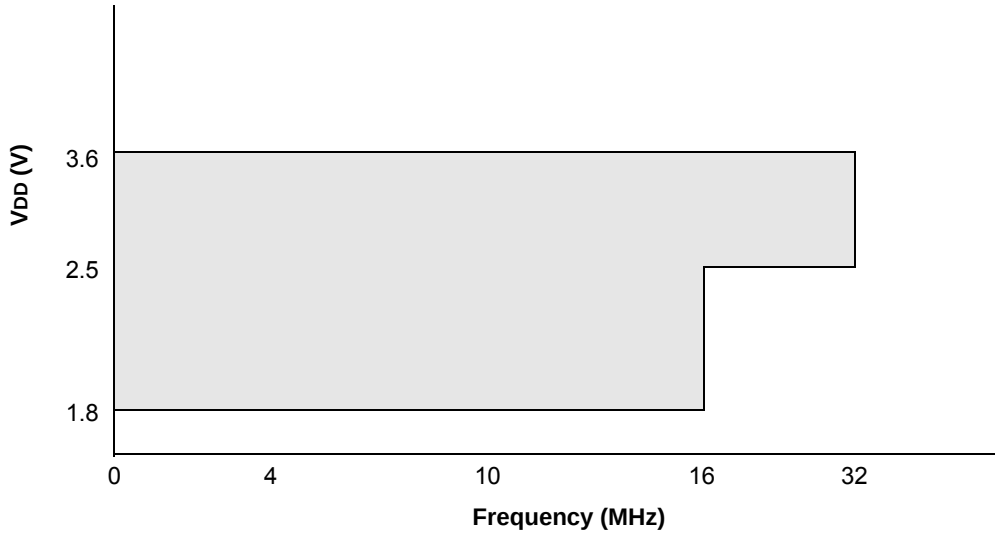
- Internal 64 MHz
- External clock

FIGURE 30-1: PIC16F1784/6/7 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 30-6 for each Oscillator mode's supported frequencies.

FIGURE 30-2: PIC16LF1784/6/7 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



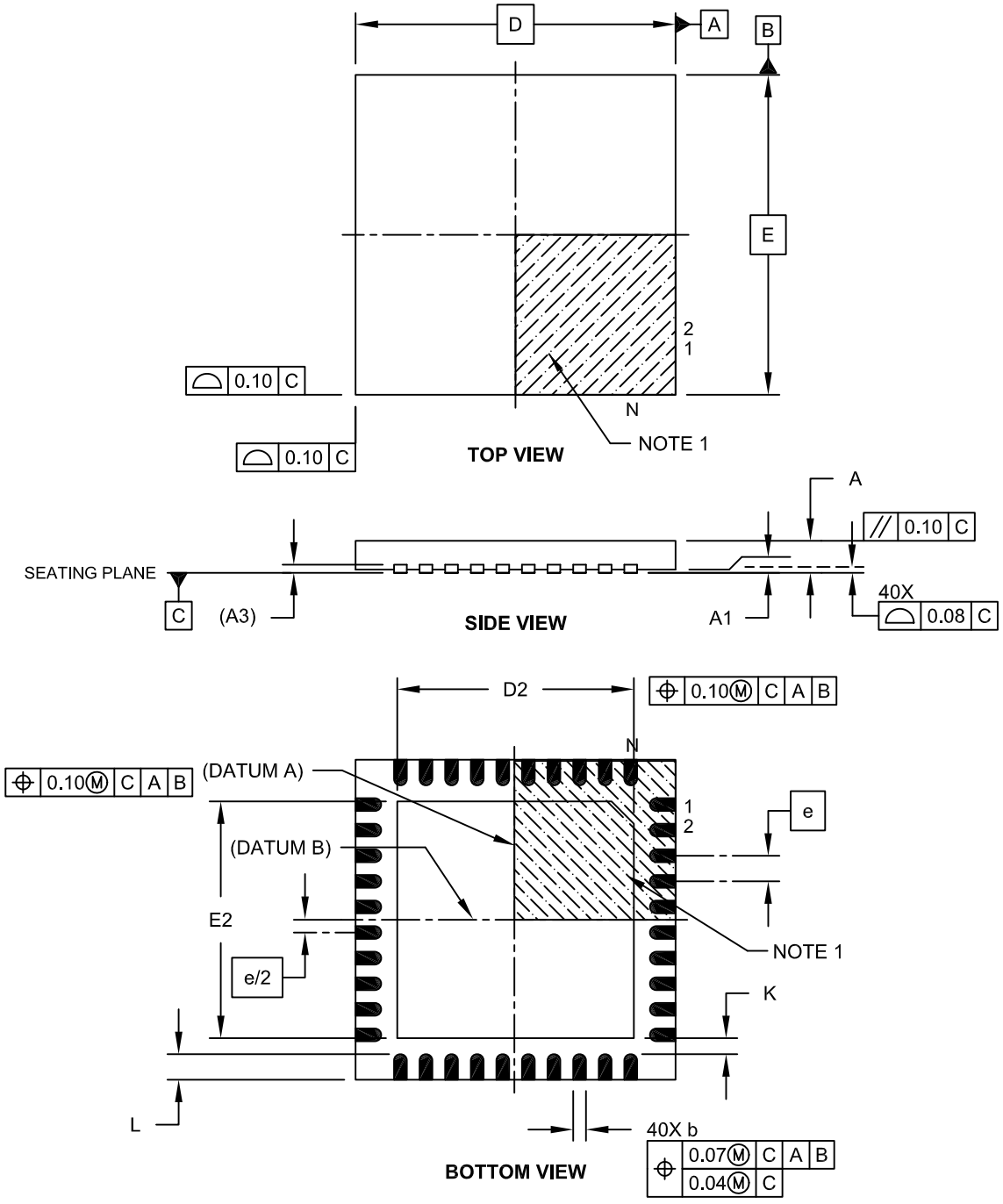
Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 30-6 for each Oscillator mode's supported frequencies.

TABLE 30-19: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-hold before CK ↓ (DT hold time)	10	—	ns	
US126	TCKL2DTL	Data-hold after CK ↓ (DT hold time)	15	—	ns	

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

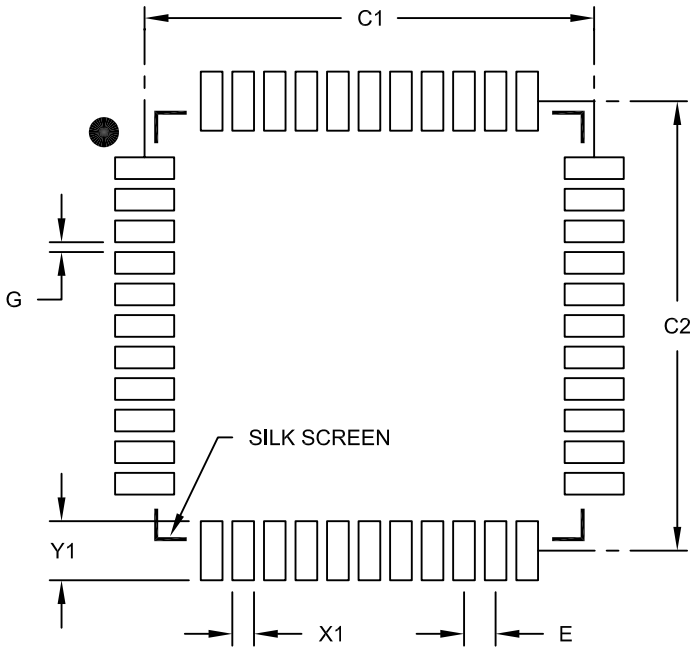
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B