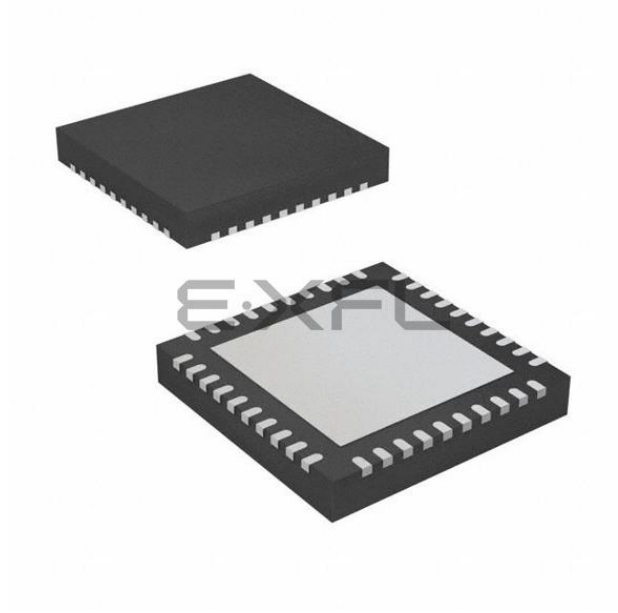

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1787-e-mv

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 16 (Continued)											
851h	PSMC3CON	PSMC3EN	PSMC3LD	P3DBFE	P3DBRE	P3MODE<3:0>				0000 0000	0000 0000
852h	PSMC3MDL	P3MDLEN	P3MDLPOL	P3MDLBIT	—	P3MSRC<3:0>				000- 0000	000- 0000
853h	PSMC3SYNC	P3POFST	P3PRPOL	P3DCPOL	—	—	—	P3SYNC<1:0>		000- --00	000- --00
854h	PSMC3CLK	—	—	P3CPRE<1:0>		—	—	P3CSRC<1:0>		--00 --00	--00 --00
855h	PSMC3OEN	—	—	—	—	—	—	P3OEB	P3OEA	---- --00	---- --00
856h	PSMC3POL	—	P3INPOL	—	—	—	—	P3POLB	P3POLA	-0-- --00	-0-- --00
857h	PSMC3BLNK	—	—	P3FEBM<1:0>		—	—	P3REBM<1:0>		--00 --00	--00 --00
858h	PSMC3REBS	P3REBSIN	—	—	P3REBSC4	P3REBSC3	P3REBSC2	P3REBSC1	—	0--0 000-	0--0 000-
859h	PSMC3FEBS	P3FEBSIN	—	—	P3FEBSC4	P3FEBSC3	P3FEBSC2	P3FEBSC1	—	0--0 000-	0--0 000-
85Ah	PSMC3PHS	P3PHSIN	—	—	P3PHSC4	P3PHSC3	P3PHSC2	P3PHSC1	P3PHST	0--0 0000	0--0 0000
85Bh	PSMC3DCS	P3DCSIN	—	—	P3DCSC4	P3DCSC3	P3DCSC2	P3DCSC1	P3DCST	0--0 0000	0--0 0000
85Ch	PSMC3PRS	P3PRSIN	—	—	P3PRSC4	P3PRSC3	P3PRSC2	P3PRSC1	P3PRST	0--0 0000	0--0 0000
85Dh	PSMC3ASDC	P3ASE	P3ASDEN	P3ARSEN	—	—	—	—	P3ASDOV	000- ---0	000- ---0
85Eh	PSMC3ASDL	—	—	—	—	—	—	P3ASDLB	P3ASDLA	---- --00	---- --00
85Fh	PSMC3ASDS	P3ASDSIN	—	—	P3ASDSC4	P3ASDSC3	P3ASDSC2	P3ASDSC1	—	0--0 000-	0--0 000-
860h	PSMC3INT	P3TOVIE	P3TPHIE	P3TDCIE	P3TPRIE	P3TOVIF	P3TPHIF	P3TDCIF	P3TPRIF	0000 0000	0000 0000
861h	PSMC3PHL	Phase Low Count								0000 0000	0000 0000
862h	PSMC3PHH	Phase High Count								0000 0000	0000 0000
863h	PSMC3DCL	Duty Cycle Low Count								0000 0000	0000 0000
864h	PSMC3DCH	Duty Cycle High Count								0000 0000	0000 0000
865h	PSMC3PRL	Period Low Count								0000 0000	0000 0000
866h	PSMC3PRH	Period High Count								0000 0000	0000 0000
867h	PSMC3TMRL	Time base Low Counter								0000 0001	0000 0001
868h	PSMC3TMRH	Time base High Counter								0000 0000	0000 0000
869h	PSMC3DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
86Ah	PSMC3DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
86Bh	PSMC3BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
86Ch	PSMC3BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
86Dh	PSMC3FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
86Eh	PSMC3STR0	—	—	—	—	—	—	P3STRB	P3STRA	---- --01	---- --01
86Fh	PSMC3STR1	P3SSYNC	—	—	—	—	—	P3LSMEN	P3HSMEN	0--- --00	0--- --00
Bank 17-30											
x0Ch or x8Ch to x1Fh or x9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	61
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	65
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	27
WDTCON	—	—	WDTPS<4:0>					SWDTEN	110

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

REGISTER 8-6: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **ADIF:** ADC Converter Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **RCIF:** EUSART Receive Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **TXIF:** EUSART Transmit Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **SSP1IF:** Synchronous Serial Port (MSSP) Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **TMR2IF:** Timer2 to PR2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

12.3 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum block size that can be erased by user software.

Flash program memory may only be written or erased if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of Configuration Words.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the EEDATH:EEDATL register pair.

Note:	If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase.

The number of data write latches may not be equivalent to the number of row locations. During programming, user software may need to fill the set of write latches and initiate a programming operation multiple times in order to fully reprogram an erased row. For example, a device with a row size of 32 words and eight write latches will need to load the write latches with data and initiate a programming operation four times.

The size of a program memory row and the number of program memory write latches may vary by device. See Table 12-1 for details.

12.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:

1. Write the Least and Most Significant address bits to the EEADRH:EEADRL register pair.
2. Clear the CFGS bit of the EECON1 register.
3. Set the EEPGD control bit of the EECON1 register.
4. Then, set control bit RD of the EECON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "`BSF EECON1,RD`" instruction to be ignored. The data is available in the very next cycle, in the EEDATH:EEDATL register pair; therefore, it can be read as two bytes in the following instructions.

EEDATH:EEDATL register pair will hold this value until another read or until it is written to by the user.

Note 1:	The two instructions following a program memory read are required to be `NOP`s. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.
2:	Flash program memory can be read regardless of the setting of the $\overline{CP}$ bit.

TABLE 12-1: FLASH MEMORY ORGANIZATION BY DEVICE

Device	Erase Block (Row) Size/Boundary	Number of Write Latches/Boundary
PIC16(L)F1784/6/7	32 words, EEADRL<4:0> = `00000`	32 words, EEADRL<4:0> = `00000`

13.11 PORTE Registers

RE3 is input only, and also functions as $\overline{MCLR}$. The $\overline{MCLR}$ feature can be disabled via a configuration fuse. RE3 also supplies the programming voltage. The TRIS bit for RE3 (TRISE3) always reads '1'.

13.11.1 DATA REGISTER

PORTE is an 8-bit wide bidirectional port. The corresponding data direction register is TRISE (Register 13-35). Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 13-1 shows how to initialize an I/O port.

Reading the PORTE register (Register 13-34) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATE).

13.11.2 DIRECTION CONTROL

The TRISE register (Register 13-35) controls the PORTE pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISE register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

13.11.3 OPEN DRAIN CONTROL

The ODCONE register (Register 13-31) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCONE bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCONE bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.11.4 SLEW RATE CONTROL

The SLRCOND register (Register 13-32) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCOND bit is set, the corresponding port pin drive is slew rate limited. When an SLRCOND bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

13.11.5 INPUT THRESHOLD CONTROL

The INLVLD register (Register 13-33) controls the input voltage threshold for each of the available PORTD input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTD register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See **Section 30.1 "DC Characteristics: PIC16(L)F1784/6/7-I/E (Industrial, Extended)"** for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.11.6 INPUT THRESHOLD CONTROL

The INLVLE register (Register 13-41) controls the input voltage threshold for each of the available PORTE input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTE register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See **Section TABLE 30-1: "Supply Voltage"** for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

REGISTER 17-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
AD<11:4>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **AD<11:4>**: ADC Result Register bits
Upper 8 bits of 12-bit conversion result

REGISTER 17-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
AD<3:0>				—	—	—	ADSIGN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **AD<3:0>**: ADC Result Register bits
Lower 4 bits of 12-bit conversion result

bit 3-1 **Extended LSb bits**: These are cleared to zero by DC conversion.

bit 0 **ADSIGN**: ADC Result Sign bit

REGISTER 24-2: PSMCxMDL: PSMC MODULATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxMDLEN	PxMDLPOL	PxMDLBIT	—	PxMSRC<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxMDLEN:** PSMC Periodic Modulation Mode Enable bit
- 1 = PSMCx is active when input signal selected by PxMSRC<3:0> is in its active state (see PxMPOL)
- 0 = PSMCx module is always active

bit 6 **PxMDLPOL:** PSMC Periodic Modulation Polarity bit
- 1 = PSMCx is active when the PSMCx Modulation source output equals logic '0' (active-low)
- 0 = PSMCx is active when the PSMCx Modulation source output equals logic '1' (active-high)

bit 5 **PxMDLBIT:** PSMC Periodic Modulation Software Control bit

PxMDLEN = 1 AND PxMSRC<3:0> = 0000
- 1 = PSMCx is active when the PxMDLPOL equals logic '0'
- 0 = PSMCx is active when the PxMDLPOL equals logic '1'

PxMDLEN = 0 OR (PxMDLEN = 1 and PxMSRC<3:0> <> '0000')
Does not affect module operation

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **PxMSRC<3:0>** PSMC Periodic Modulation Source Selection bits
- 1111 = Reserved
- 1110 = Reserved
- 1101 = Reserved
- 1100 = Reserved
- 1011 = Reserved
- 1010 = Reserved
- 1001 = Reserved
- 1000 = PSMCx Modulation Source is PSMCxIN pin
- 0111 = Reserved
- 0110 = PSMCx Modulation Source is CCP2
- 0101 = PSMCx Modulation Source is CCP1
- 0100 = Reserved
- 0011 = PSMCx Modulation Source is sync_C3OUT
- 0010 = PSMCx Modulation Source is sync_C2OUT
- 0001 = PSMCx Modulation Source is sync_C1OUT
- 0000 = PSMCx Modulation Source is PxMDLBIT register bit

REGISTER 24-5: PSMC3SYNC: PSMC3 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
P3POFST	P3PRPOL	P3DCPOL	—	—	—	P3SYNC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P3POFST:** PSMC3 Phase Offset Control bit
- 1 = sync_out source is phase event and latch set source is synchronous period event
- 0 = sync_out source is period event and latch set source is phase event

bit 6 **P3PRPOL:** PSMC3 Period Polarity Event Control bit
- 1 = Selected asynchronous period event inputs are inverted
- 0 = Selected asynchronous period event inputs are not inverted

bit 5 **P3DCPOL:** PSMC3 Duty-cycle Event Polarity Control bit
- 1 = Selected asynchronous duty-cycle event inputs are inverted
- 0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-2 **Unimplemented:** Read as '0'

bit 1-0 **P3SYNC<1:0>:** PSMC3 Period Synchronization Mode bits
- 11 = Reserved – Do not use
- 10 = PSMC3 is synchronized with the PSMC2 module (sync_in comes from PSMC2 sync_out)
- 01 = PSMC3 is synchronized with the PSMC1 module (sync_in comes from PSMC1 sync_out)
- 00 = PSMC3 is synchronized with period event

REGISTER 24-8: PSMCxPOL: PSMC POLARITY CONTROL REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	PxPOLIN	PxPOLF(1)	PxPOLE(1)	PxPOLD(1)	PxPOLC(1)	PxPOLB	PxPOLA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6 **PxPOLIN:** PSMCxIN Polarity bit
- 1 = PSMCxIN input is active-low
- 0 = PSMCxIN input is active-high

bit 5-0 **PxPOLy:** PSMCx Output y Polarity bit(1)
- 1 = PWM PSMCx output y is active-low
- 0 = PWM PSMCx output y is active-high

Note 1: These bits are not implemented on PSMC2.

REGISTER 24-9: PSMCxBLNK: PSMC BLANKING CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	PxFEBM1	PxFEBM0	—	—	PxREBM1	PxREBM0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **PxFEBM<1:0>** PSMC Falling Edge Blanking Mode bits
- 11 = Reserved – do not use
- 10 = Reserved – do not use
- 01 = Immediate blanking
- 00 = No blanking

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **PxREBM<1:0>** PSMC Rising Edge Blanking Mode bits
- 11 = Reserved – do not use
- 10 = Reserved – do not use
- 01 = Immediate blanking
- 00 = No blanking

26.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an $\overline{ACK}$ bit during the ninth bit time if an address match occurred, or if data was received properly. The status of $\overline{ACK}$ is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSP1IF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 26-27).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/$\overline{W}$ bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the $\overline{ACK}$ bit is loaded into the ACKSTAT Status bit of the SSPCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSP1IF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

26.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPSTAT register is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

26.6.6.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

26.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPCON2 register is cleared when the slave has sent an Acknowledge ($\overline{ACK}$ = 0) and is set when the slave does not Acknowledge ($\overline{ACK}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

26.6.6.4 Typical transmit sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. The MSSP module will wait the required start time before any other operation takes place.
5. The user loads the SSPBUF with the slave address to transmit.
6. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
7. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
8. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
9. The user loads the SSPBUF with eight bits of data.
10. Data is shifted out the SDA pin until all 8 bits are transmitted.
11. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPCON2 register. Interrupt is generated once the Stop/Restart condition is complete.

26.8 Register Definitions: MSSP Control

REGISTER 26-1: SSPSTAT: SSP STATUS REGISTER

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **SMP:** SPI Data Input Sample bit

SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode

In I^2C Master or Slave mode:
1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for high speed mode (400 kHz)

bit 6 **CKE:** SPI Clock Edge Select bit (SPI mode only)

In SPI Master or Slave mode:
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state

In I^2C™ mode only:
1 = Enable input logic so that thresholds are compliant with SMBus specification
0 = Disable SMBus specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)
0 = Stop bit was not detected last

bit 3 **S:** Start bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
0 = Start bit was not detected last

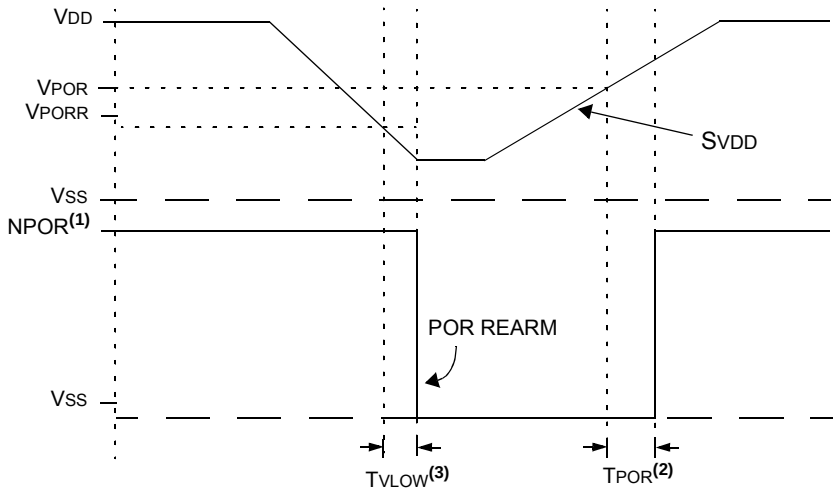
bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information (I^2C mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit.

In I^2C Slave mode:
1 = Read
0 = Write

In I^2C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

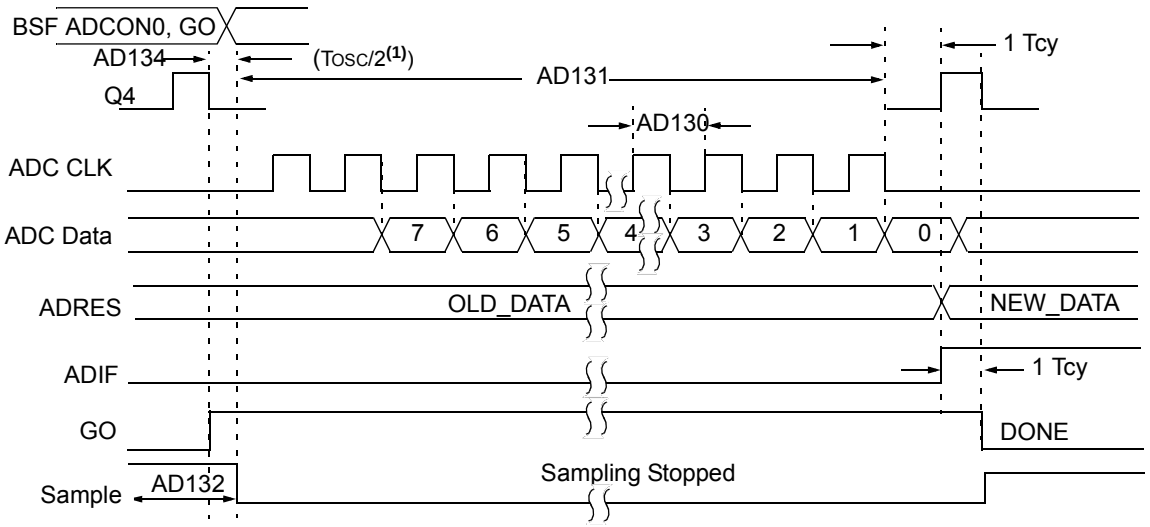
bit 1 **UA:** Update Address bit (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

FIGURE 30-3: POR AND POR REARM WITH SLOW RISING VDD



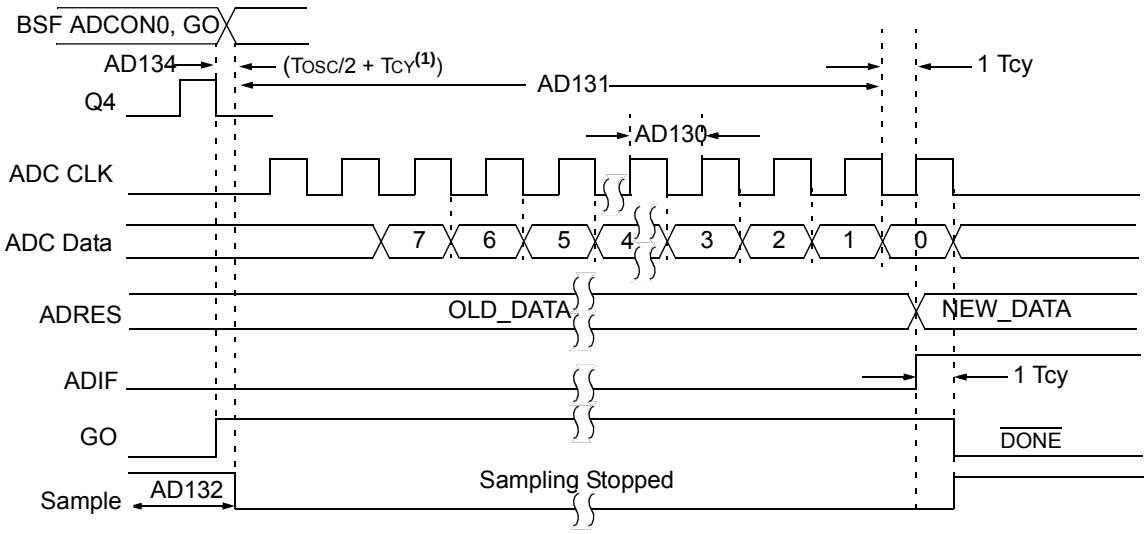
Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.

FIGURE 30-12: ADC CONVERSION TIMING (NORMAL MODE)



Note 1: If the ADC clock source is selected as RC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.

FIGURE 30-13: ADC CONVERSION TIMING (SLEEP MODE)



Note 1: If the ADC clock source is selected as RC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.

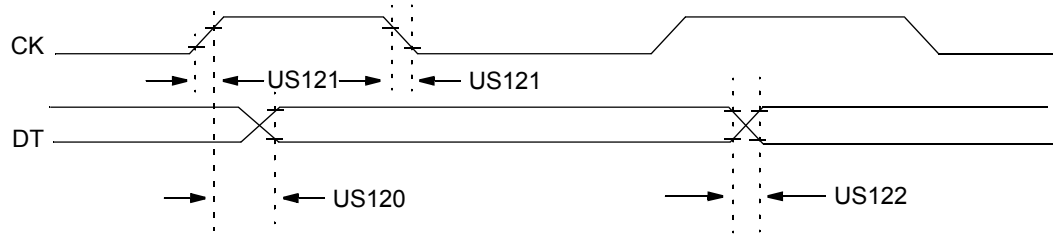
TABLE 30-17: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: V_{DD} = 3V, Temperature = 25°C (unless otherwise stated).							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DAC01*	C_{LSB}	Step Size	—	$V_{DD}/256$	—	V	
DAC02*	C_{ACC}	Absolute Accuracy	—	—	± 1.5	LSb	
DAC03*	C_R	Unit Resistor Value (R)	—	600	—	Ω	
DAC04*	C_{ST}	Settling Time(1)	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<7:0> transitions from '0x00' to '0xFF'.

FIGURE 30-14: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

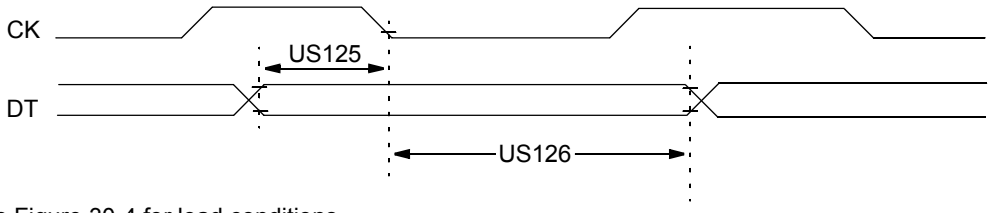


Note: Refer to Figure 30-4 for load conditions.

TABLE 30-18: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
US120	$T_{CKH2DTV}$	SYNC XMIT (Master and Slave) Clock high to data-out valid	3.0-5.5V	—	80	ns	
			1.8-5.5V	—	100	ns	
US121	T_{CKRF}	Clock out rise time and fall time (Master mode)	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	
US122	T_{DTRF}	Data-out rise time and fall time	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	

FIGURE 30-15: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 30-4 for load conditions.

FIGURE 30-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

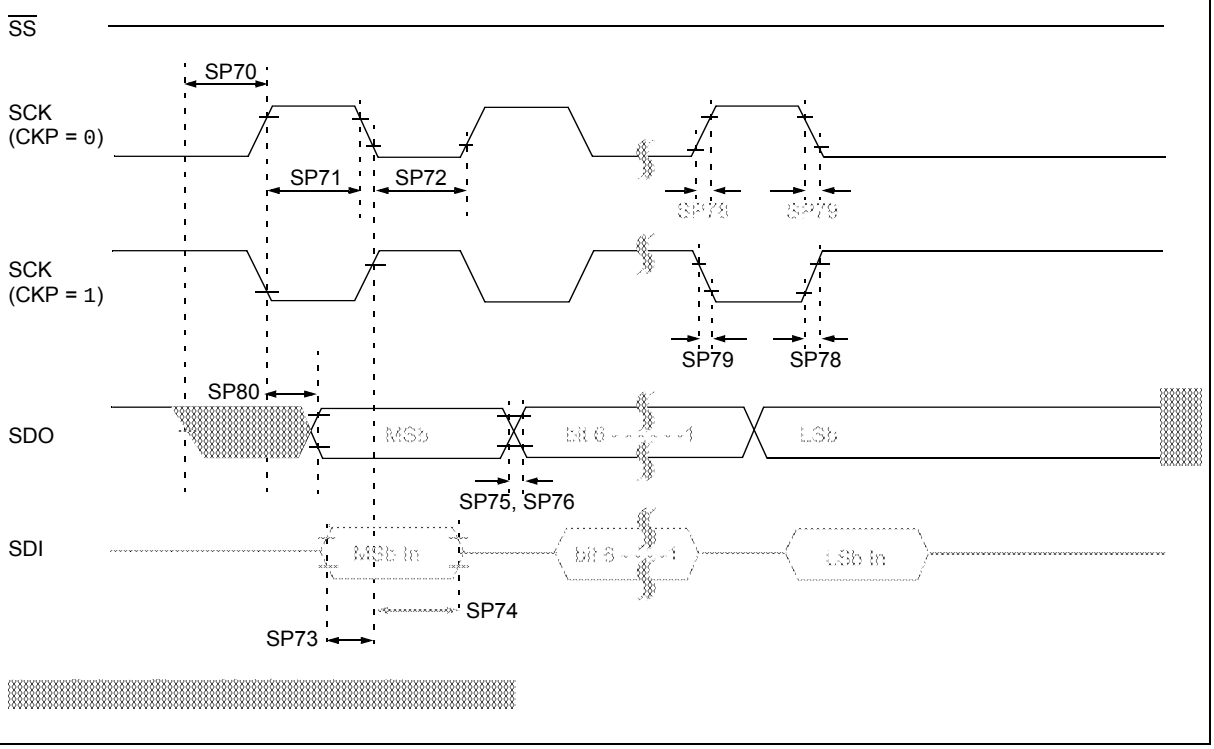
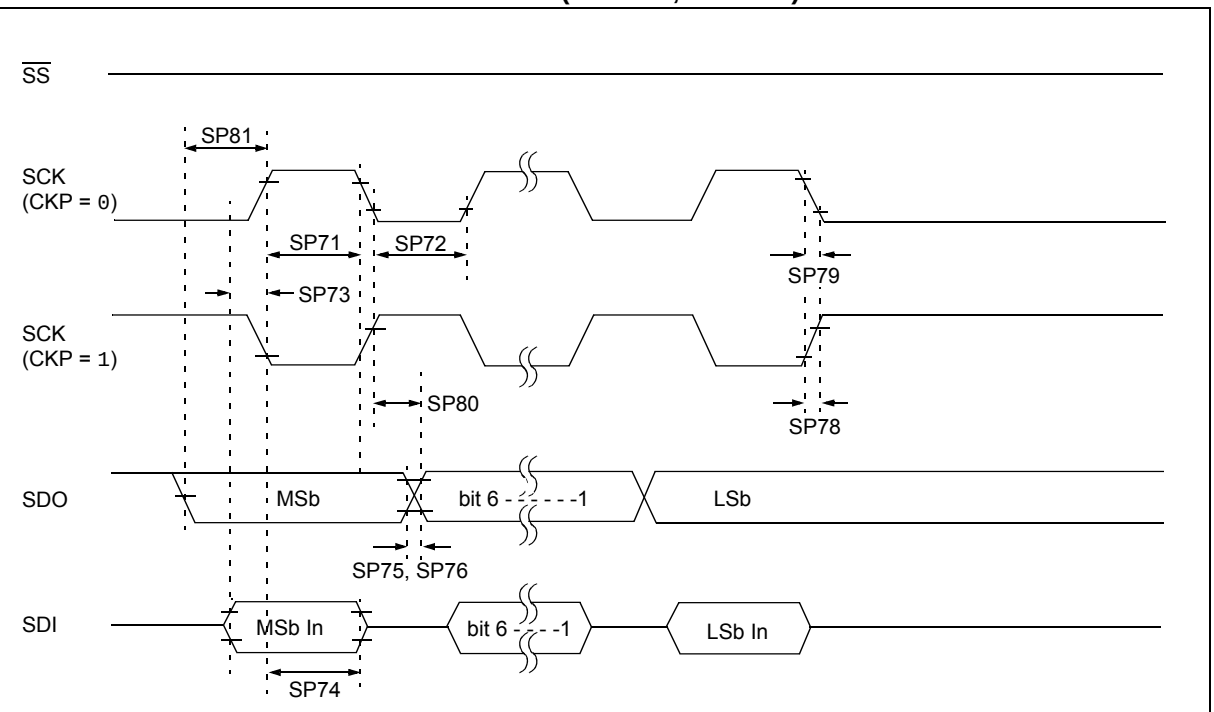


FIGURE 30-17: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



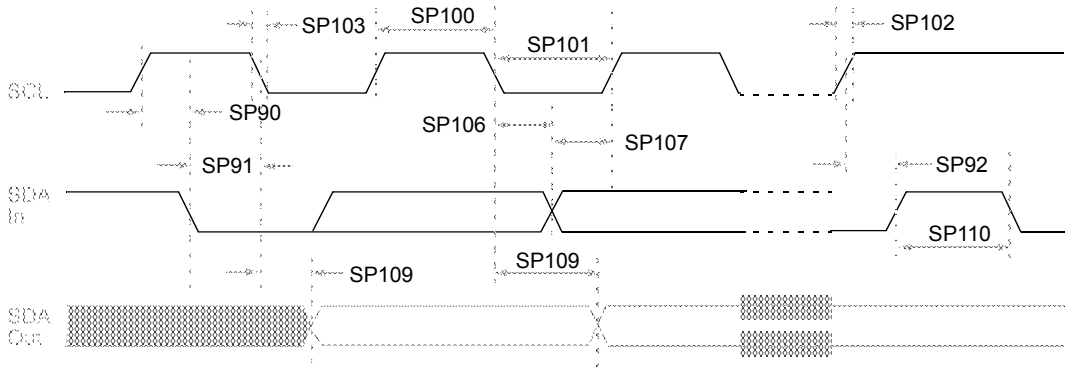
Note: Refer to Figure 30-4 for load conditions.

TABLE 30-21: I²C™ BUS START/STOP BITS REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
SP90*	TSU:STA	Start condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	—		
SP91*	THD:STA	Start condition Hold time	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	—		
SP92*	TSU:STO	Stop condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
SP93	THD:STO	Stop condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

FIGURE 30-21: I²C™ BUS DATA TIMING



Note: Refer to Figure 30-4 for load conditions.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

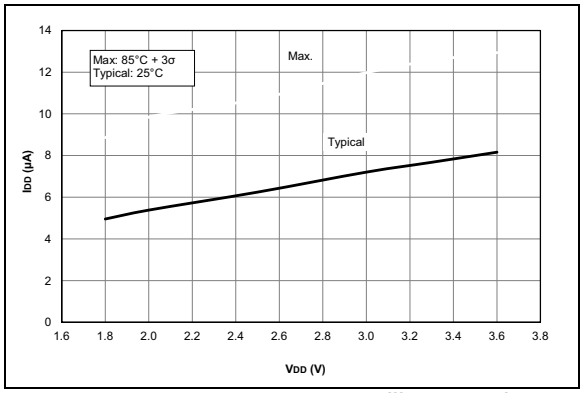


FIGURE 31-1: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16LF1784/6/7 Only.*

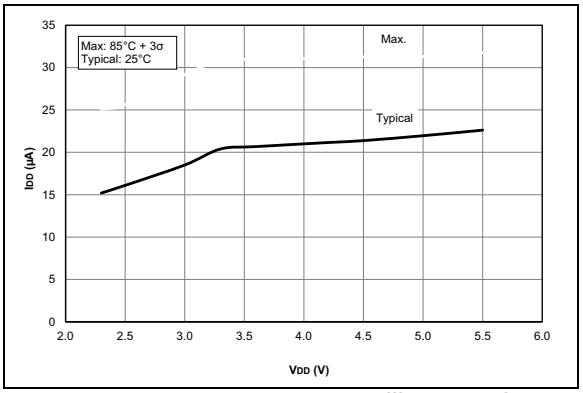


FIGURE 31-2: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16F1784/6/7 Only.*

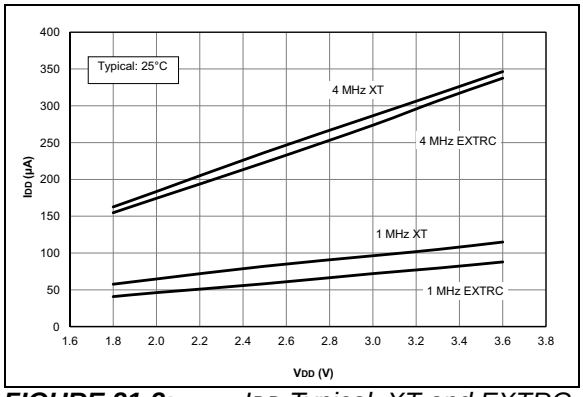


FIGURE 31-3: *IDD Typical, XT and EXTRC Oscillator, PIC16LF1784/6/7 Only.*

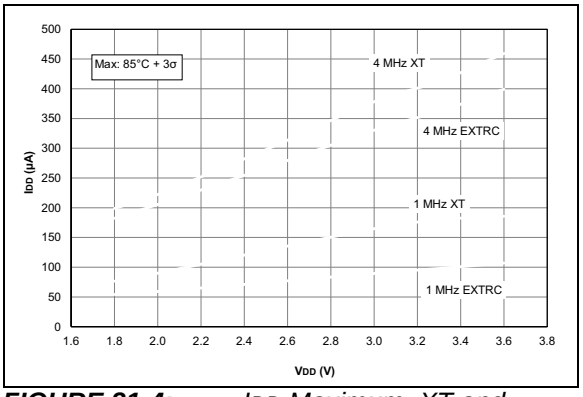


FIGURE 31-4: *IDD Maximum, XT and EXTRC Oscillator, PIC16LF1784/6/7 Only.*

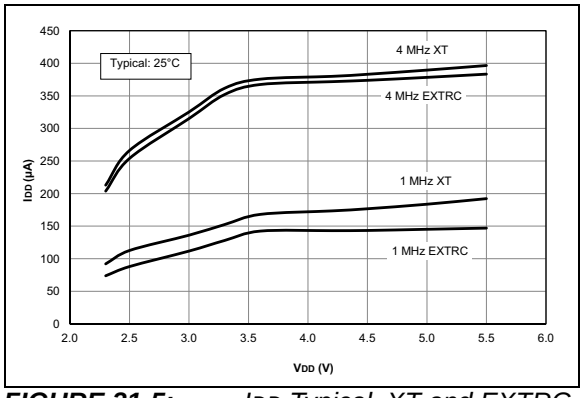


FIGURE 31-5: *IDD Typical, XT and EXTRC Oscillator, PIC16F1784/6/7 Only.*

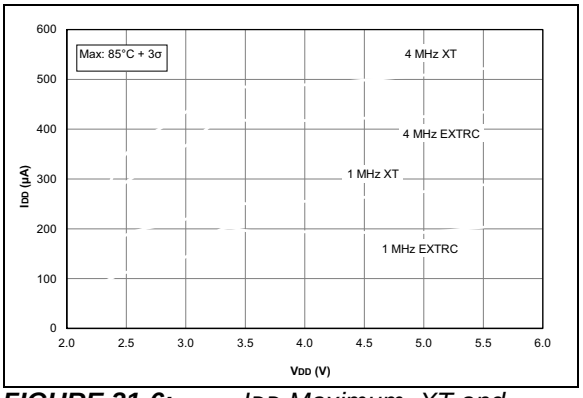


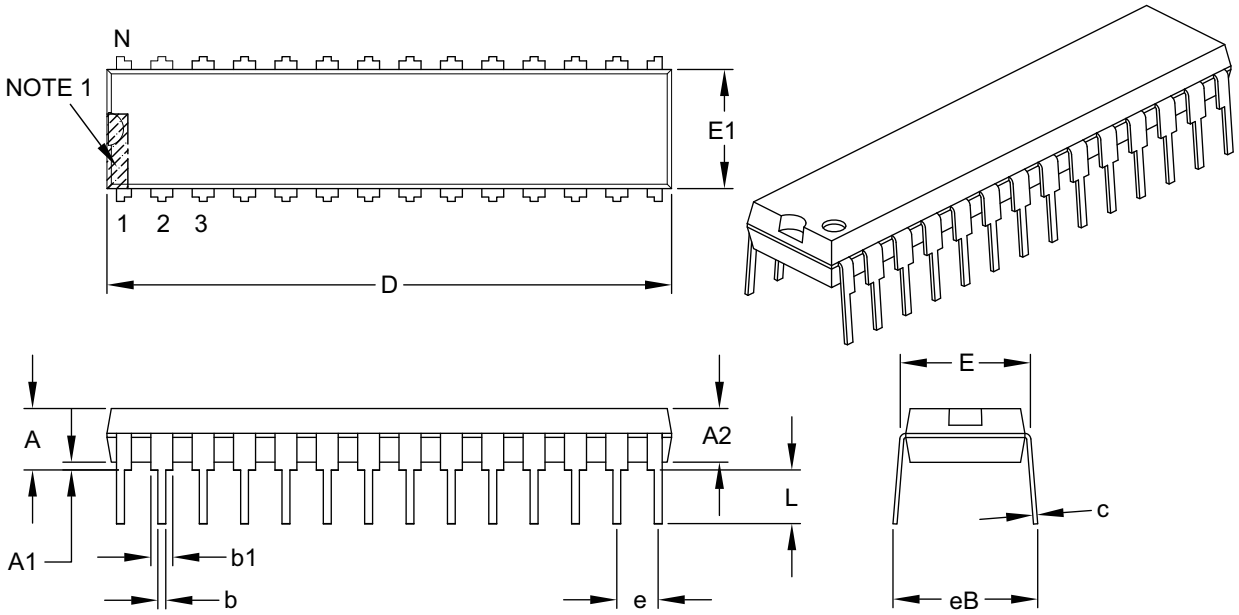
FIGURE 31-6: *IDD Maximum, XT and EXTRC Oscillator, PIC16F1784/6/7 Only.*

33.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

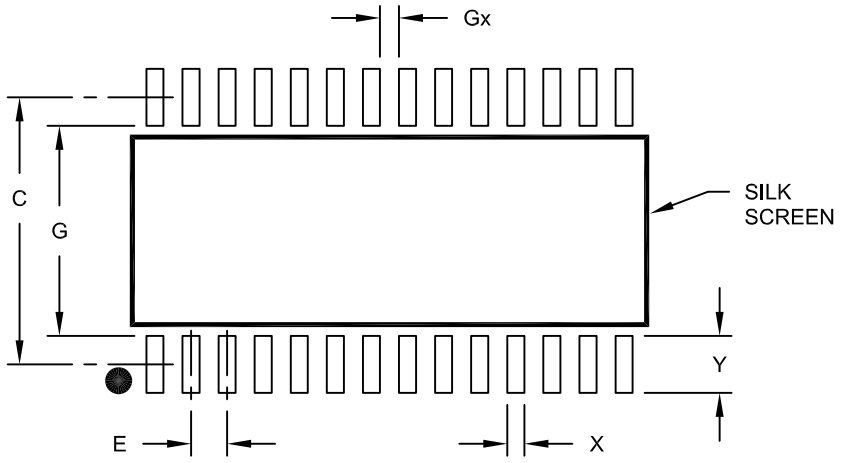
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

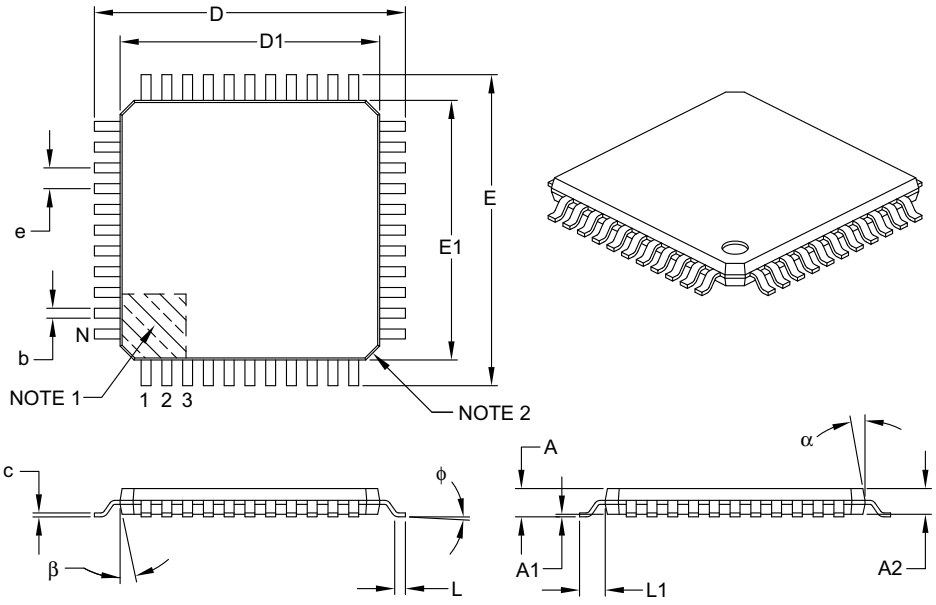
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B