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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1787-e-p

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5.3 Register Definitions: BOR Control

REGISTER 5-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	R/W-0/u	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	BORFS	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	SBOREN: Software Brown-out Reset Enable bit
	If BOREN <1:0> in Configuration Words ≠ 01:
	SBOREN is read/write, but has no effect on the BOR.
	If BOREN <1:0> in Configuration Words = 01:
	1 = BOR Enabled
	0 = BOR Disabled
bit 6	BORFS: Brown-out Reset Fast Start bit ⁽¹⁾
	<u>If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)</u>
	BORFS is Read/Write, but has no effect.
	If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):
	1 = Band gap is forced on always (covers sleep/wake-up/operating cases)
	0 = Band gap operates normally, and may turn off
bit 5-1	Unimplemented: Read as '0'
bit 0	BORRDY: Brown-out Reset Circuit Ready Status bit
	1 = The Brown-out Reset circuit is active
	0 = The Brown-out Reset circuit is inactive
Note 1:	BOREN<1:0> bits are located in Configuration Words.

6.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

A fast startup oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

6.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

6.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 6-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

6.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a multiplexer (see Figure 6-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See Section 6.2.2.7 "Internal Oscillator Clock Switch Timing" for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low-Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.

6.4.2 TWO-SPEED START-UP SEQUENCE

- 1. Wake-up from Power-on Reset or Sleep.
- 2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<3:0> bits of the OSCCON register.
- 3. OST enabled to count 1024 clock cycles.
- 4. OST timed out, wait for falling edge of the internal oscillator.
- 5. OSTS is set.
- 6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- 7. System clock is switched to external clock source.

$INTOSC \longrightarrow for the second seco$

FIGURE 6-8: TWO-SPEED START-UP

6.4.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCSTAT register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or the internal oscillator.

11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- · Independent clock source
- · Multiple operating modes
 - WDT is always on
 - WDT is off when in Sleep
 - WDT is controlled by software
 - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep





12.7 Register Definitions: EEPROM and Flash Control

REGISTER 12-1: EEDATL: EEPROM DATA LOW BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			EEDA	T<7:0>			
bit 7							bit 0
Logond							
R = Readable bit		W = Writable bit		U = Unimpleme	nted bit, read as '0	3	
u = Bit is unchanged		x = Bit is unknown		-n/n = Value at F	POR and BOR/Valu	ue at all other Res	ets
'1' = Bit is set		'0' = Bit is cleared					

bit 7-0

EEDAT<7:0>: Read/write value for EEPROM data byte or Least Significant bits of program memory

REGISTER 12-2: EEDATH: EEPROM DATA HIGH BYTE REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—			EEDA	\T<13:8>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'
bit 5-0	EEDAT<13:8>: Read/write value for Most Significant bits of program memory

REGISTER 12-3: EEADRL: EEPROM ADDRESS REGISTER

| R/W-0/0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| | | | EEADI | R<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 EEADR<7:0>: Specifies the Least Significant bits for program memory address or EEPROM address

REGISTER 12-4: EEADRH: EEPROM ADDRESS HIGH BYTE REGISTER

U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
(1)				EEADR<14:8>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 Unimplemented: Read as '1'

bit 6-0 EEADR<14:8>: Specifies the Most Significant bits for program memory address or EEPROM address

Note 1: Unimplemented, read as '1'.

PORTA Registers 13.3

13.3.1 DATA REGISTER

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 13-4). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 13-1 shows how to initialize PORTA.

Reading the PORTA register (Register 13-3) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

DIRECTION CONTROL 13.3.2

The TRISA register (Register 13-4) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

OPEN DRAIN CONTROL 13.3.3

The ODCONA register (Register 13-8) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.3.4 SLEW RATE CONTROL

The SLRCONA register (Register 13-9) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

13.3.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 13-10) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section TABLE 30-1: "Supply Voltage" for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.3.6 ANALOG CONTROL

The ANSELA register (Register 13-6) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

EXAMPL	E 13-1: IN	ITIALIZING PORTA
; This c ; initia ; other ; manner	code example alizing the P ports are in c.	illustrates ORTA register. The itialized in the same
BANKSEL	PORTA	;
CLRF	PORTA	;Init PORTA
BANKSEL	LATA	;Data Latch
CLRF	LATA	;
BANKSEL	ANSELA	;
CLRF	ANSELA	;digital I/O
BANKSEL	TRISA	;
MOVLW	B'00111000'	;Set RA<5:3> as inputs
MOVWF	TRISA	;and set RA<2:0> as
		;outputs

24.0 PROGRAMMABLE SWITCH MODE CONTROL (PSMC)

The Programmable Switch Mode Controller (PSMC) is a high-performance Pulse Width Modulator (PWM) that can be configured to operate in one of several modes to support single or multiple phase applications.

A simplified block diagram indicating the relationship between inputs, outputs, and controls is shown in Figure 24-1.

This section begins with the fundamental aspects of the PSMC operation. A more detailed description of operation for each mode is located later in **Section 24.3** "**Modes of Operation**"

Modes of operation include:

- Single-phase
- · Complementary Single-phase
- Push-Pull
- Push-Pull 4-Bridge
- · Complementary Push-Pull 4-Bridge
- · Pulse Skipping
- Variable Frequency Fixed Duty Cycle
- Complementary Variable Frequency Fixed Duty
 Cycle
- · ECCP Compatible modes
 - Full-Bridge
 - Full-Bridge Reverse
- · 3-Phase 6-Step PWM

24.3.10 VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM

This mode of operation is quite different from all of the other modes. It uses only the period event for waveform generation. At each period event, the PWM output is toggled.

The rising edge and falling edge events are unused in this mode.

24.3.10.1 Mode Features

- · No dead-band control available
- · No steering control available
- Fractional Frequency Adjust
 - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 24-28)
- PWM is output on the following pin only:
 - PSMCxA

24.3.10.2 Waveform Generation

Period Event

- · Output of PSMCxA is toggled
- FFA counter is incremented by the 4-bit value in PSMCxF FA

FIGURE 24-13: VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WAVEFORM



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The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 25-4).

25.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 25-4.

EQUATION 25-4: PWM RESOLUTION

Resolution =
$$\frac{\log[4(PR2 + 1)]}{\log(2)}$$
 bits

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 25-1:	EXAMPLE PWM FREQUENCIES AND RESOLUTIONS ((Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 25-2:	EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 M	Hz)
-------------	-----------------------------------------------------	-----

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5



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26.5.4 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 10-bit Addressing mode.

Figure 26-19 is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I²C communication.

- 1. Bus starts Idle.
- Master sends Start condition; S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- 3. Master sends matching high address with R/W bit clear; UA bit of the SSPSTAT register is set.
- 4. Slave sends ACK and SSP1IF is set.
- 5. Software clears the SSP1IF bit.
- 6. Software reads received address from SSPBUF clearing the BF flag.
- 7. Slave loads low address into SSPADD, releasing SCL.
- 8. Master sends matching low address byte to the slave; UA bit is set.

Note: Updates to the SSPADD register are not allowed until after the ACK sequence.

- 9. Slave sends ACK and SSP1IF is set.
- **Note:** If the low address does not match, SSP1IF and UA are still set so that the slave software can set SSPADD back to the high address. BF is not set because there is no match. CKP is unaffected.
- 10. Slave clears SSP1IF.
- 11. Slave reads the received matching address from SSPBUF clearing BF.
- 12. Slave loads high address into SSPADD.
- Master clocks a data byte to the slave and clocks out the slaves ACK on the 9th SCL pulse; SSP1IF is set.
- 14. If SEN bit of SSPCON2 is set, CKP is cleared by hardware and the clock is stretched.
- 15. Slave clears SSP1IF.
- 16. Slave reads the received byte from SSPBUF clearing BF.
- 17. If SEN is set the slave sets CKP to release the SCL.
- 18. Steps 13-17 repeat for each received byte.
- 19. Master sends Stop to end the transmission.

26.5.5 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and SCL line is held low are the same. Figure 26-20 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 26-21 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.

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FIGURE 26-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

R-0/0	R-1/1	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
ABDOVF	RCIDL	—	SCKP	BRG16		WUE	ABDEN
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BOF	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	ABDOVF: Au	to-Baud Detec	t Overflow bit				
	1 = Auto-bau	d timer overflow	ved				
	0 = Auto-bau	d timer did not	overflow				
	Synchronous	mode:					
bit 6	RCIDI · Recei	ive Idle Flag bi	t				
Sit o	Asynchronous	s mode:					
	1 = Receiver	is idle					
	0 = Start bit h	as been receiv	ed and the red	ceiver is receiv	ving		
	Don't care	<u>moue</u> .					
bit 5	Unimplemen	ted: Read as '	0'				
bit 4	SCKP: Synch	ronous Clock I	Polarity Select	bit			
	Asynchronous	<u>s mode</u> :					
	1 = Transmit i 0 = Transmit i	nverted data to non-inverted da	o the TX/CK p ata to the TX/0	in CK pin			
	Synchronous	mode:					
	1 = Data is clo 0 = Data is clo	ocked on rising ocked on falling	edge of the c gedge of the c	lock clock			
bit 3	BRG16: 16-bi	it Baud Rate G	enerator bit				
	1 = 16-bit Bau 0 = 8-bit Bau	ud Rate Gener d Rate Genera	ator is used tor is used				
bit 2	Unimplemen	ted: Read as '	0'				
bit 1	WUE: Wake-u	up Enable bit					
	Asynchronous	<u>s mode</u> :					
	 1 = Receiver is waiting for a falling edge. No character will be received, byte RCIF will be set. WU will automatically clear after RCIF is set. 						
	<u>Synchronous</u>	mode:	innany				
	Don't care						
bit 0	ABDEN: Auto	-Baud Detect I	Enable bit				
	Asynchronous	<u>s mode</u> :					
	1 = Auto-Bau	Id Detect mode	e is enabled (c	lears when au	ito-baud is comp	lete)	
	Synchronous	mode:					
	Don't care						

REGISTER 27-3: BAUDCON: BAUD RATE CONTROL REGISTER

			_		14-Bit (Opcod	е	Status	
Mnem Opera	Mnemonic, Description		Cycle s	MS			I Sh	Affecte	Notes
-				b			LOD	a	
	BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f,d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWF	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2
С	f,d	AND W with £	1	00	0101	dfff	ffff	Z	2
ANDWF	f,d	Arithmetic Right Shift	1		0111	dIII dfff	IIII ffff	C, Z	2
ASRF	f,d	Logical Left Shift	1	11	0110	dfff	ffff	C, Z	2
LSLF	f, d	Logical Right Shift	1	00	0001	lfff	ffff	C, Z	2
LSRF	f	Clear f	1	00	0001	0000	00xx	Z	2
CLRF	-	Clear W	1	00	1001	dfff	ffff	Z	
CLRW	f,d	Complement f	1	00	0011	dfff	ffff	Z	2
COMF	f,d	Decrement f	1	00	1010	dfff	ffff	Z	2
DECF	f,d	Increment f	1	00	0100	dfff	ffff	Z	2
INCF	f,d	Inclusive OR W with f	1	00	1000	dfff	ffff	Z	2
IORWF	f,d	Move f	1	00	0000	lfff	ffff	Z	2
MOVF	f	Move W to f	1	00	1101	dfff	ffff		2
MOVWF	f,d	Rotate Left f through Carry	1	00	1100	diii	titi eeee	С	2
RLF	f,d	Rotate Right f through Carry	1	11	1011	diii	LLLL ffff	С	2
RRF	f,d	Subtract W from f	1	00	1110	dfff	ffff	C, DC, Z	2
SUBWF	f,d	Subtract with Borrow W from f	1	00	0110	dfff	ffff	C, DC, Z	2
SUB-	f,d	Swap nibbles in £	1						2
WFB	f,d	Exclusive OR W with f	1					Z	2
SWAPF									
XORWF									
		BYTE ORIENTED SKIP	OPERAT	IONS	5				
DECES7	f,d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1, 2
INCFSZ	f, d	Increment £, Skip if 0	1(2)	00	1111	dfff	ffff		1, 2
		BIT-ORIENTED FILE REGIS		ERATI	IONS				
DOF	fb	Rit Cloar f	1	01	0066	hfff	ffff		2
BCF	f b	Bit Set f	1	01	0000 01bb	bfff	ffff		2
БЭГ	1, 0	BROOFF	•	01	0100	UIII			-
		BIT-ORIENTED SKIP C	PERATI	ONS					
BTFSC	f, b	Bit Test £, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2
BTFSS	f, b	Bit Test £, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2
			TIONS					0.50 -	
ADDLW	k	Add literal and W	1	11	1110	KKKK	kkkk	C, DC, Z	
ANDLW	ĸ	AND literal with W	1	11	1001	KKKK	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	0000	001k	kkkk		
MOVLP	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

TABLE 29-3: ENHANCED MID-RANGE INSTRUCTION SET

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

Mnomonic					14-Bit (Opcod	Status		
Opera	ands	Description	s	MS b			LSb	Affecte d	Notes
		CONTROL OPER	ATIONS						
BRA	k	Relative Branch	2	11	001k	kkkk	kkkk		
BRW	-	Relative Branch with W	2	00	0000	0000	1011		
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CALLW	-	Call Subroutine with W	2	00	0000	0000	1010		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
RETFIE	k	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	0100	kkkk	kkkk		
RETUR	-	Return from Subroutine	2	00	0000	0000	1000		
N									
		INHERENT OPER	ATIONS						
CLR-	_	Clear Watchdog Timer	1	00	0000	0110	0100	TO, PD	
WDT	_	No Operation	1	00	0000	0000	0000		
NOP	_	Load OPTION REG register with W	1	00	0000	0110	0010		
OPTION	_	Software device Reset	1	00	0000	0000	0001		
RESET	_	Go into Standby mode	1	00	0000	0110	0011	TO, PD	
SLEEP	f	Load TRIS register with W	1	00	0000	0110	Offf		
TRIS		-							
		C-COMPILER OP	TIMIZED						
ADDFS	n, k	Add Literal k to FSRn	1	11	0001	0nkk	kkkk		
R	n mm	Move Indirect FSRn to W with pre/post	1	00	0000	0001	0nm	Z	2.3
MOVIW		inc/dec modifier, mm					m		,
	k[n]	Move INDFn to W. Indexed Indirect.	1	11	1111	0nkk	kkkk	Z	2
	n mm	Move W to Indirect FSRn with pre/post	1	00	0000	0001	1nmm		2, 3
MOVWI		inc/dec modifier, mm					kkkk		,
	k[n]	Move W to INDFn, Indexed Indirect.	1	ΤT	1111	1nkk			2

TABLE 29-4: ENHANCED MID-RANGE INSTRUCTION SET (CONTINUED)

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

3: See Table in the MOVIW and MOVWI instruction descriptions.

29.2 Instruction Descriptions

ADDFSR	Add Literal to FSRn
Syntax:	[label] ADDFSR FSRn, k
Operands:	-32 ≤ k ≤ 31 n Î [0, 1]
Operation:	$FSR(n) + k \rightarrow FSR(n)$
Status Affected:	None
Description:	The signed 6-bit literal 'k' is added to the contents of the FSRnH:FSRnL register pair.
	FSRn is limited to the range 0000h - FFFFh. Moving beyond these bounds will cause the FSR to wrap-around.

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Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 31-25: IDD Typical, HFINTOSC Mode, PIC16F1784/6/7 Only.



FIGURE 31-26: IDD Maximum, HFINTOSC Mode, PIC16F1784/6/7 Only.



FIGURE 31-27: IDD Typical, HS Oscillator, 25°C, PIC16LF1784/6/7 Only.



FIGURE 31-28: IDD Maximum, HS Oscillator, PIC16LF1784/6/7 Only.



FIGURE 31-29: IDD Typical, HS Oscillator, 25°C, PIC16F1784/6/7 Only.



FIGURE 31-30: IDD Maximum, HS Oscillator, PIC16F1784/6/7 Only.

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Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.







FIGURE 31-69: PWRT Period, PIC16F1784/6/7 Only.









FIGURE 31-72: POR Rearm Voltage, NP Mode (VREGPM = 0), PIC16F1784/6/7 Only.

33.0 PACKAGING INFORMATION

33.1 Package Marking Information



Legend:	XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC [®] designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the even be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available for customer-specific information.

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