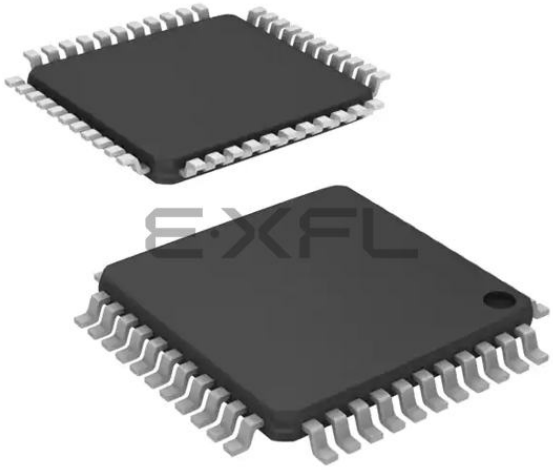

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PSMC, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 14x12b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1787-e-pt |

**REGISTER 8-6: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1**

| R/W-0/0 | R/W-0/0 | R-0/0 | R-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **ADIF:** ADC Converter Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **RCIF:** EUSART Receive Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **TXIF:** EUSART Transmit Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **SSP1IF:** Synchronous Serial Port (MSSP) Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **TMR2IF:** Timer2 to PR2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

## 13.4 Register Definitions: PORTA

### REGISTER 13-3: PORTA: PORTA REGISTER

| R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x |
|---|---|---|---|---|---|---|---|
| RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **RA<7:0>**: PORTA I/O Value bits(1)
1 = Port pin is ≥ $V_{IH}$
0 = Port pin is ≤ $V_{IL}$

**Note 1:** Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

### REGISTER 13-4: TRISA: PORTA TRI-STATE REGISTER

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **TRISA<7:0>:** PORTA Tri-State Control bits
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

### REGISTER 13-5: LATA: PORTA DATA LATCH REGISTER

| R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u |
|---|---|---|---|---|---|---|---|
| LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-4 **LATA<7:0>**: PORTA Output Latch Value bits(1)

**Note 1:** Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

**REGISTER 13-14: ANSELB: PORTB ANALOG SELECT REGISTER**

| U-0 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | ANSB6 | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ANSB<6:0>**: Analog Select between Analog or Digital Function on pins RB<6:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**REGISTER 13-15: WPUB: WEAK PULL-UP PORTB REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| WPUB7 | WPUB6 | WPUB5 | WPUB4 | WPUB3 | WPUB2 | WPUB1 | WPUB0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0 **WPUB<7:0>**: Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

**Note 1:** Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.

**REGISTER 13-29: ANSELD: PORTD ANALOG SELECT REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | ANSD2 | ANSD1 | ANSD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **ANSD<2:0>**: Analog Select between Analog or Digital Function on pins RD<2:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**REGISTER 13-30: WPUD: WEAK PULL-UP PORTD REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| WPUD7 | WPUD6 | WPUD5 | WPUD4 | WPUD3 | WPUD2 | WPUD1 | WPUD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0 **WPUD<7:0>**: Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

**Note 1:** Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.

**TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| ADCON0 | ADRMD | CHS<4:0> | | | | | GO/$\overline{\text{DONE}}$ | ADON | 172 |
| ADCON1 | ADFM | ADCS<2:0> | | | — | ADNREF | ADPREF<1:0> | | 173 |
| ADCON2 | TRIGSEL<3:0> | | | | CHSN<3:0> | | | | 174 |
| ADRESH | A/D Result Register High | | | | | | | | 175, 176 |
| ADRESL | A/D Result Register Low | | | | | | | | 175, 176 |
| ANSELA | ANSA7 | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | 132 |
| ANSELB | — | ANSB6 | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 | 138 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 94 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 131 |
| TRISB | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | 137 |
| FVRCON | FVREN | FVRRDY | TSEN | TSRNG | CDAFVR<1:0> | | ADFVR<1:0> | | 162 |

**Legend:** x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for the ADC module.

## 18.4 Register Definitions: Op Amp Control

**REGISTER 18-1: OPAxCON: OPERATIONAL AMPLIFIERS (OPAx) CONTROL REGISTERS**

| R/W-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| OPAxEN | OPAxSP | — | — | — | — | OPAxCH<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | q = Value depends on condition |

bit 7 **OPAxEN:** Op Amp Enable bit
1 = Op amp is enabled
0 = Op amp is disabled and consumes no active power

bit 6 **OPAxSP:** Op Amp Speed/Power Select bit
1 = Comparator operates in high GBWP mode
0 = Reserved. Do not use.

bit 5-2 **Unimplemented:** Read as '0'

bit 1-0 **OPAxCH<1:0>:** Non-inverting Channel Selection bits
11 = Non-inverting input connects to FVR Buffer 2 output
10 = Non-inverting input connects to DAC_output
0x = Non-inverting input connects to OPAxIN+ pin

**TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH OP AMPS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| ANSELA | ANSA7 | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | 132 |
| ANSELB | — | ANSB6 | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 | 138 |
| DAC1CON0 | DAC1EN | — | DAC1OE1 | DAC1OE2 | DAC1PSS<1:0> | | — | DAC1NSS | 186 |
| DAC1CON1 | DAC1R<7:0> | | | | | | | | 186 |
| OPA1CON | OPA1EN | OPA1SP | — | — | — | — | OPA1PCH<1:0> | | 182 |
| OPA2CON | OPA2EN | OPA2SP | — | — | — | — | OPA2PCH<1:0> | | 182 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 131 |
| TRISB | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | 137 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 142 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by op amps.
**Note 1:** PIC16(L)F1784/7 only

**TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| CCP2CON | — | — | DC2B<1:0> | | CCP2M<3:0> | | | | 280 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 94 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| PR2 | Timer2 Module Period Register | | | | | | | | 210* |
| T2CON | — | T2OUTPS<3:0> | | | | TMR2ON | T2CKPS<1:0> | | 212 |
| TMR2 | Holding Register for the 8-bit TMR2 Register | | | | | | | | 210* |

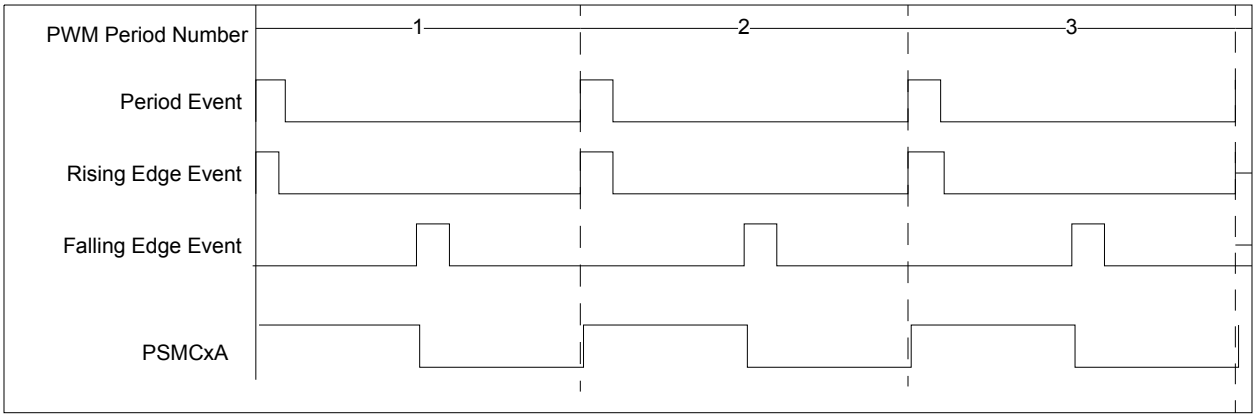
**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

* Page provides register information.

**EXAMPLE 24-1: SINGLE-PHASE SETUP**

```
; Single-phase PWM PSMC setup
; Fully synchronous operation
; Period = 10 us
; Duty cycle = 50%
    BANKSEL PSMC1CON
    MOVLW   0x02        ; set period
    MOVWF   PSMC1PRH
    MOVLW   0x7F
    MOVWF   PSMC1PRL
    MOVLW   0x01        ; set duty cycle
    MOVWF   PSMC1DCH
    MOVLW   0x3F
    MOVWF   PSMC1DCL
    CLRF    PSMC1PHH    ; no phase offset
    CLRF    PSMC1PHL
    MOVLW   0x01        ; PSMC clock=64 MHz
    MOVWF   PSMC1CLK
; output on A, normal polarity
    BSF     PSMC1STR0,P1STRA
    BCF     PSMC1POL, P1POLA
    BSF     PSMC1OEN, P1OEA
; set time base as source for all events
    BSF     PSMC1PRS, P1PRST
    BSF     PSMC1PHS, P1PHST
    BSF     PSMC1DCS, P1DCST
; enable PSMC in Single-Phase Mode
; this also loads steering and time buffers
    MOVLW   B'11000000'
    MOVWF   PSMC1CON
    BANKSEL TRISC
    BCF     TRISC, 0    ; enable pin driver
```

**FIGURE 24-4: SINGLE PWM WAVEFORM – PSMCXSTR0 = 01H**



### 24.3.9 ECCP COMPATIBLE FULL-BRIDGE PWM

This mode of operation is designed to match the Full-Bridge mode from the ECCP module. It is called ECCP compatible as the term “full-bridge” alone has different connotations in regards to the output waveforms.

Full-Bridge Compatible mode uses the same waveform events as the single PWM mode to generate the output waveforms.

There are both Forward and Reverse modes available for this operation, again to match the ECCP implementation. Direction is selected with the mode control bits.

#### 24.3.9.1 Mode Features

- Dead-band control available on direction switch
  - Changing from forward to reverse uses the falling edge dead-band counters.
  - Changing from reverse to forward uses the rising edge dead-band counters.
- No steering control available
- PWM is output on the following four pins only:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD

#### 24.3.9.2 Waveform Generation - Forward

In this mode of operation, three of the four pins are static. PSMCxA is the only output that changes based on rising edge and falling edge events.

Static Signal Assignment

- Outputs set to active state
  - PSMCxD
- Outputs set to inactive state
  - PSMCxB
  - PSMCxC

Rising Edge Event

- PSMCxA is set active

Falling Edge Event

- PSMCxA is set inactive

#### 24.3.9.3 Waveform Generation – Reverse

In this mode of operation, three of the four pins are static. Only PSMCxB toggles based on rising edge and falling edge events.

Static Signal Assignment

- Outputs set to active state
  - PSMCxC
- Outputs set to inactive state
  - PSMCxA
  - PSMCxD

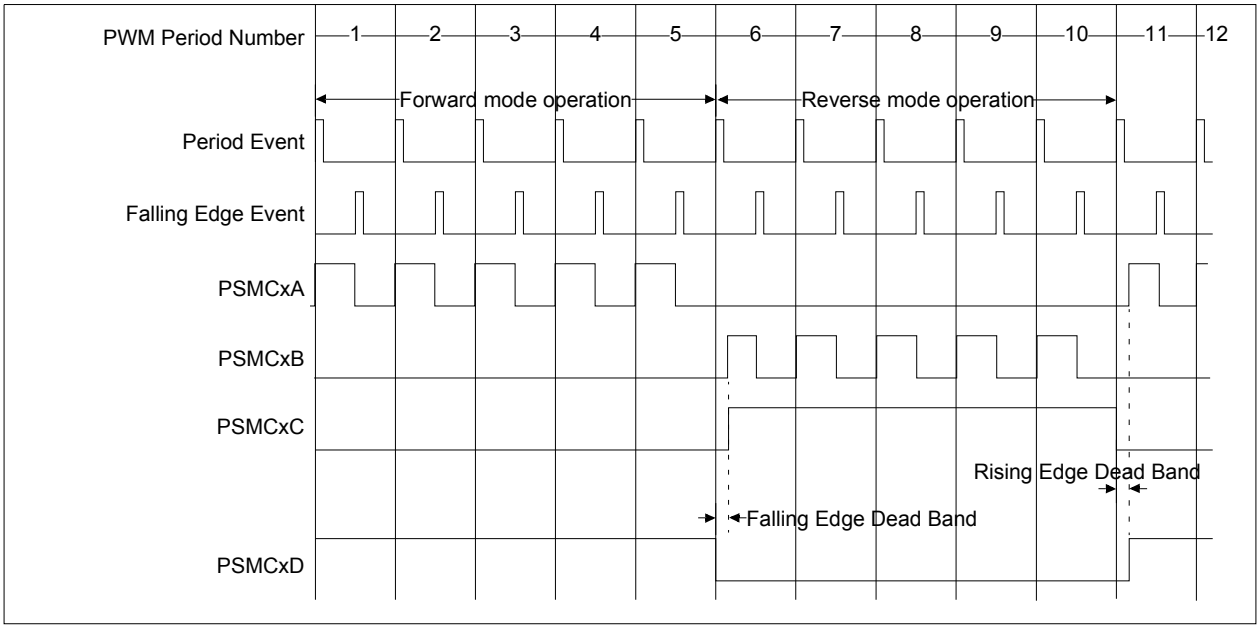
Rising Edge Event

- PSMCxB is set active

Falling Edge Event

- PSMCxB is set inactive

**FIGURE 24-12: ECCP COMPATIBLE FULL-BRIDGE PWM WAVEFORM – PSMCXSTR0 = 0FH**



**REGISTER 24-33: PSMCxINT: PSMC TIME BASE INTERRUPT CONTROL REGISTER**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| PxTOVIE | PxTPHIE | PxTDCIE | PxTPRIE | PxTOVIF | PxTPHIF | PxTDCIF | PxTPRIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7 **PxTOVIE**: PSMC Time Base Counter Overflow Interrupt Enable bit
1 = Time base counter overflow interrupts are enabled
0 = Time base counter overflow interrupts are disabled

bit 6 **PxTPHIE**: PSMC Time Base Phase Interrupt Enable bit
1 = Time base phase match interrupts are enabled
0 = Time base phase match interrupts are disabled

bit 5 **PxTDCIE**: PSMC Time Base Duty Cycle Interrupt Enable bit
1 = Time base duty cycle match interrupts are enabled
0 = Time base duty cycle match interrupts are disabled

bit 4 **PxTPRIE**: PSMC Time Base Period Interrupt Enable bit
1 = Time base period match interrupts are enabled
0 = Time base period match Interrupts are disabled

bit 3 **PxTOVIF**: PSMC Time Base Counter Overflow Interrupt Flag bit
1 = The 16-bit PSMCxTMR has overflowed from FFFFh to 0000h
0 = The 16-bit PSMCxTMR counter has not overflowed

bit 2 **PxTPHIF**: PSMC Time Base Phase Interrupt Flag bit
1 = The 16-bit PSMCxTMR counter has matched PSMCxPH<15:0>
0 = The 16-bit PSMCxTMR counter has not matched PSMCxPH<15:0>

bit 1 **PxTDCIF**: PSMC Time Base Duty Cycle Interrupt Flag bit
1 = The 16-bit PSMCxTMR counter has matched PSMCxDC<15:0>
0 = The 16-bit PSMCxTMR counter has not matched PSMCxDC<15:0>

bit 0 **PxTPRIF**: PSMC Time Base Period Interrupt Flag bit
1 = The 16-bit PSMCxTMR counter has matched PSMCxPR<15:0>
0 = The 16-bit PSMCxTMR counter has not matched PSMCxPR<15:0>

## 25.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 25-3 shows a typical waveform of the PWM signal.

### 25.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 25-4 shows a simplified block diagram of PWM operation.

| | |
|---|---|
| **Note 1:** | The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin. |
| **2:** | Clearing the CCPxCON register will relinquish control of the CCPx pin. |

**FIGURE 25-3: CCP PWM OUTPUT SIGNAL**

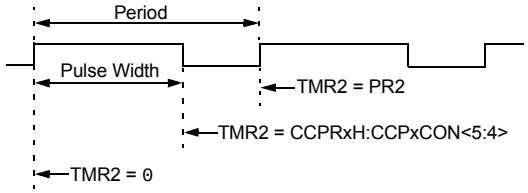
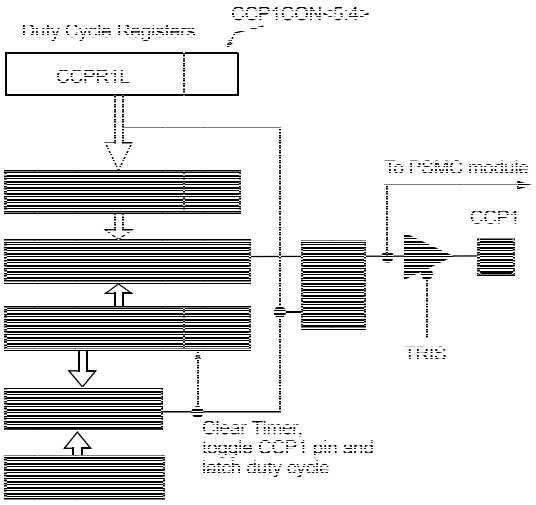


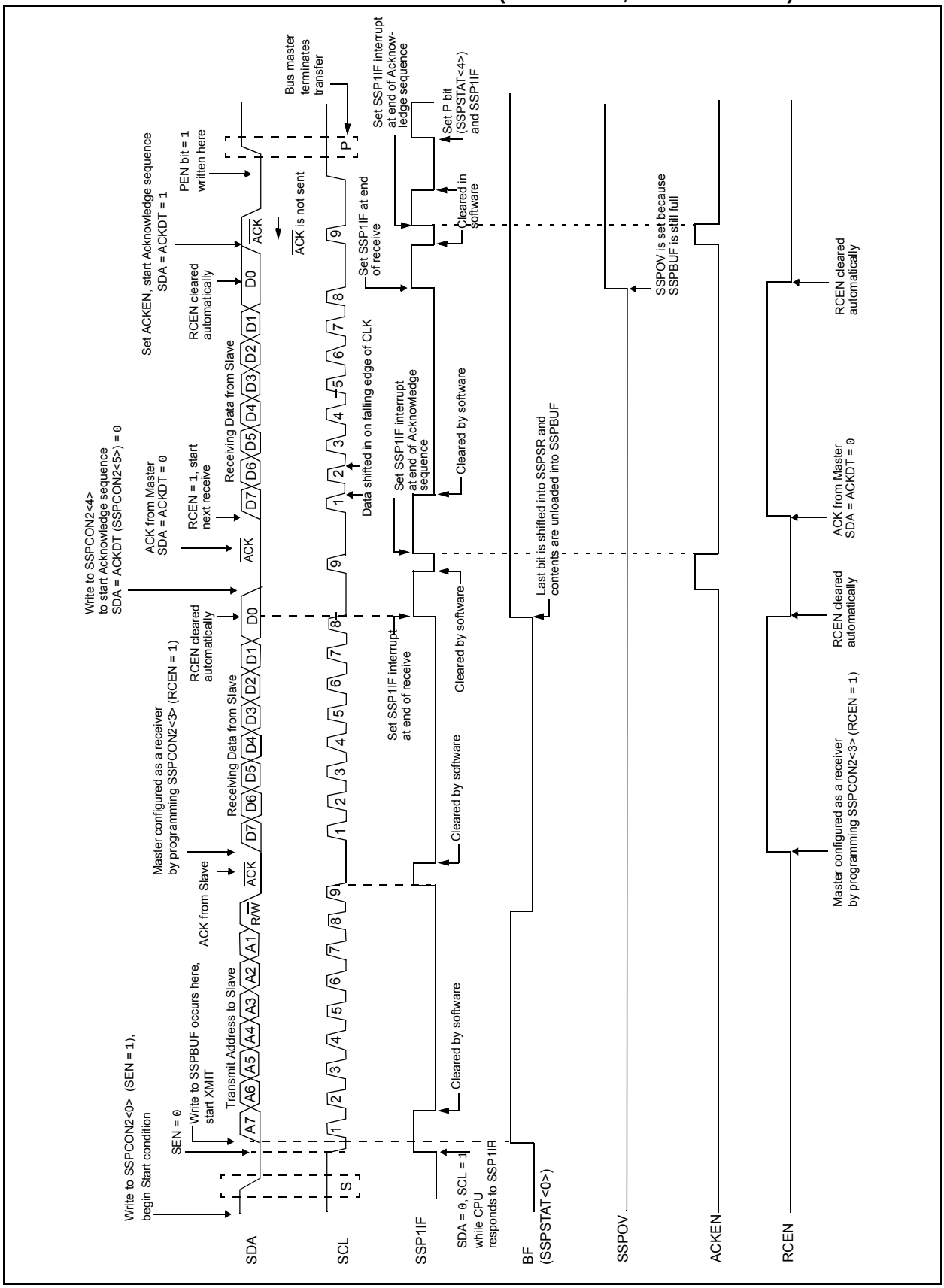

**FIGURE 25-4: SIMPLIFIED PWM BLOCK DIAGRAM**




Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPR1H is a read-only register.

**FIGURE 26-29: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)**



## 27.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 27-1 and Figure 27-2.

**FIGURE 27-1: EUSART TRANSMIT BLOCK DIAGRAM**

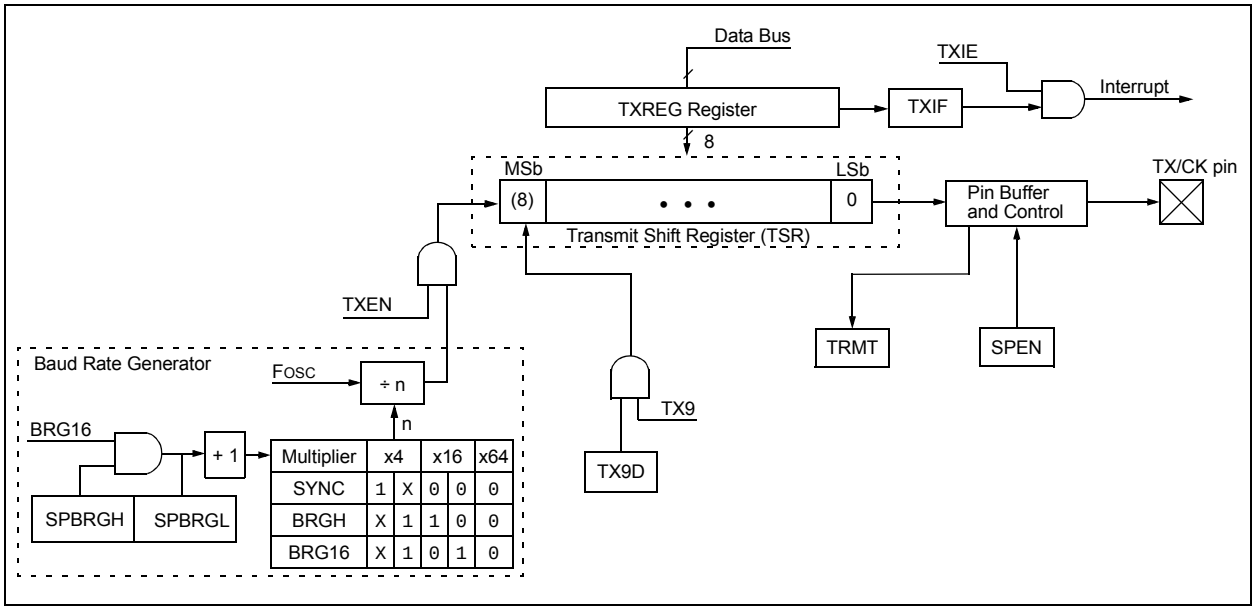
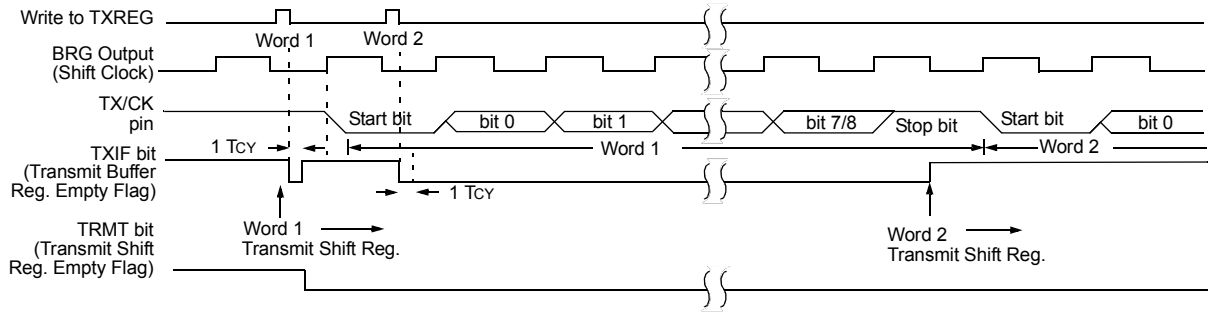


**FIGURE 27-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)**




**Note:** This timing diagram shows two consecutive transmissions.

**TABLE 27-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| APFCON1 | C2OUTSEL | CC1PSEL | SDOSEL | SCKSEL | SDISEL | TXSEL | RXSEL | CCP2SEL | 127 |
| BAUDCON | ABDOVF | RCIDL | — | SCKP | BRG16 | — | WUE | ABDEN | 347 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 94 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 346 |
| SPBRGL | BRG<7:0> | | | | | | | | 348 |
| SPBRGH | BRG<15:8> | | | | | | | | 348 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 142 |
| TXREG | EUSART Transmit Data Register | | | | | | | | 337* |
| TXSTA | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D | 345 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous transmission.

* Page provides register information.

| TRIS | Load TRIS Register with W |
|---|---|
| Syntax: | [ *label* ] TRIS f |
| Operands: | $5 \leq f \leq 7$ |
| Operation: | (W) $\rightarrow$ TRIS register 'f' |
| Status Affected: | None |
| Description: | Move data from W register to TRIS register.<br>When 'f' = 5, TRISA is loaded.<br>When 'f' = 6, TRISB is loaded.<br>When 'f' = 7, TRISC is loaded. |

| XORLW | Exclusive OR literal with W |
|---|---|
| Syntax: | [ *label* ] XORLW k |
| Operands: | $0 \leq k \leq 255$ |
| Operation: | (W) .XOR. k $\rightarrow$ (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register. |

| XORWF | Exclusive OR W with f |
|---|---|
| Syntax: | [ *label* ] XORWF f,d |
| Operands: | $0 \leq f \leq 127$<br>$d \in [0,1]$ |
| Operation: | (W) .XOR. (f) $\rightarrow$ (destination) |
| Status Affected: | Z |
| Description: | Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

**TABLE 30-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{MCLR}$ Pulse Width (low) | 2<br>5 | —<br>— | —<br>— | μs<br>μs | VDD = 3.3-5V, -40°C to +85°C<br>VDD = 3.3-5V |
| 31 | TWDTLP | Low-Power Watchdog Timer Time-out Period | 10 | 16 | 27 | ms | VDD = 3.3V-5V<br>1:16 Prescaler used |
| 32 | TOST | Oscillator Start-up Timer Period(1), (2) | — | 1024 | — | Tosc | **(Note 3)** |
| 33* | TPWRT | Power-up Timer Period, $\overline{PWRTE}$ = 0 | 40 | 65 | 140 | ms | |
| 34* | TIOZ | I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset | — | — | 2.0 | μs | |
| 35 | VBOR | Brown-out Reset Voltage | 2.55<br>2.30<br>1.80 | 2.70<br>2.45<br>1.90 | 2.85<br>2.6<br>2.10 | V<br>V<br>V | BORV = 0<br>BORV=1 (F device)<br>BORV=1 (LF device) |
| 35A | VLPBOR | Low-Power Brown-out | 1.8 | 2.1 | 2.5 | V | LPBOR = 1 |
| 36* | VHYST | Brown-out Reset Hysteresis | 0 | 25 | 75 | mV | -40°C to +85°C |
| 37* | TBORDC | Brown-out Reset DC Response Time | 1 | 3 | 35 | μs | VDD ≤ VBOR |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** By design.

**3:** Period of the slower clock.

**4:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

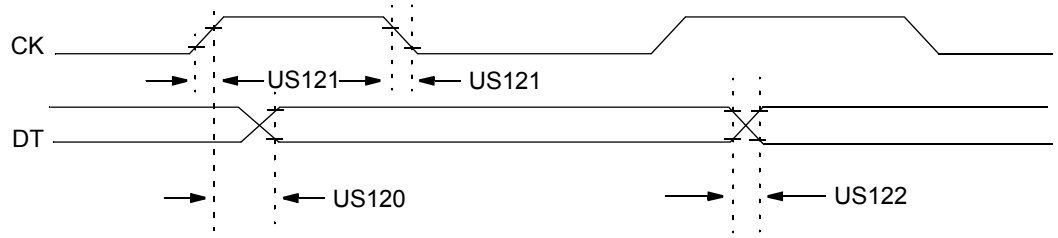
**TABLE 30-17: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS**

| **Operating Conditions:** $V_{DD}$ = 3V, Temperature = 25°C (unless otherwise stated). | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| DAC01* | $C_{LSB}$ | Step Size | — | $V_{DD}/256$ | — | V | |
| DAC02* | $C_{ACC}$ | Absolute Accuracy | — | — | ± 1.5 | LSb | |
| DAC03* | $C_R$ | Unit Resistor Value (R) | — | 600 | — | Ω | |
| DAC04* | $C_{ST}$ | Settling Time(1) | — | — | 10 | μs | |

* These parameters are characterized but not tested.

**Note 1:** Settling time measured while DACR<7:0> transitions from '0x00' to '0xFF'.

**FIGURE 30-14: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**

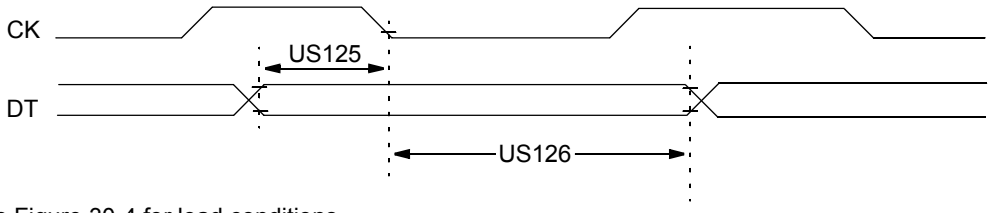



**Note:** Refer to Figure 30-4 for load conditions.

**TABLE 30-18: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS**

| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | | **Min.** | **Max.** | **Units** | **Conditions** |
| US120 | $T_{CKH2DTV}$ | SYNC XMIT (Master and Slave) Clock high to data-out valid | 3.0-5.5V | — | 80 | ns | |
| | | | 1.8-5.5V | — | 100 | ns | |
| US121 | $T_{CKRF}$ | Clock out rise time and fall time (Master mode) | 3.0-5.5V | — | 45 | ns | |
| | | | 1.8-5.5V | — | 50 | ns | |
| US122 | $T_{DTRF}$ | Data-out rise time and fall time | 3.0-5.5V | — | 45 | ns | |
| | | | 1.8-5.5V | — | 50 | ns | |

**FIGURE 30-15: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**




**Note:** Refer to Figure 30-4 for load conditions.

**Note:** Unless otherwise noted, $V_{IN}$ = 5V, $F_{OSC}$ = 300 kHz, $C_{IN}$ = 0.1 µF, $T_A$ = 25°C.

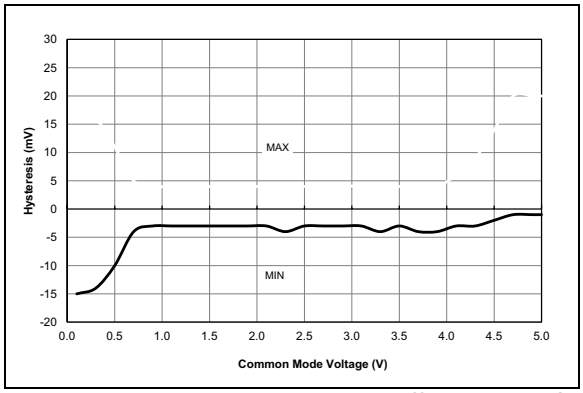



***FIGURE 31-120:*** *Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values at 25°C, PIC16F1784/6/7 Only.*

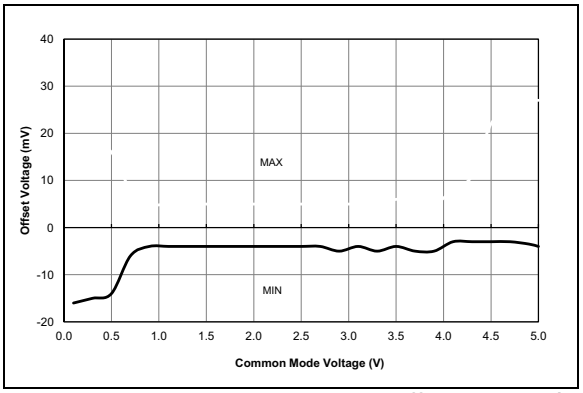



***FIGURE 31-121:*** *Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values From -40°C to 125°C, PIC16F1784/6/7 Only.*

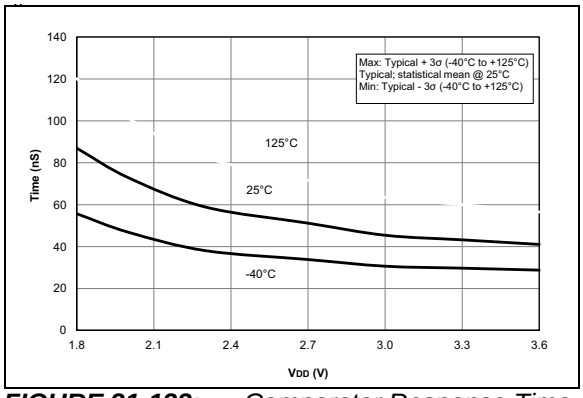



***FIGURE 31-122:*** *Comparator Response Time Over Voltage, NP Mode (CxSP = 1), Typical Measured Values, PIC16LF1784/6/7 Only.*

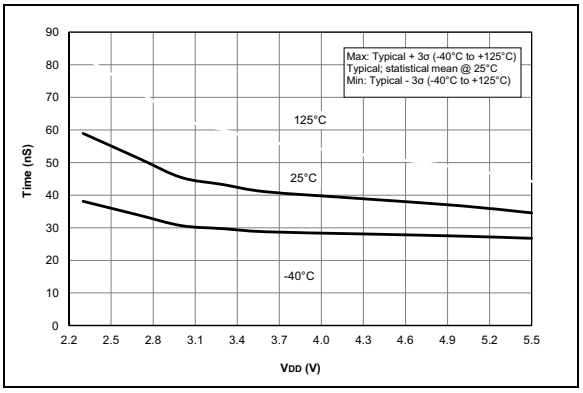



***FIGURE 31-123:*** *Comparator Response Time Over Voltage, NP Mode (CxSP = 1), Typical Measured Values, PIC16F1784/6/7 Only.*

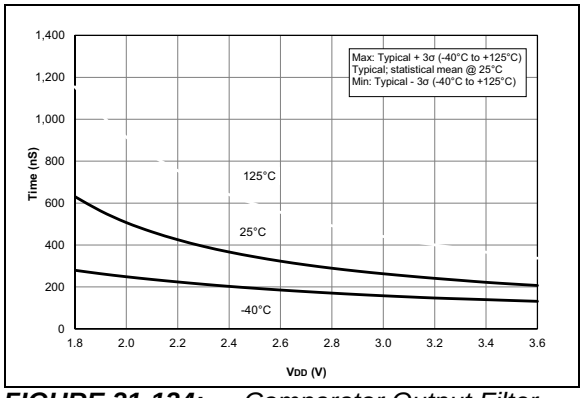



***FIGURE 31-124:*** *Comparator Output Filter Delay Time Over Temp., NP Mode (CxSP = 1), Typical Measured Values, PIC16LF1784/6/7 Only.*

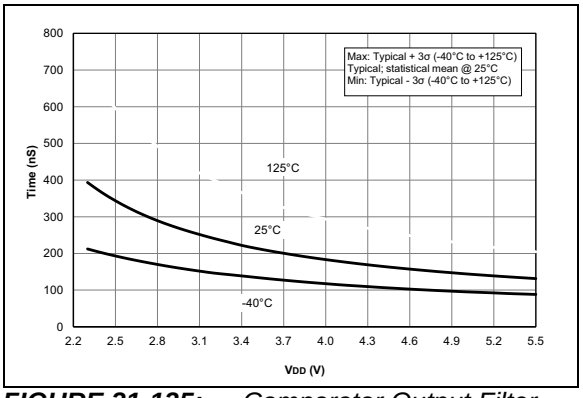
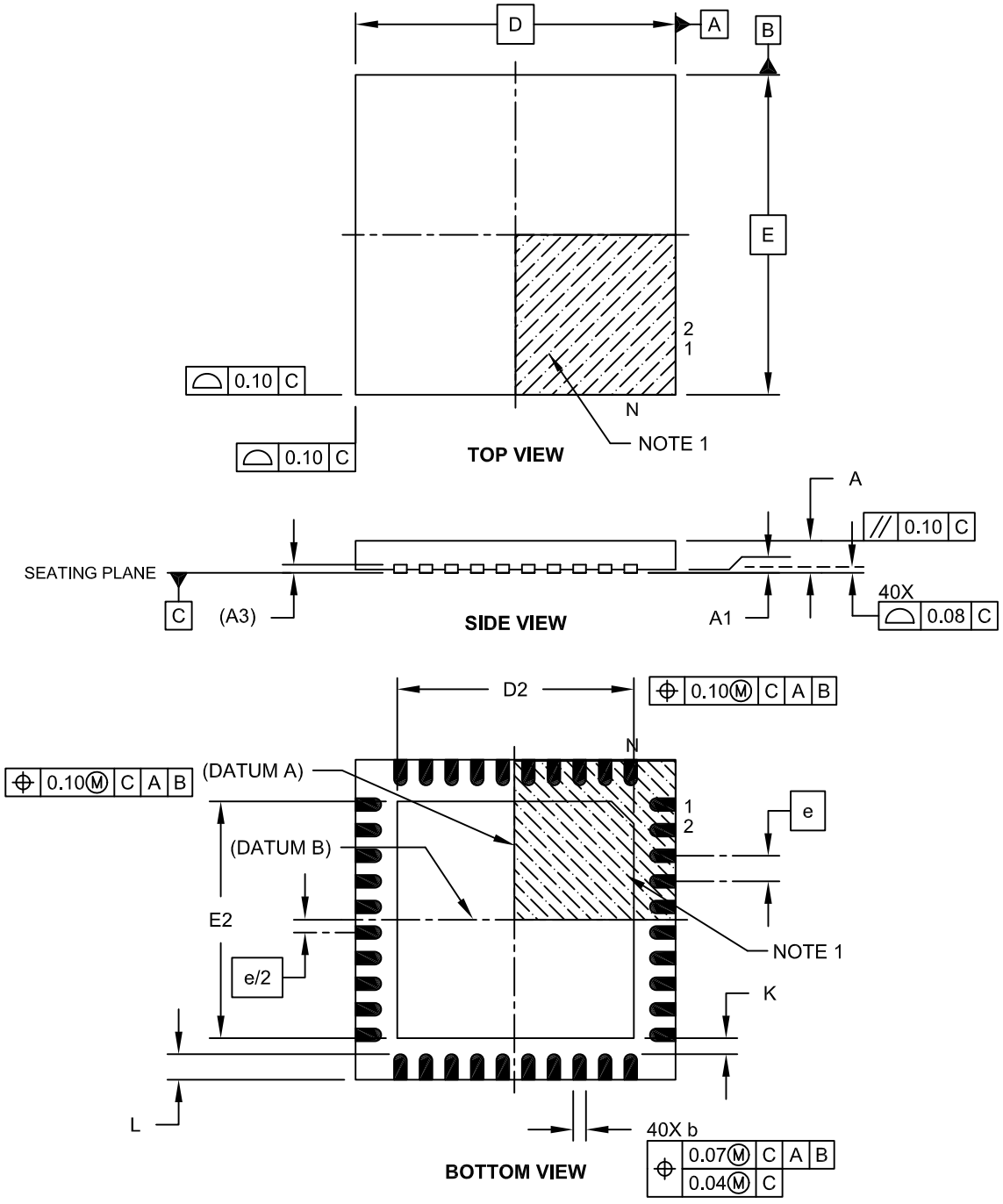



***FIGURE 31-125:*** *Comparator Output Filter Delay Time Over Temp., NP Mode (CxSP = 1), Typical Measured Values, PIC16F1784/6/7 Only.*

### 40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-156A Sheet 1 of 2

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