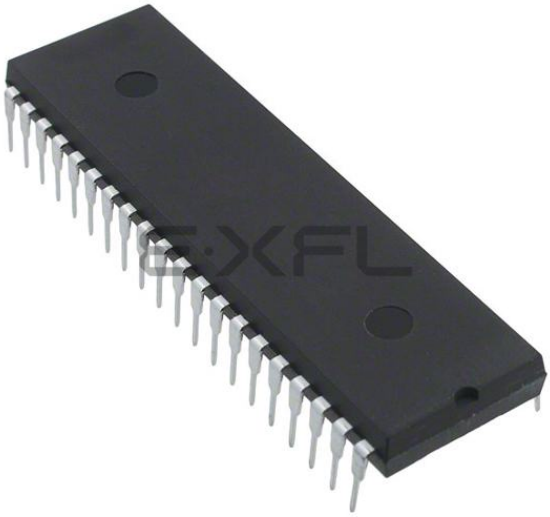

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PSMC, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 14x12b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1787-i-p |

**TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RA6/C2OUT(1)/OSC2/ CLKOUT/VCAP | RA6 | TTL/ST | CMOS | General purpose I/O. |
| | C2OUT | — | CMOS | Comparator C2 output. |
| | OSC2 | — | XTAL | Crystal/Resonator (LP, XT, HS modes). |
| | CLKOUT | — | CMOS | FOSC/4 output. |
| | VCAP | Power | Power | Filter capacitor for Voltage Regulator. |
| RA7/PSMC1CLK/PSMC2CLK/ PSMC3CLK/OSC1/CLKIN | RA7 | TTL/ST | CMOS | General purpose I/O. |
| | PSMC1CLK | ST | — | PSMC1 clock input. |
| | PSMC2CLK | ST | — | PSMC2 clock input. |
| | PSMC3CLK | ST | — | PSMC3 clock input. |
| | OSC1 | — | XTAL | Crystal/Resonator (LP, XT, HS modes). |
| | CLKIN | st | — | External clock input (EC mode). |
| RB0/AN12/C2IN1+/PSMC1IN/ PSMC2IN/PSMC3IN/CCP1(1)/ INT | RB0 | TTL/ST | CMOS | General purpose I/O. |
| | AN12 | AN | — | ADC Channel 12 input. |
| | C2IN1+ | AN | — | Comparator C2 positive input. |
| | PSMC1IN | ST | — | PSMC1 Event Trigger input. |
| | PSMC2IN | ST | — | PSMC2 Event Trigger input. |
| | PSMC3IN | ST | — | PSMC3 Event Trigger input. |
| | CCP1 | ST | CMOS | Capture/Compare/PWM1. |
| | INT | ST | — | External interrupt. |
| RB1/AN10/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/OPA2OUT | RB1 | TTL/ST | CMOS | General purpose I/O. |
| | AN10 | AN | — | ADC Channel 10 input. |
| | C1IN3- | AN | — | Comparator C1 negative input. |
| | C2IN3- | AN | — | Comparator C2 negative input. |
| | C3IN3- | AN | — | Comparator C3 negative input. |
| | C4IN3- | AN | — | Comparator C4 negative input. |
| | OPA2OUT | — | AN | Operational Amplifier 2 output. |
| RB2/AN8/OPA2IN-/CLKR | RB2 | TTL/ST | CMOS | General purpose I/O. |
| | AN8 | AN | — | ADC Channel 8 input. |
| | OPA2IN- | AN | — | Operational Amplifier 2 inverting input. |
| | CLKR | — | CMOS | Clock output. |
| RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN+/CCP2(1) | RB3 | TTL/ST | CMOS | General purpose I/O. |
| | AN9 | AN | — | ADC Channel 9 input. |
| | C1IN2- | AN | — | Comparator C1 negative input. |
| | C2IN2- | AN | — | Comparator C2 negative input. |
| | C3IN2- | AN | — | Comparator C3 negative input. |
| | OPA2IN+ | AN | — | Operational Amplifier 2 non-inverting input. |
| | CCP2 | ST | CMOS | Capture/Compare/PWM2. |
| RB4/AN11/C3IN1+ | RB4 | TTL/ST | CMOS | General purpose I/O. |
| | AN11 | AN | — | ADC Channel 11 input. |
| | C3IN1+ | AN | — | Comparator C3 positive input. |

**Legend:** AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels $I^2C$™ = Schmitt Trigger input with $I^2C$ levels
HV = High Voltage XTAL = Crystal

**Note 1:** Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
**2:** All pins have interrupt-on-change functionality.
**3:** PIC16(L)F1784/7 only.
**4:** PIC16(L)F1786 only.

**TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RC5/PSMC1F/SDO(1) | RC5 | TTL/ST | CMOS | General purpose I/O. |
| | PSMC1F | — | CMOS | PSMC1 output F. |
| | SDO | — | CMOS | SPI data output. |
| RC6/PSMC2A/TX(1)/CK(1) | RC6 | TTL/ST | CMOS | General purpose I/O. |
| | PSMC2A | — | CMOS | PSMC2 output A. |
| | TX | — | CMOS | EUSART asynchronous transmit. |
| | CK | ST | CMOS | EUSART synchronous clock. |
| RC7/PSMC2B/RX(1)/DT(1)/ C4OUT(4) | RC7 | TTL/ST | CMOS | General purpose I/O. |
| | PSMC2B | — | CMOS | PSMC2 output B. |
| | RX | ST | — | EUSART asynchronous input. |
| | DT | ST | CMOS | EUSART synchronous data. |
| | C4OUT | — | CMOS | Comparator C4 output. |
| RD0(3)/OPA3IN+ | RD0 | TTL/ST | CMOS | General purpose I/O. |
| | OPA3IN+ | AN | — | Operational Amplifier 3 non-inverting input. |
| RD1(3)/AN21/C1IN4-/C2IN4-/ C3IN4-/C4IN4-/OPA3OUT | RD1 | TTL/ST | CMOS | General purpose I/O. |
| | AN21 | AN | — | ADC Channel 21 input. |
| | C1IN4- | AN | — | Comparator C4 negative input. |
| | C2IN4- | AN | — | Comparator C4 negative input. |
| | C3IN4- | AN | — | Comparator C4 negative input. |
| | C4IN4- | AN | — | Comparator C4 negative input. |
| | OPA3OUT | — | AN | Operational Amplifier 3 output. |
| RD2(3)/OPA3IN- | RD2 | TTL/ST | CMOS | General purpose I/O. |
| | OPA3IN- | AN | — | Operational Amplifier 3 inverting input. |
| RD3(3) | RD3 | TTL/ST | CMOS | General purpose I/O. |
| RD4(3)/PSMC3F | RD4 | TTL/ST | CMOS | General purpose I/O. |
| | PSMC3F | — | CMOS | PSMC3 output F. |
| RD5(3)/PSMC3E | RD5 | TTL/ST | CMOS | General purpose I/O. |
| | PSMC3E | — | CMOS | PSMC3 output E. |
| RD6(3)/C3OUT/PSMC3D | RD6 | TTL/ST | CMOS | General purpose I/O. |
| | C3OUT | — | CMOS | Comparator C3 output. |
| | PSMC3D | — | CMOS | PSMC3 output D. |
| RD7(3)/C4OUT/PSMC3C | RD6 | TTL/ST | CMOS | General purpose I/O. |
| | C4OUT | — | CMOS | Comparator C4 output. |
| | PSMC3C | — | CMOS | PSMC3 output C. |
| RE0(3)/AN5/CCP3(1) | RE0 | TTL/ST | — | General purpose input. |
| | AN5 | AN | — | ADC Channel 5 input. |
| | CCP3 | ST | CMOS | Capture/Compare/PWM3. |
| RE1(3)/AN6/PSMC3B | RE1 | TTL/ST | CMOS | General purpose I/O. |
| | AN6 | AN | — | ADC Channel 6 input. |
| | PSMC3B | — | CMOS | PSMC3 output B. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$™ = Schmitt Trigger input with $I^2C$ levels
HV = High Voltage; XTAL = Crystal

**Note 1:** Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
**2:** All pins have interrupt-on-change functionality.
**3:** PIC16(L)F1784/7 only.
**4:** PIC16(L)F1786 only.

**TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 2** | | | | | | | | | | | |
| 10Ch | LATA | PORTA Data Latch | | | | | | | | xxxx xxxx | uuuu uuuu |
| 10Dh | LATB | PORTB Data Latch | | | | | | | | xxxx xxxx | uuuu uuuu |
| 10Eh | LATC | PORTC Data Latch | | | | | | | | xxxx xxxx | uuuu uuuu |
| 10Fh | LATD(3) | PORTD Data Latch | | | | | | | | xxxx xxxx | uuuu uuuu |
| 110h | LATE(3) | — | — | — | — | — | LATE2 | LATE1 | LATE0 | ---- -111 | ---- -111 |
| 111h | CM1CON0 | C1ON | C1OUT | C1OE | C1POL | C1ZLF | C1SP | C1HYS | C1SYNC | 0000 0100 | 0000 0100 |
| 112h | CM1CON1 | C1INTP | C1INTN | C1PCH<2:0> | | | C1NCH<2:0> | | | 0000 0000 | 0000 0000 |
| 113h | CM2CON0 | C2ON | C2OUT | C2OE | C2POL | C2ZLF | C2SP | C2HYS | C2SYNC | 0000 0100 | 0000 0100 |
| 114h | CM2CON1 | C2INTP | C2INTN | C2PCH<2:0> | | | C2NCH<2:0> | | | 0000 0000 | 0000 0000 |
| 115h | CMOUT | — | — | — | — | MC4OUT(3) | MC3OUT | MC2OUT | MC1OUT | ---- 0000 | ---- 0000 |
| 116h | BORCON | SBOREN | BORFS | — | — | — | — | — | BORRDY | 1x-- ---q | uu-- ---u |
| 117h | FVRCON | FVREN | FVRRDY | TSEN | TSRNG | CDAFVR<1:0> | | ADFVR<1:0> | | 0q00 0000 | 0q00 0000 |
| 118h | DAC1CON0 | DAC1EN | --- | DAC1OE1 | DAC1OE2 | DAC1PSS<1:0> | | --- | DAC1NSS | 0-00 00-0 | 0-00 00-0 |
| 119h | DAC1CON1 | DAC1R<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 11Ah | CM4CON0 | C4ON | C4OUT | C4OE | C4POL | C4ZLF | C4SP | C4HYS | C4SYNC | 0000 0100 | 0000 0100 |
| 11Bh | CM4CON1 | C4INTP | C4INTN | C4PCH<1:0> | | — | — | C4NCH<1:0> | | 0000 --00 | 0000 --00 |
| 11Ch | APFCON2 | — | — | — | — | — | — | — | CCP3SEL | ---- ---0 | ---- ---0 |
| 11Dh | APFCON1 | C2OUTSEL | CC1PSEL | SDOSEL | SCKSEL | SDISEL | TXSEL | RXSEL | CCP2SEL | 0000 0000 | 0000 0000 |
| 11Eh | CM3CON0 | C3ON | C3OUT | C3OE | C3POL | C3ZLF | C3SP | C3HYS | C3SYNC | 0000 0100 | 0000 0100 |
| 11Fh | CM3CON1 | C3INTP | C3INTN | C3PCH<2:0> | | | C3NCH<2:0> | | | 0000 0000 | 0000 0000 |
| **Bank 3** | | | | | | | | | | | |
| 18Ch | ANSELA | ANSA7 | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | 1-11 1111 | 1-11 1111 |
| 18Dh | ANSELB | — | ANSB6 | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 | -111 1111 | -111 1111 |
| 18Eh | Unimplemented | | | | | | | | — | — | — |
| 18Fh | ANSELD(3) | — | — | — | — | — | ANSD2 | ANSD1 | ANSD0 | ---- -111 | ---- -111 |
| 190h | ANSELE(3) | — | — | — | — | — | ANSE2 | ANSE1 | ANSE0 | ---- -111 | ---- -111 |
| 191h | EEADRL | EEPROM / Program Memory Address Register Low Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 192h | EEADRH | —(2) | EEPROM / Program Memory Address Register High Byte | | | | | | | 1000 0000 | 1000 0000 |
| 193h | EEDATL | EEPROM / Program Memory Read Data Register Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| 194h | EEDATH | — | — | EEPROM / Program Memory Read Data Register High Byte | | | | | | --xx xxxx | --uu uuuu |
| 195h | EECON1 | EEPGD | CFGS | LWLO | FREE | WRERR | WREN | WR | RD | 0000 x000 | 0000 q000 |
| 196h | EECON2 | EEPROM / Program Memory Control Register 2 | | | | | | | | 0000 0000 | 0000 0000 |
| 197h | VREGCON(4) | — | — | — | — | — | — | VREGPM | Reserved | ---- --01 | ---- --01 |
| 198h | — | Unimplemented | | | | | | | | — | — |
| 199h | RCREG | EUSART Receive Data Register | | | | | | | | 0000 0000 | 0000 0000 |
| 19Ah | TXREG | EUSART Transmit Data Register | | | | | | | | 0000 0000 | 0000 0000 |
| 19Bh | SPBRG | BRG<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 19Ch | SPBRGH | BRG<15:8> | | | | | | | | 0000 0000 | 0000 0000 |
| 19Dh | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 0000 | 0000 0000 |
| 19Eh | TXSTA | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D | 0000 0010 | 0000 0010 |
| 19Fh | BAUDCON | ABDOVF | RCIDL | — | SCKP | BRG16 | — | WUE | ABDEN | 01-0 0-00 | 01-0 0-00 |

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

**Note 1:** These registers can be addressed from any bank.
**2:** Unimplemented, read as '1'.
**3:** PIC16(L)F1784/7 only.
**4:** PIC16F1784/6/7 only.

## 4.6 Device ID and Revision ID

The memory location 8006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See **Section 12.5 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

## 4.7 Register Definitions: Device and Revision

**REGISTER 4-3: DEVID: DEVICE ID REGISTER**

| R | R | R | R | R | R |
|---|---|---|---|---|---|
| DEV<8:3> | | | | | |
| bit 13 | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEV<2:0> | | | REV<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | |
|---|---|
| R = Readable bit | |
| '1' = Bit is set | '0' = Bit is cleared |

bit 13-5 **DEV<8:0>:** Device ID bits

| Device | DEVICEID<13:0> Values | |
|---|---|---|
| | DEV<8:0> | REV<4:0> |
| PIC16F1784 | 10 1010 010 | x xxxx |
| PIC16LF1784 | 10 1010 111 | x xxxx |
| PIC16F1786 | 10 1010 011 | x xxxx |
| PIC16LF1786 | 10 1011 000 | x xxxx |
| PIC16F1787 | 10 1010 100 | x xxxx |
| PIC16LF1787 | 10 1011 001 | x xxxx |

bit 4-0 **REV<4:0>:** Revision ID bits

These bits are used to identify the revision (see Table under DEV<8:0> above).

## 5.4 Low-Power Brown-Out Reset (LPBOR)

The Low-Power Brown-Out Reset (LPBOR) is an essential part of the Reset subsystem. Refer to Figure 5-1 to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external VDD pin. When too low of a voltage is detected, the device is held in Reset. When this occurs, a register bit ($\overline{BOR}$) is changed to indicate that a BOR Reset has occurred. The same bit is set for both the BOR and the LPBOR. Refer to Register 5-2.

### 5.4.1 ENABLING LPBOR

The LPBOR is controlled by the $\overline{LPBOR}$ bit of Configuration Words. When the device is erased, the LPBOR module defaults to disabled.

#### 5.4.1.1 LPBOR Module Output

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. This signal is OR'd together with the Reset signal of the BOR module to provide the generic $\overline{BOR}$ signal, which goes to the PCON register and to the power control block.

## 5.5 $\overline{MCLR}$

The $\overline{MCLR}$ is an optional external input that can reset the device. The $\overline{MCLR}$ function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 5-2).

**TABLE 5-2: $\overline{MCLR}$ CONFIGURATION**

| MCLRE | LVP | $\overline{MCLR}$ |
|---|---|---|
| 0 | 0 | Disabled |
| 1 | 0 | Enabled |
| x | 1 | Enabled |

### 5.5.1 $\overline{MCLR}$ ENABLED

When $\overline{MCLR}$ is enabled and the pin is held low, the device is held in Reset. The $\overline{MCLR}$ pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

**Note:** A Reset does not drive the $\overline{MCLR}$ pin low.

### 5.5.2 $\overline{MCLR}$ DISABLED

When $\overline{MCLR}$ is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See **Section 13.11 "PORTE Registers"** for more information.

## 5.6 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the WDT Reset. See **Section 11.0 "Watchdog Timer (WDT)"** for more information.

## 5.7 RESET Instruction

A RESET instruction will cause a device Reset. The $\overline{RI}$ bit in the PCON register will be set to '0'. See Table 5-4 for default conditions after a RESET instruction has occurred.

## 5.8 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See **Section 5.8 "Stack Overflow/Underflow Reset"** for more information.

## 5.9 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

## 5.10 Power-Up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the $\overline{PWRTE}$ bit of Configuration Words.

## 5.11 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for oscillator source).
3. $\overline{MCLR}$ must be released (if enabled).

The total time-out will vary based on oscillator configuration and Power-up Timer configuration. See **Section 6.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information.

The Power-up Timer and oscillator start-up timer run independently of $\overline{MCLR}$ Reset. If $\overline{MCLR}$ is kept low long enough, the Power-up Timer and oscillator start-up timer will expire. Upon bringing $\overline{MCLR}$ high, the device will begin execution immediately (see Figure 5-3). This is useful for testing purposes or to synchronize more than one device operating in parallel.

**REGISTER 6-2: OSCSTAT: OSCILLATOR STATUS REGISTER**

| R-1/q | R-0/q | R-q/q | R-0/q | R-0/q | R-q/q | R-0/0 | R-0/q |
|---|---|---|---|---|---|---|---|
| T1OSCR | PLLR | OSTS | HFIOFR | HFIOFL | MFIOFR | LFIOFR | HFIOFS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | q = Conditional |

bit 7 **T1OSCR:** Timer1 Oscillator Ready bit
If T1OSCEN = 1:
1 = Timer1 oscillator is ready
0 = Timer1 oscillator is not ready
If T1OSCEN = 0:
1 = Timer1 clock source is always ready

bit 6 **PLLR** 4x PLL Ready bit
1 = 4x PLL is ready
0 = 4x PLL is not ready

bit 5 **OSTS:** Oscillator Start-up Timer Status bit
1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Words
0 = Running from an internal oscillator (FOSC<2:0> = 100)

bit 4 **HFIOFR:** High-Frequency Internal Oscillator Ready bit
1 = HFINTOSC is ready
0 = HFINTOSC is not ready

bit 3 **HFIOFL:** High-Frequency Internal Oscillator Locked bit
1 = HFINTOSC is at least 2% accurate
0 = HFINTOSC is not 2% accurate

bit 2 **MFIOFR:** Medium-Frequency Internal Oscillator Ready bit
1 = MFINTOSC is ready
0 = MFINTOSC is not ready

bit 1 **LFIOFR:** Low-Frequency Internal Oscillator Ready bit
1 = LFINTOSC is ready
0 = LFINTOSC is not ready

bit 0 **HFIOFS:** High-Frequency Internal Oscillator Stable bit
1 = HFINTOSC is at least 0.5% accurate
0 = HFINTOSC is not 0.5% accurate

## 8.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIE1 or PIE2 registers)

The INTCON, PIR1 and PIR2 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See **"Section 8.5 "Automatic Context Saving"."**)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

| | |
|---|---|
| **Note 1:** | Individual interrupt flag bits are set, regardless of the state of any other enable bits. |
| **2:** | All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again. |

## 8.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is three or four instruction cycles. For asynchronous interrupts, the latency is three to five instruction cycles, depending on when the interrupt occurs. See Figure 8-2 and Figure 8.3 for more details.

**REGISTER 13-36: LATE: PORTE DATA LATCH REGISTER(2)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x/u | R/W-x/u | R/W-x/u |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | LATE2 | LATE1 | LATE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-3 **Unimplemented**: Read as ‘0’

bit 2-0 **LATE<2:0>**: PORTE Output Latch Value bits(2)

**Note 1:** Writes to PORTE are actually written to corresponding LATE register. Reads from PORTE register is return of actual I/O pin values.

**2:** LATE<2:0> are available on PIC16(L)F1784/7 only.

**REGISTER 13-37: ANSELE: PORTE ANALOG SELECT REGISTER(2)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | ANSE2 | ANSE1 | ANSE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ANSE<2:0>**: Analog Select between Analog or Digital Function on pins RE<2:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**2:** ANSELE<2:0> are available on PIC16(L)F1784/7 only.

**TABLE 16-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on page |
|---|---|---|---|---|---|---|---|---|---|
| FVRCON | FVREN | FVRRDY | TSEN | TSRNG | — | — | ADFVR<1:0> | | 161 |

**Legend:** Shaded cells are unused by the temperature indicator module.

## 24.0 PROGRAMMABLE SWITCH MODE CONTROL (PSMC)

The Programmable Switch Mode Controller (PSMC) is a high-performance Pulse Width Modulator (PWM) that can be configured to operate in one of several modes to support single or multiple phase applications.

A simplified block diagram indicating the relationship between inputs, outputs, and controls is shown in Figure 24-1.

This section begins with the fundamental aspects of the PSMC operation. A more detailed description of operation for each mode is located later in **Section 24.3 "Modes of Operation"**

Modes of operation include:

- Single-phase
- Complementary Single-phase
- Push-Pull
- Push-Pull 4-Bridge
- Complementary Push-Pull 4-Bridge
- Pulse Skipping
- Variable Frequency Fixed Duty Cycle
- Complementary Variable Frequency Fixed Duty Cycle
- ECCP Compatible modes
  - Full-Bridge
  - Full-Bridge Reverse
- 3-Phase 6-Step PWM

### 24.2.6 CLOCK PRESCALER

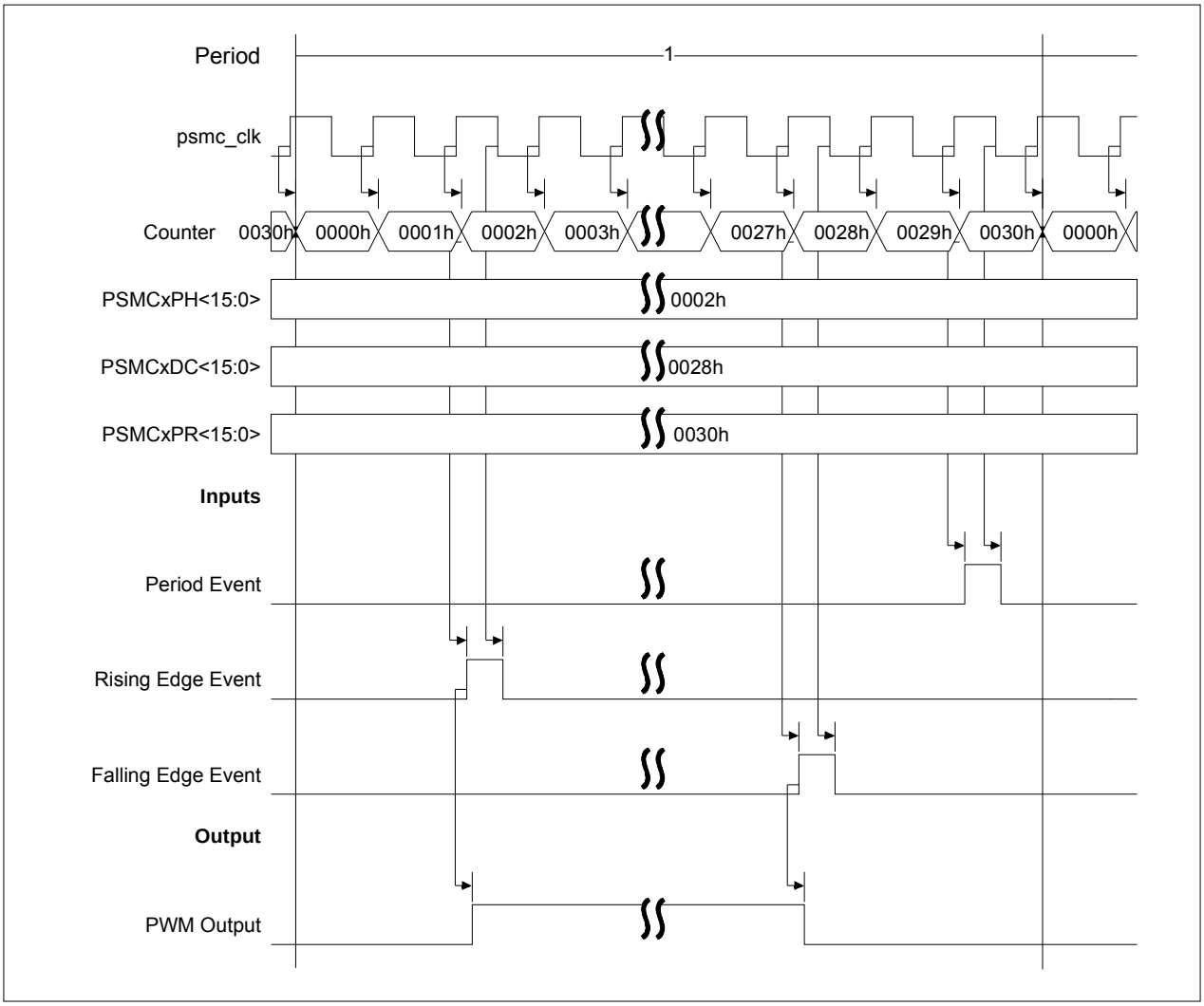
There are four prescaler choices available to be applied to the selected clock:

- Divide by 1
- Divide by 2
- Divide by 4
- Divide by 8

The clock source is selected with the PxCPRE<1:0> bits of the PSMCx Clock Control (PSMCxCLK) register (Register 24-6).

The prescaler output is psmc_clk, which is the clock used by all of the other portions of the PSMC module.

**FIGURE 24-3: TIME BASE WAVEFORM GENERATION**



**REGISTER 24-26: PSMCxDBR: PSMC RISING EDGE DEAD-BAND TIME REGISTER**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| PSMCxDBR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **PSMCxDBR<7:0>:** Rising Edge Dead-Band Time bits
= Unsigned number of PSMCx psmc_clk clock periods in rising edge dead band

**REGISTER 24-27: PSMCxDBF: PSMC FALLING EDGE DEAD-BAND TIME REGISTER**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| PSMCxDBF<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **PSMCxDBF<7:0>:** Falling Edge Dead-Band Time bits
= Unsigned number of PSMCx psmc_clk clock periods in falling edge dead band

**REGISTER 24-28: PSMCxFFA: PSMC FRACTIONAL FREQUENCY ADJUST REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | PSMCxFFA<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **PSMCxFFA<3:0>:** Fractional Frequency Adjustment bits
= Unsigned number of fractional PSMCx psmc_clk clock periods to add to each period event time. The fractional time period = 1/(16*psmc_clk)

**TABLE 24-5: SUMMARY OF REGISTERS ASSOCIATED WITH PSMC**

| Name | Bit7 | Bit6 | Bit5 | Bit4 | BIt3 | Bit2 | Bit1 | Bit0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| ODCONC | ODC7 | ODC6 | ODC5 | ODC4 | ODC3 | ODC2 | ODC1 | ODC0 | 143 |
| PIE4 | — | PSMC3TIE | PSMC2TIE | PSMC1TIE | — | PSMC3SIE | PSMC2SIE | PSMC1SIE | 97 |
| PIR4 | — | PSMC3TIF | PSMC2TIF | PSMC1TIF | — | PSMC3SIF | PSMC2SIF | PSMC1SIF | 101 |
| PSMCxASDC | PxASE | PxASDEN | PxARSEN | — | — | — | — | PxASDOV | 257 |
| PSMCxASDL | — | — | PxASDLF(1) | PxASDLE(1) | PxASDLD(1) | PxASDLC(1) | PxASDLB | PxASDLA | 258 |
| PSMCxASDS | PxASDSIN | — | — | PxASDSC4 | PxASDSC3 | PxASDSC2 | PxASDSC1 | — | 259 |
| PSMCxBLKF | PSMCxBLKF<7:0> | | | | | | | | 265 |
| PSMCxBLKR | PSMCxBLKR<7:0> | | | | | | | | 265 |
| PSMCxBLNK | — | — | PxFEBM1 | PxFEBM0 | — | — | PxREBM1 | PxREBM0 | 252 |
| PSMCxCLK | — | — | PxCPRE<1:0> | | — | — | PxCSRC<1:0> | | 251 |
| PSMCxCON | PSMCxEN | PSMCxLD | PxDBFE | PxDBRE | PxMODE<3:0> | | | | 247 |
| PSMCxDBF | PSMCxDBF<7:0> | | | | | | | | 264 |
| PSMCxDBR | PSMCxDBR<7:0> | | | | | | | | 264 |
| PSMCxDCH | PSMCxDC<15:8> | | | | | | | | 262 |
| PSMCxDCL | PSMCxDC<7:0> | | | | | | | | 262 |
| PSMCxDCS | PxDCSIN | — | — | PxDCSC4 | PxDCSC3 | PxDCSC2 | PxDCSC1 | PxDCST | 255 |
| PSMCxFEBS | PxFEBSIN | — | — | PxFEBSC4 | PxFEBSC3 | PxFEBSC2 | PxFEBSC1 | — | 253 |
| PSMCxFFA | — | — | — | — | PSMCxFFA<3:0> | | | | 264 |
| PSMCxINT | PxTOVIE | PxTPHIE | PxTDCIE | PxTPRIE | PxTOVIF | PxTPHIF | PxTDCIF | PxTPRIF | 269 |
| PSMCxMDL | PxMDLEN | PxMDLPOL | PxMDLBIT | — | PxMSRC<3:0> | | | | 248 |
| PSMCxOEN | — | — | PxOEF(1) | PxOEE(1) | PxOED(1) | PxOEC(1) | PxOEB | PxOEA | 251 |
| PSMCxPHH | PSMCxPH<15:8> | | | | | | | | 261 |
| PSMCxPHL | PSMCxPH<7:0> | | | | | | | | 261 |
| PSMCxPHS | PxPHSIN | — | — | PxPHSC4 | PxPHSC3 | PxPHSC2 | PxPHSC1 | PxPHST | 254 |
| PSMCxPOL | — | PxPOLIN | PxPOLF(1) | PxPOLE(1) | PxPOLD(1) | PxPOLC(1) | PxPOLB | PxPOLA | 252 |
| PSMCxPRH | PSMCxPR<15:8> | | | | | | | | 263 |
| PSMCxPRL | PSMCxPR<7:0> | | | | | | | | 263 |
| PSMCxPRS | PxPRSIN | — | — | PxPRSC4 | PxPRSC3 | PxPRSC2 | PxPRSC1 | PxPRST | 256 |
| PSMCxREBS | PxREBSIN | — | — | PxREBSC4 | PxREBSC3 | PxREBSC2 | PxREBSC1 | — | 253 |
| PSMCxSTR0 | — | — | PxSTRF(1) | PxSTRE(1) | PxSTRD(1) | PxSTRC(1) | PxSTRB | PxSTRA | 266 |
| PSMCxSTR1 | PxSSYNC | — | — | — | — | — | PxLSMEN | PxHSMEN | 268 |
| PSMCxSYNC | PxPOFST | PxPRPOL | PxDCPOL | — | — | — | PxSYNC<1:0> | | 249 |
| PSMCxTMRH | PSMCxTMR<15:8> | | | | | | | | 260 |
| PSMCxTMRL | PSMCxTMR<7:0> | | | | | | | | 260 |
| SLRCONC | SLRC7 | SLRC6 | SLRC5 | SLRC4 | SLRC3 | SLCR2 | SRC1 | SLRC0 | 143 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 142 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by PSMC module.

**Note 1:** Unimplemented in PSMC2.

### 26.5.8 GENERAL CALL ADDRESS SUPPORT

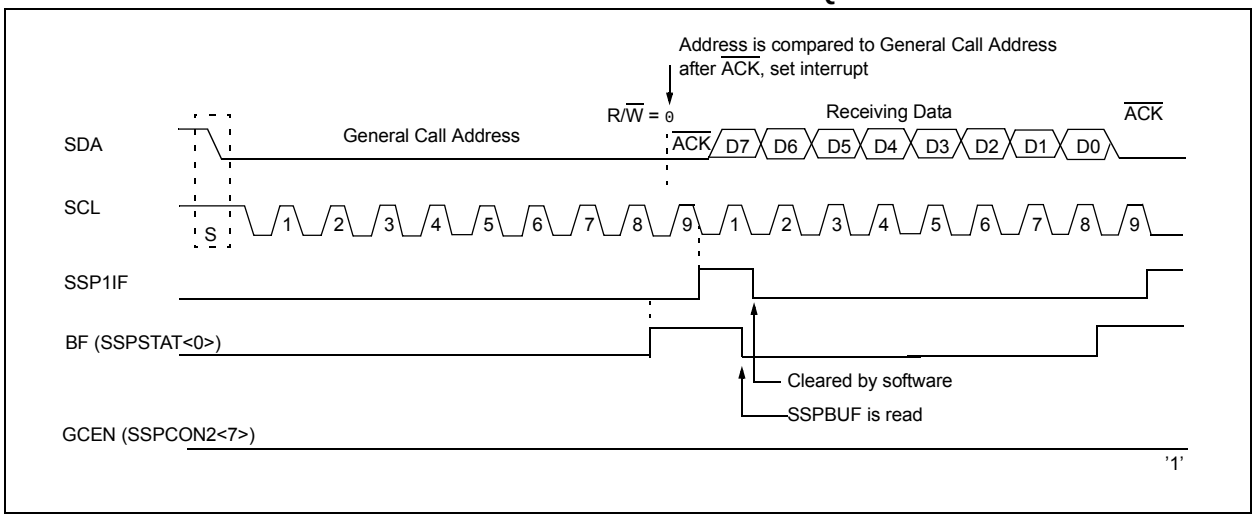
The addressing procedure for the $I^2C$ bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the $I^2C$ protocol, defined as address 0x00. When the GCEN bit of the SSPCON2 register is set, the slave module will automatically $\overline{ACK}$ the reception of this address regardless of the value stored in SSPADD. After the slave clocks in an address of all zeros with the R/$\overline{W}$ bit clear, an interrupt is generated and slave software can read SSPBUF and respond. Figure 26-23 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

**FIGURE 26-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE**




### 26.5.9 SSP MASK REGISTER

An SSP Mask (SSPMSK) register (Register 26-5) is available in $I^2C$ Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero ('0') bit in the SSPMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

**TABLE 26-3: SUMMARY OF REGISTERS ASSOCIATED WITH I²C™ OPERATION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset Values on Page: |
|---|---|---|---|---|---|---|---|---|---|
| APFCON1 | C2OUTSEL | CCP1SEL | SDOSEL | SCKSEL | SDISEL | TXSEL | RXSEL | CCP2SEL | 127 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 93 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 94 |
| PIE2 | OSFIE | C2IE | C1IE | EEIE | BCL1IE | C4IE | C3IE | CCP2IE | 95 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 98 |
| PIR2 | OSFIF | C2IF | C1IF | EEIF | BCL1IF | C4IF | C3IF | CCP2IF | 99 |
| SSP1ADD | ADD<7:0> | | | | | | | | 334 |
| SSP1BUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | 285* |
| SSP1CON1 | WCOL | SSPOV | SSPEN | CKP | SSPM<3:0> | | | | 331 |
| SSP1CON2 | GCEN | ACKSTAT | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 332 |
| SSP1CON3 | ACKTIM | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN | 331 |
| SSP1MSK | MSK<7:0> | | | | | | | | 334 |
| SSP1STAT | SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF | 329 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISA0 | 142 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in I²C™ mode.

* Page provides register information.

**Note 1:** PIC16(L)F1784/7 only.

## 30.4 Thermal Considerations

| Standard Operating Conditions (unless otherwise stated) | | | | | |
|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Typ.** | **Units** | **Conditions** |
| TH01 | $\theta_{JA}$ | Thermal Resistance Junction to Ambient | 60 | °C/W | 28-pin SPDIP package |
| | | | 80 | °C/W | 28-pin SOIC package |
| | | | 90 | °C/W | 28-pin SSOP package |
| | | | 27.5 | °C/W | 28-pin QFN 6x6mm package |
| | | | 47.2 | °C/W | 40-pin DIP package |
| | | | 41 | °C/W | 40-pin UQFN 5x5 |
| | | | 46 | °C/W | 44-pin TQFP package |
| | | | 24.4 | °C/W | 44-pin QFN 8x8mm package |
| TH02 | $\theta_{JC}$ | Thermal Resistance Junction to Case | 31.4 | °C/W | 28-pin SPDIP package |
| | | | 24 | °C/W | 28-pin SOIC package |
| | | | 24 | °C/W | 28-pin SSOP package |
| | | | 24 | °C/W | 28-pin QFN 6x6mm package |
| | | | 24.7 | °C/W | 40-pin DIP package |
| | | | 5.5 | °C/W | 40-pin UQFN 5x5 |
| | | | 14.5 | °C/W | 44-pin TQFP package |
| | | | 20 | °C/W | 44-pin QFN 8x8mm package |
| TH03 | $T_{JMAX}$ | Maximum Junction Temperature | 150 | °C | |
| TH04 | PD | Power Dissipation | — | W | $PD = P_{INTERNAL} + P_{I/O}$ |
| TH05 | $P_{INTERNAL}$ | Internal Power Dissipation | — | W | $P_{INTERNAL} = I_{DD} \times V_{DD}$ (1) |
| TH06 | $P_{I/O}$ | I/O Power Dissipation | — | W | $P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$ |
| TH07 | $P_{DER}$ | Derated Power | — | W | $P_{DER} = P_{DMAX} (T_J - T_A)/\theta_{JA}$ (2) |

**Note 1:** $I_{DD}$ is current to run the chip alone without driving any load on the output pins.
**2:** $T_A$ = Ambient Temperature
**3:** $T_J$ = Junction Temperature

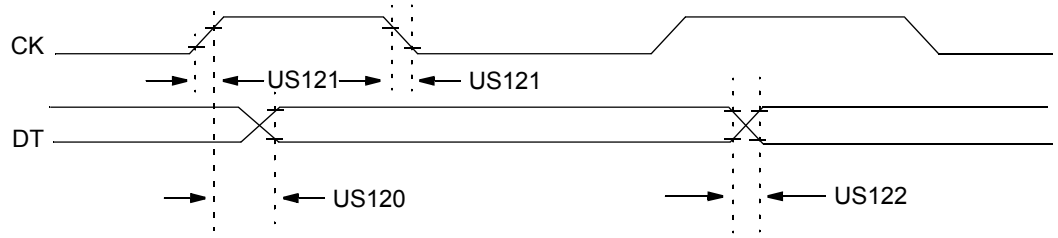
**TABLE 30-17: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS**

| **Operating Conditions:** $V_{DD}$ = 3V, Temperature = 25°C (unless otherwise stated). | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| DAC01* | $C_{LSB}$ | Step Size | — | $V_{DD}/256$ | — | V | |
| DAC02* | $C_{ACC}$ | Absolute Accuracy | — | — | ± 1.5 | LSb | |
| DAC03* | $C_R$ | Unit Resistor Value (R) | — | 600 | — | Ω | |
| DAC04* | $C_{ST}$ | Settling Time(1) | — | — | 10 | μs | |

* These parameters are characterized but not tested.

**Note 1:** Settling time measured while DACR<7:0> transitions from '0x00' to '0xFF'.

**FIGURE 30-14: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**

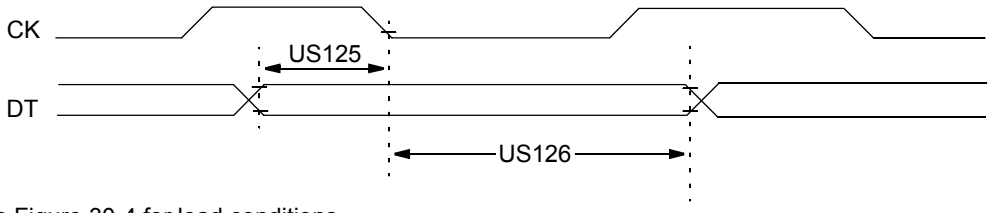



**Note:** Refer to Figure 30-4 for load conditions.

**TABLE 30-18: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS**

| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | | **Min.** | **Max.** | **Units** | **Conditions** |
| US120 | $T_{CKH2DTV}$ | SYNC XMIT (Master and Slave) Clock high to data-out valid | 3.0-5.5V | — | 80 | ns | |
| | | | 1.8-5.5V | — | 100 | ns | |
| US121 | $T_{CKRF}$ | Clock out rise time and fall time (Master mode) | 3.0-5.5V | — | 45 | ns | |
| | | | 1.8-5.5V | — | 50 | ns | |
| US122 | $T_{DTRF}$ | Data-out rise time and fall time | 3.0-5.5V | — | 45 | ns | |
| | | | 1.8-5.5V | — | 50 | ns | |

**FIGURE 30-15: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**



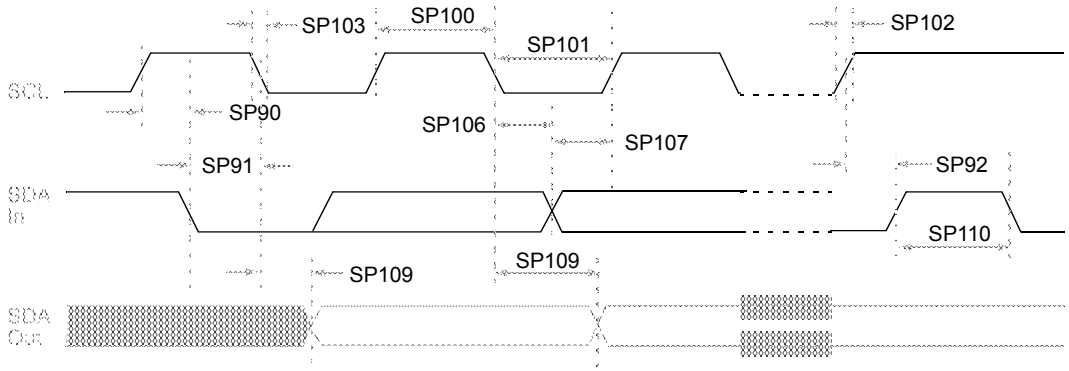

**Note:** Refer to Figure 30-4 for load conditions.

**TABLE 30-21: I²C™ BUS START/STOP BITS REQUIREMENTS**

| Standard Operating Conditions (unless otherwise stated) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| SP90* | TSU:STA | Start condition Setup time | 100 kHz mode | 4700 | — | — | ns | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 600 | — | — | | |
| SP91* | THD:STA | Start condition Hold time | 100 kHz mode | 4000 | — | — | ns | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | — | | |
| SP92* | TSU:STO | Stop condition Setup time | 100 kHz mode | 4700 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |
| SP93 | THD:STO | Stop condition Hold time | 100 kHz mode | 4000 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |

* These parameters are characterized but not tested.

**FIGURE 30-21: I²C™ BUS DATA TIMING**




**Note:** Refer to Figure 30-4 for load conditions.

**Note:** Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

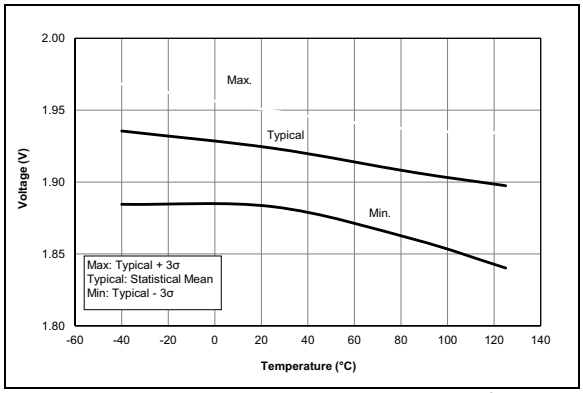



***FIGURE 31-61:*** *Brown-Out Reset Voltage, Low Trip Point (BORV = 1), PIC16LF1784/6/7 Only.*

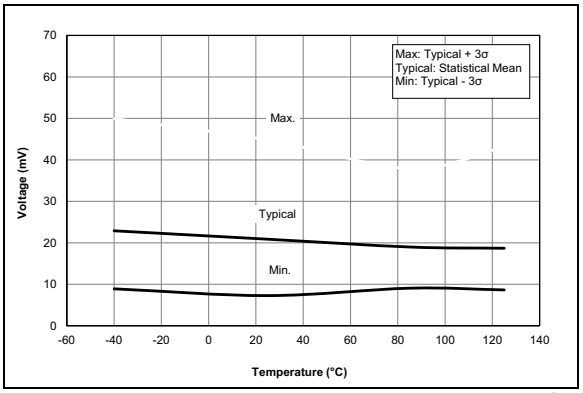



***FIGURE 31-62:*** *Brown-Out Reset Hysteresis, Low Trip Point (BORV = 1), PIC16LF1784/6/7 Only.*

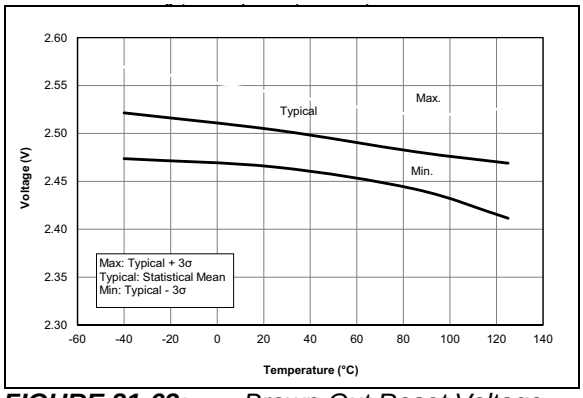



***FIGURE 31-63:*** *Brown-Out Reset Voltage, Low Trip Point (BORV = 1), PIC16F1784/6/7 Only.*

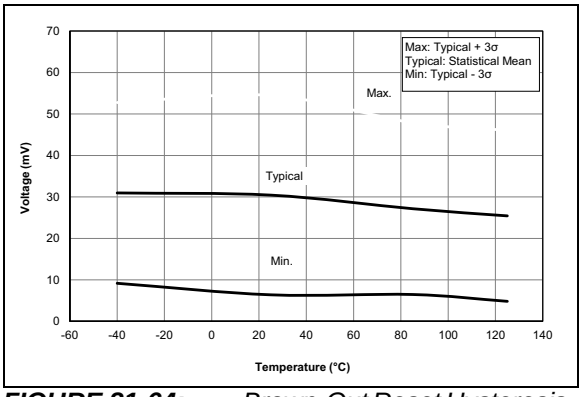



***FIGURE 31-64:*** *Brown-Out Reset Hysteresis, Low Trip Point (BORV = 1), PIC16F1784/6/7 Only.*

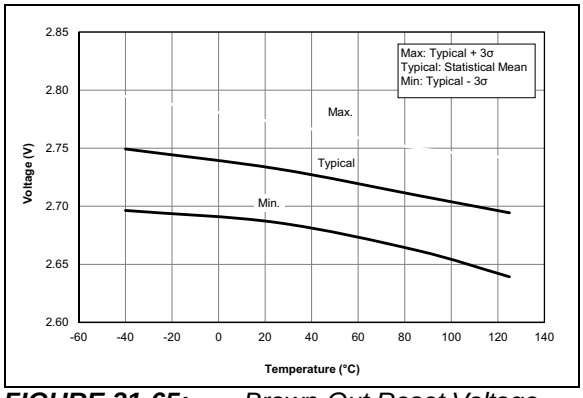



***FIGURE 31-65:*** *Brown-Out Reset Voltage, High Trip Point (BORV = 0).*

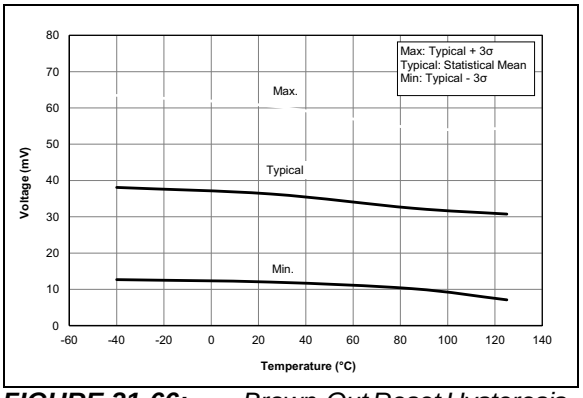
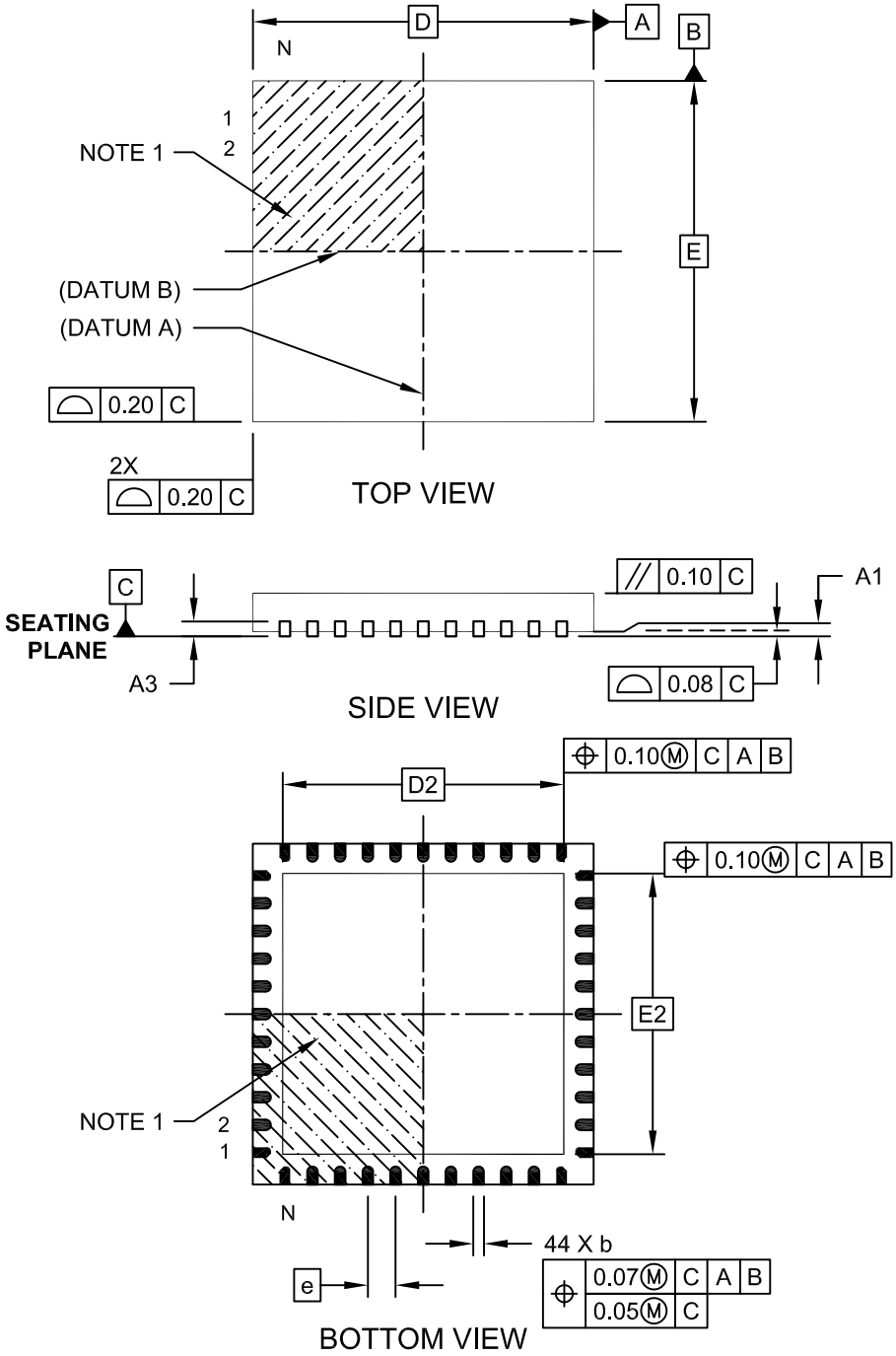



***FIGURE 31-66:*** *Brown-Out Reset Hysteresis, High Trip Point (BORV = 0).*

### 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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