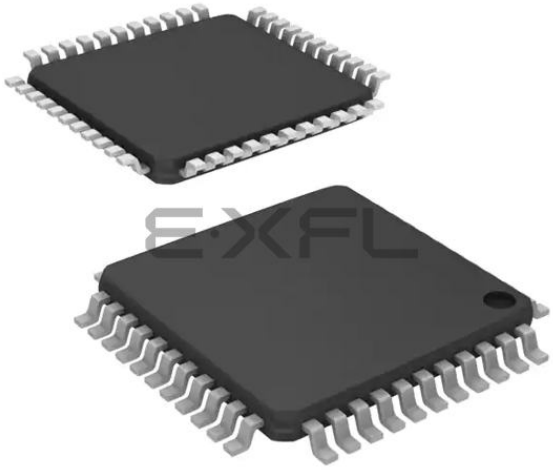

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1787-i-pt

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/C2OUT(1)/OSC2/ CLKOUT/VCAP	RA6	TTL/ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator.
RA7/PSMC1CLK/PSMC2CLK/ PSMC3CLK/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	PSMC1CLK	ST	—	PSMC1 clock input.
	PSMC2CLK	ST	—	PSMC2 clock input.
	PSMC3CLK	ST	—	PSMC3 clock input.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	st	—	External clock input (EC mode).
RB0/AN12/C2IN1+/PSMC1IN/ PSMC2IN/PSMC3IN/CCP1(1)/ INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	PSMC1IN	ST	—	PSMC1 Event Trigger input.
	PSMC2IN	ST	—	PSMC2 Event Trigger input.
	PSMC3IN	ST	—	PSMC3 Event Trigger input.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	INT	ST	—	External interrupt.
RB1/AN10/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	C3IN3-	AN	—	Comparator C3 negative input.
	C4IN3-	AN	—	Comparator C4 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-/CLKR	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CLKR	—	CMOS	Clock output.
RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN+/CCP2(1)	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	C3IN2-	AN	—	Comparator C3 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RB4/AN11/C3IN1+	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	C3IN1+	AN	—	Comparator C3 positive input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB5/AN13/C4IN2-/T1G/CCP3(1) SDO(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	C4IN2-	AN	—	Comparator C4 negative input.
	T1G	ST	—	Timer1 gate input.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SDO	—	CMOS	SPI data output.
RB6/C4IN1+/TX(1)/CK(1)/SDI(1)/ SDA(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	C4IN1+	AN	—	Comparator C4 positive input.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/RX(1)/DT(1)/ SCK(1)/SCL(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Voltage Reference output.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1OSO/T1CKI/PSMC1A	RC0	TTL/ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 Oscillator Connection.
	T1CKI	ST	—	Timer1 clock input.
	PSMC1A	—	CMOS	PSMC1 output A.
RC1/T1OSI/PSMC1B/CCP2	RC1	TTL/ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 Oscillator Connection.
	PSMC1B	—	CMOS	PSMC1 output B.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/PSMC1C/CCP1	RC2	TTL/ST	CMOS	General purpose I/O.
	PSMC1C	—	CMOS	PSMC1 output C.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/PSMC1D/SCK(1)/SCL(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	PSMC1D	—	CMOS	PSMC1 output D.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
RC4/PSMC1E/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	PSMC1E	—	CMOS	PSMC1 output E.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

5.1 Power-On Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

5.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms time-out on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTE bit in Configuration Words.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

5.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 5-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Words.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 5-2 for more information.

TABLE 5-1: BOR OPERATING MODES

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Instruction Execution upon: Release of POR or Wake-up from Sleep
11	X	X	Active	Waits for BOR ready(1) (BORRDY = 1)
10	X	Awake	Active	Waits for BOR ready (BORRDY = 1)
		Sleep	Disabled	
01	1	X	Active	Waits for BOR ready(1) (BORRDY = 1)
	0	X	Disabled	Begins immediately (BORRDY = x)
00	X	X	Disabled	

Note 1: In these specific cases, "Release of POR" and "Wake-up from Sleep", there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

5.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

5.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Words are programmed to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

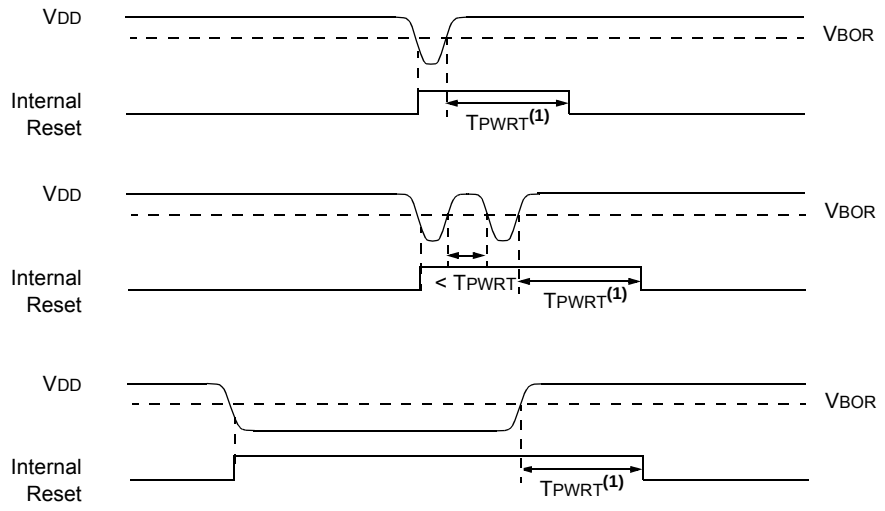
5.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

FIGURE 5-2: BROWN-OUT SITUATIONS



Note 1: TPWRT delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

5.3 Register Definitions: BOR Control

REGISTER 5-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	R/W-0/u	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	BORFS	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-out Reset Enable bit
If BOREN <1:0> in Configuration Words ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN <1:0> in Configuration Words = 01:
1 = BOR Enabled
0 = BOR Disabled

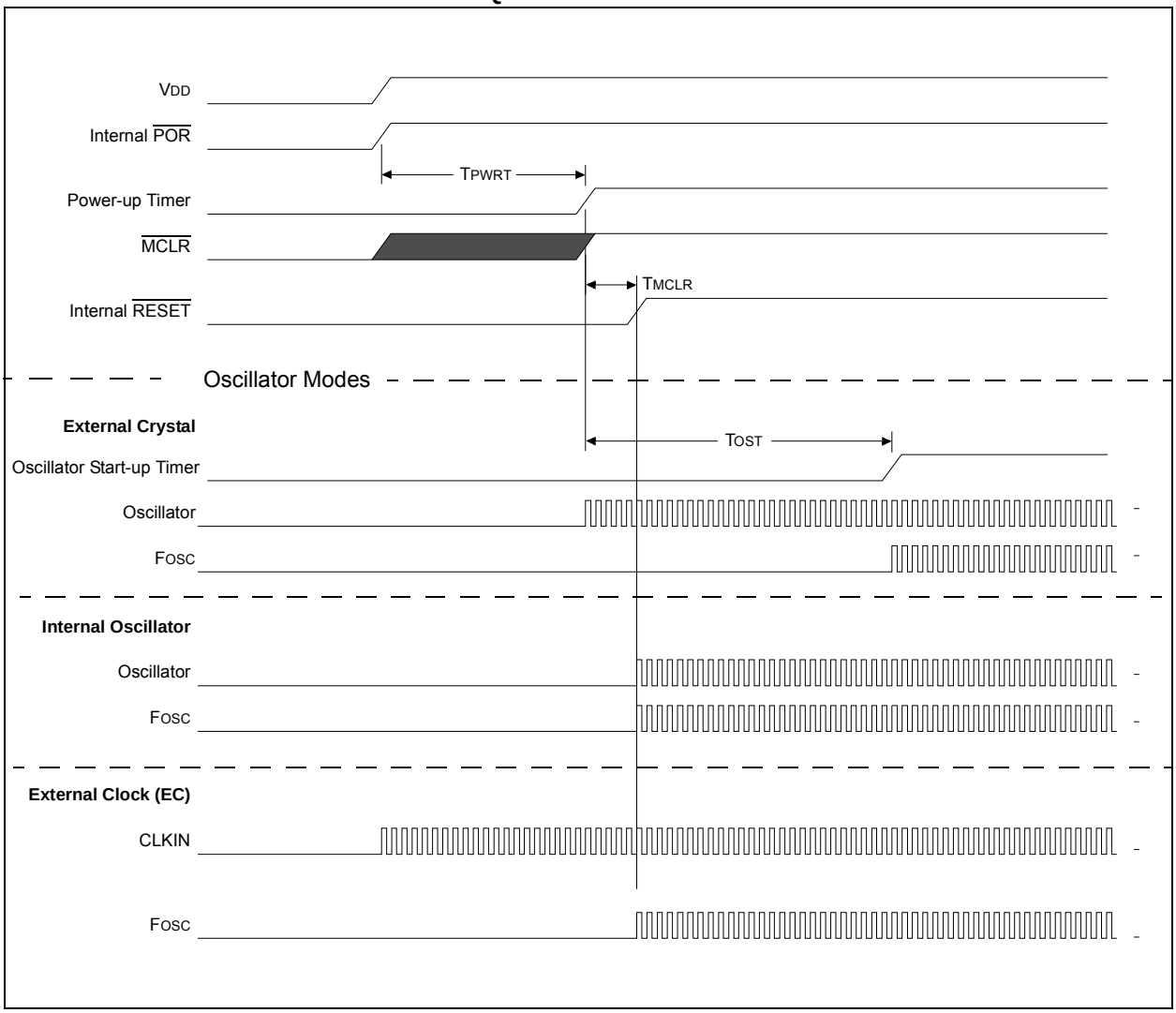
bit 6 **BORFS:** Brown-out Reset Fast Start bit(1)
If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)
BORFS is Read/Write, but has no effect.
If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):
1 = Band gap is forced on always (covers sleep/wake-up/operating cases)
0 = Band gap operates normally, and may turn off

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

Note 1: BOREN<1:0> bits are located in Configuration Words.

FIGURE 5-3: RESET START-UP SEQUENCE



12.3 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum block size that can be erased by user software.

Flash program memory may only be written or erased if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of Configuration Words.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the EEDATH:EEDATL register pair.

Note:	If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase.

The number of data write latches may not be equivalent to the number of row locations. During programming, user software may need to fill the set of write latches and initiate a programming operation multiple times in order to fully reprogram an erased row. For example, a device with a row size of 32 words and eight write latches will need to load the write latches with data and initiate a programming operation four times.

The size of a program memory row and the number of program memory write latches may vary by device. See Table 12-1 for details.

12.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:

1. Write the Least and Most Significant address bits to the EEADRH:EEADRL register pair.
2. Clear the CFGS bit of the EECON1 register.
3. Set the EEPGD control bit of the EECON1 register.
4. Then, set control bit RD of the EECON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "`BSF EECON1,RD`" instruction to be ignored. The data is available in the very next cycle, in the EEDATH:EEDATL register pair; therefore, it can be read as two bytes in the following instructions.

EEDATH:EEDATL register pair will hold this value until another read or until it is written to by the user.

Note 1:	The two instructions following a program memory read are required to be `NOP`s. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.
2:	Flash program memory can be read regardless of the setting of the $\overline{CP}$ bit.

TABLE 12-1: FLASH MEMORY ORGANIZATION BY DEVICE

Device	Erase Block (Row) Size/Boundary	Number of Write Latches/Boundary
PIC16(L)F1784/6/7	32 words, EEADRL<4:0> = `00000`	32 words, EEADRL<4:0> = `00000`

13.5.7 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-5.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

TABLE 13-5: PORTB OUTPUT PRIORITY

Pin Name	Function Priority(1)
RB0	CCP1 RB0
RB1	OPA2OUT RB1
RB2	CLKR RB2
RB3	CCP2 RB3
RB4	RB4
RB5	SDO C3OUT CCP3 RB5
RB6	ICSPCLK SDA TX/CK RB6
RB7	ICSPDAT DAC1OUT2 SCL/SCK DT RB7

Note 1: Priority listed from highest to lowest.

TABLE 17-1: ADC CLOCK PERIOD (T_{AD}) VS. DEVICE OPERATING FREQUENCIES

ADC Clock Period (T_{AD})		Device Frequency (F_{OSC})					
ADC Clock Source	ADCS<2:0>	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
F_{OSC}/2	000	62.5ns(2)	100 ns(2)	125 ns(2)	250 ns(2)	500 ns(2)	2.0 μs
F_{OSC}/4	100	125 ns(2)	200 ns(2)	250 ns(2)	500 ns(2)	1.0 μs	4.0 μs
F_{OSC}/8	001	0.5 μs(2)	400 ns(2)	0.5 μs(2)	1.0 μs	2.0 μs	8.0 μs(3)
F_{OSC}/16	101	800 ns	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs(3)
F_{OSC}/32	010	1.0 μs	1.6 μs	2.0 μs	4.0 μs	8.0 μs(3)	32.0 μs(3)
F_{OSC}/64	110	2.0 μs	3.2 μs	4.0 μs	8.0 μs(3)	16.0 μs(3)	64.0 μs(3)
F_{RC}	x11	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)

Legend: Shaded cells are outside of recommended range.

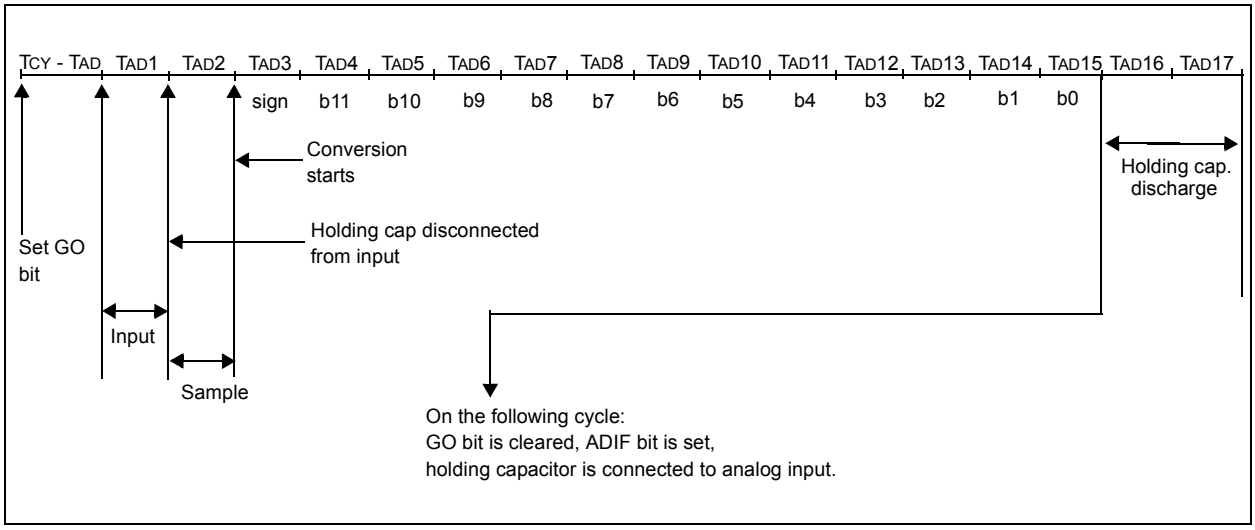
Note 1: The F_{RC} source has a typical T_{AD} time of 1.6 μs for V_{DD}.

2: These values violate the minimum required T_{AD} time.

3: For faster conversion times, the selection of another clock source is recommended.

4: The ADC clock period (T_{AD}) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock F_{OSC}. However, the F_{RC} oscillator source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 17-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES



20.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and fixed voltage reference

20.1 Comparator Overview

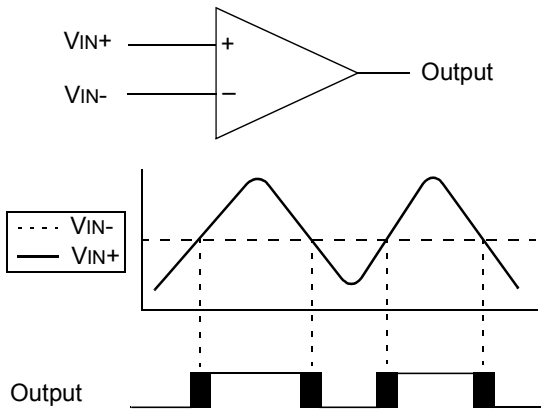
A single comparator is shown in Figure 20-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available for this device are located in Table 20-1.

TABLE 20-1: COMPARATOR AVAILABILITY PER DEVICE

Device	C1	C2	C3	C4
PIC16(L)F1784/6/7	●	●	●	●

FIGURE 20-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

REGISTER 20-3: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	R-0/0	R-0/0	R-0/0	R-0/0
—	—	—	—	MC4OUT(1)	MC3OUT	MC2OUT	MC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **MC4OUT:** Mirror Copy of C4OUT bit(1)

bit 2 **MC3OUT:** Mirror Copy of C3OUT bit

bit 1 **MC2OUT:** Mirror Copy of C2OUT bit

bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

Note 1: PIC16(L)F1784/7 only.

TABLE 20-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	132
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	138
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	193
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	193
CM1CON1	C1NTP	C1INTN	C1PCH<2:0>			C1NCH<2:0>			194
CM2CON1	C2NTP	C2INTN	C2PCH<2:0>			C2NCH<2:0>			194
CM3CON0	C3ON	C3OUT	C3OE	C3POL	C3ZLF	C3SP	C3HYS	C3SYNC	193
CM3CON1	C3INTP	C3INTN	C3PCH<2:0>			C3NCH<2:0>			194
CMOUT	—	—	—	—	MC4OUT(1)	MC3OUT	MC2OUT	MC1OUT	195
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		162
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	186
DAC1CON1	DAC1R<7:0>								186
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	95
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	99
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	132
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	138
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: PIC16(L)F1784/7 only.

REGISTER 24-31: PSMCxSTR0: PSMC STEERING CONTROL REGISTER 0

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1
—	—	PxSTRF(2)	PxSTRE(2)	PxSTRD(2)	PxSTRC(2)	PxSTRB	PxSTRA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **PxSTRF**: PWM Steering PSMCxF Output Enable bit(2)

If PxMODE<3:0> = 0000 (Single-phase PWM):
1 = Single PWM output is active on pin PSMCxF
0 = Single PWM output is not active on pin PSMCxF. PWM drive is in inactive state

If PxMODE<3:0> = 0001 (Complementary Single-phase PWM):
1 = Complementary PWM output is active on pin PSMCxF
0 = Complementary PWM output is not active on pin PSMCxOUT5. PWM drive is in inactive state

IF PxMODE<3:0> = 1100 (3-phase Steering):(1)
1 = PSMCxD and PSMCxE are high. PSMCxA, PMSCxB, PSMCxC and PMSCxF are low.
0 = 3-phase output combination is not active

bit 4 **PxSTRE**: PWM Steering PSMCxE Output Enable bit(2)

If PxMODE<3:0> = 000x (single-phase PWM or Complementary PWM):
1 = Single PWM output is active on pin PSMCxE
0 = Single PWM output is not active on pin PSMCxE. PWM drive is in inactive state

IF PxMODE<3:0> = 1100 (3-phase Steering):(1)
1 = PSMCxB and PSMCxE are high. PSMCxA, PMSCxC, PSMCxD and PMSCxF are low.
0 = 3-phase output combination is not active

bit 3 **PxSTRD**: PWM Steering PSMCxD Output Enable bit(2)

If PxMODE<3:0> = 0000 (Single-phase PWM):
1 = Single PWM output is active on pin PSMCxD
0 = Single PWM output is not active on pin PSMCxD. PWM drive is in inactive state

If PxMODE<3:0> = 0001 (Complementary single-phase PWM):
1 = Complementary PWM output is active on pin PSMCxD
0 = Complementary PWM output is not active on pin PSMCxD. PWM drive is in inactive state

IF PxMODE<3:0> = 1100 (3-phase Steering):(1)
1 = PSMCxB and PSMCxC are high. PSMCxA, PMSCxD, PSMCxE and PMSCxF are low.
0 = 3-phase output combination is not active

bit 2 **PxSTRC**: PWM Steering PSMCxC Output Enable bit(2)

If PxMODE<3:0> = 000x (Single-phase PWM or Complementary PWM):
1 = Single PWM output is active on pin PSMCxC
0 = Single PWM output is not active on pin PSMCxC. PWM drive is in inactive state

IF PxMODE<3:0> = 1100 (3-phase Steering):(1)
1 = PSMCxC and PSMCxF are high. PSMCxA, PMSCxB, PSMCxD and PMSCxE are low.
0 = 3-phase output combination is not active

25.2.6 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 "Alternate Pin Function"**for more information.

When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

26.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

26.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

26.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

26.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/$\overline{W}$ bit of SSPSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPBUF with data to transfer to the master. If the SEN bit of SSPCON2 is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPBUF was read before the 9th falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPBUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

26.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

26.5.6.3 Byte NACKing

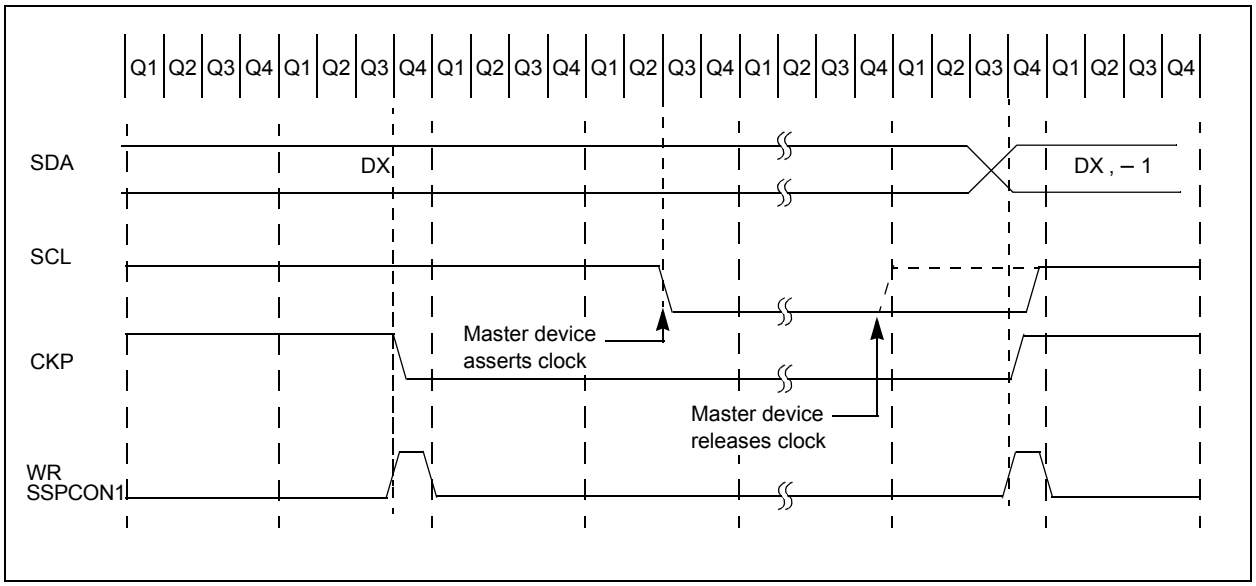
When AHEN bit of SSPCON3 is set; CKP is cleared by hardware after the 8th falling edge of SCL for a received matching address byte. When DHEN bit of SSPCON3 is set; CKP is cleared after the 8th falling edge of SCL for received data.

Stretching after the 8th falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

26.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 26-22).

FIGURE 26-23: CLOCK SYNCHRONIZATION TIMING



26.6.7 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

Note:	The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

26.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

26.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

26.6.7.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

26.6.7.4 Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/$\overline{W}$ bit set.
5. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
8. User sets the RCEN bit of the SSPCON2 register and the master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSP1IF and BF are set.
10. User clears the SSP1IF bit and reads the received byte from SSPUF, which clears the BF flag.
11. The user either clears the SSPCON2 register's ACKDT bit to receive another byte or sets the ADKDT bit to suppress further data and then initiates the acknowledge sequence by setting the ACKEN bit.
12. Master's ACK or $\overline{ACK}$ is clocked out to the slave and SSP1IF is set.
13. User clears SSP1IF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. If the ACKST bit was set in step 11 then the user can send a STOP to release the bus.

26.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 26-29).

26.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

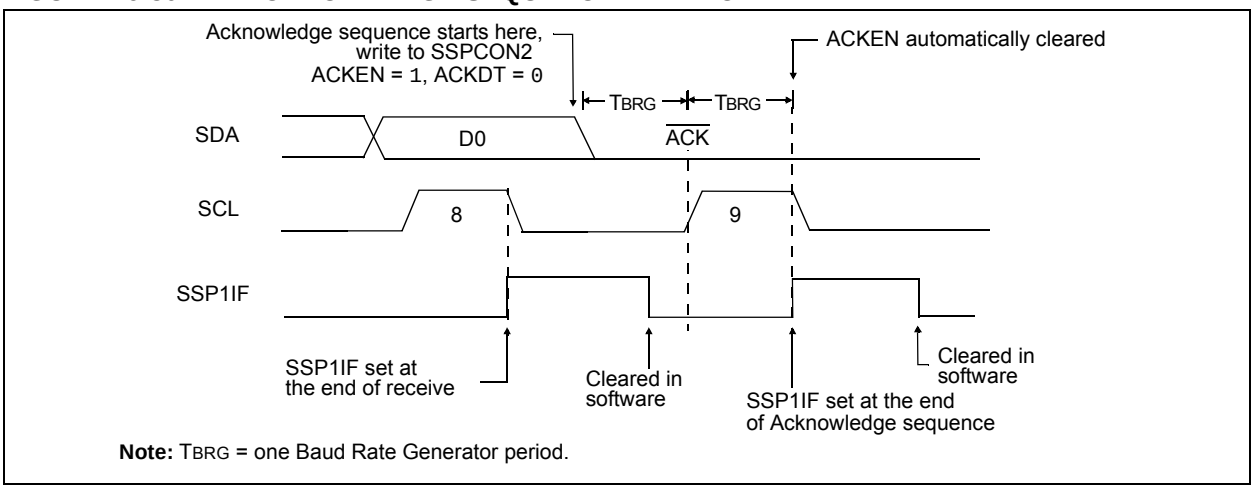
26.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 26-30).

26.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 26-30: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

27.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 6.2.2 "Internal Clock Sources"** for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 27.4.1 "Auto-Baud Detect"**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

RRF **Rotate Right f through Carry**

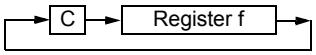
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SUBWFB **Subtract W from f with Borrow**

Syntax: SUBWFB f {,d}

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) – (W) – ($\overline{B}$) → dest

Status Affected: C, DC, Z

Description: Subtract W and the BORROW flag (CARRY) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

TABLE 30-2: SUPPLY VOLTAGE (I_{DD})(1,2)

PIC16LF1784/6/7			Standard Operating Conditions (unless otherwise stated)				
PIC16F1784/6/7							
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						V_{DD}	Note
D009	LDO Regulator	—	75	—	µA	—	High Power mode, normal operation
		—	15	—	µA	—	Sleep VREGCON<1> = 0
		—	0.3	—	µA	—	Sleep VREGCON<1> = 1
D010		—	8	20	µA	1.8	F_{OSC} = 32 kHz LP Oscillator mode **(Note 4)**, -40°C ≤ T_A ≤ +85°C
		—	12	24	µA	3.0	
D010		—	18	63	µA	2.3	F_{OSC} = 32 kHz LP Oscillator mode **(Note 4, 5)**, -40°C ≤ T_A ≤ +85°C
		—	20	74	µA	3.0	
		—	22	79	µA	5.0	
D012		—	160	650	µA	1.8	F_{OSC} = 4 MHz XT Oscillator mode
		—	320	1000	µA	3.0	
D012		—	260	700	µA	2.3	F_{OSC} = 4 MHz XT Oscillator mode **(Note 5)**
		—	330	1100	µA	3.0	
		—	380	1300	µA	5.0	

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

4: FVR and BOR are disabled.

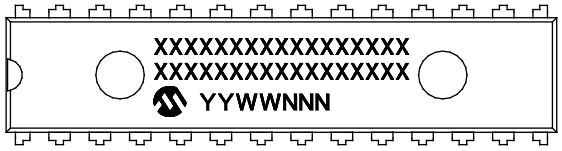
5: 0.1 µF capacitor on V_{CAP}.

6: 8 MHz crystal oscillator with 4x PLL enabled.

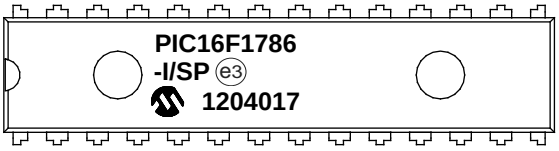
33.0 PACKAGING INFORMATION

33.1 Package Marking Information

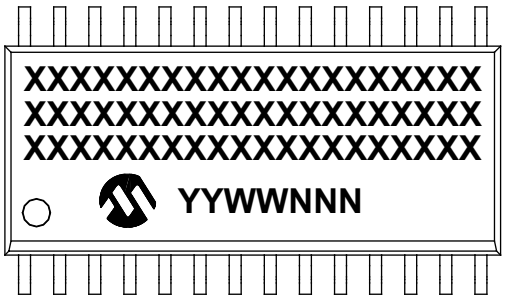
28-Lead SPDIP (.300")



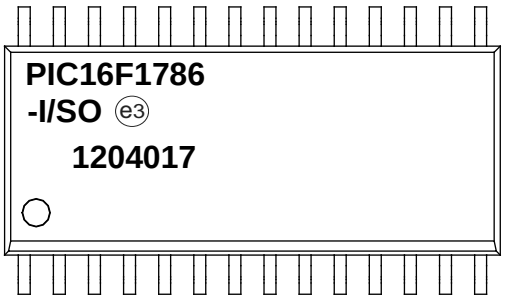
Example



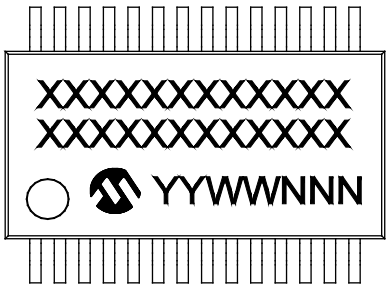
28-Lead SOIC (7.50 mm)



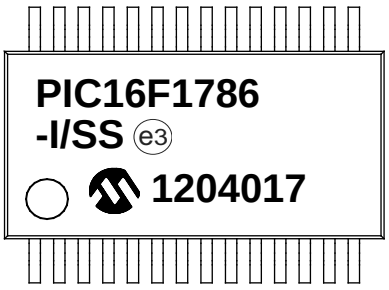
Example



28-Lead SSOP (5.30 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.