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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1787t-i-mv

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3.3.1 SPECIAL FUNCTION REGISTER

The Special Function Registers (SFR) are registers used by the application to control the desired operation of peripheral functions in the device. The SFR occupies the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of each peripheral are described in the corresponding peripheral chapters of this data sheet.

3.3.2 GENERAL PURPOSE RAM

There are up to 80 bytes of General Purpose Registers (GPR) in each data memory bank. The GPR occupies the space immediately after the SFR of selected data memory banks. The number of banks selected depends on the total amount of GPR space available in the device.

3.3.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2** "Linear Data Memory" for more information.

3.3.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



TABLE 3-5: PIC16(L)F1787 MEMORY MAP (BANKS 0-7)

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	_	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	PORTD	08Fh	TRISD	10Fh	LATD	18Fh	ANSELD	20Fh	WPUD	28Fh	ODCOND	30Fh	SLRCOND	38Fh	INLVLD
010h	PORTE	090h	TRISE	110h	LATE	190h	ANSELE	210h	WPUE	290h	ODCONE	310h	SLRCONE	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSP1BUF	291h	CCPR1L	311h	_	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSP1ADD	292h	CCPR1H	312h	_	392h	IOCAN
013h	_	093h	_	113h	CM2CON0	193h	EEDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	PIR4	094h	PIE4	114h	CM2CON1	194h	EEDATH	214h	SSP1STAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	EECON1	215h	SSP1CON1	295h	—	315h	_	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSP1CON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON ⁽¹⁾	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	_	218h	—	298h	CCPR2L	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RCREG	219h	—	299h	CCPR2H	319h	_	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	CM4CON0	19Ah	TXREG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	_
01Bh	PR2	09Bh	ADRESL	11Bh	CM4CON1	19Bh	SPBRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	_
01Ch	T2CON	09Ch	ADRESH	11Ch	APFCON2	19Ch	SPBRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON1	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	IOCEP
01Eh	—	09Eh	ADCON1	11Eh	CM3CON0	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	IOCEN
01Fh	_	09Fh	ADCON2	11Fh	CM3CON1	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	IOCEF
020h		0A0h		120h		1A0h		220h		2A0h		320h		3A0h	
	General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	13Fh 140h	General Purpose Register 80 Bytes		General Purpose Register 80 Bytes								
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h		0F0h		170h		1F0h		270h		2F0h		370h		3F0h	
	Common RAM 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16F1787 only.

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
	—			TUN	<5:0>		
bit 7	·						bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7-6	Unimplemer	nted: Read as '	0'				
bit 5-0	TUN<5:0>: F	Frequency Tunir	ng bits				
	100000 = M	linimum frequer	псу				
	•						
	•						
	111111 =						
	000000 = O	scillator module	e is running at	the factory-cali	brated frequen	cy.	
	000001 =						
	•						
	•						
	011110 =						
	011111 = M	laximum freque	ncy				

REGISTER 6-3: OSCTUNE: OSCILLATOR TUNING REGISTER

TABLE 6-2:	SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES
------------	--

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN		IRCF	<3:0>		—	SCS	82	
OSCSTAT	T10SCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	83
OSCTUNE	_	-			TUN	<5:0>			84
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	95
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	99
T1CON	TMR1C	S<1:0>	T1CKP	S<1:0>	T10SCEN	T1SYNC	_	TMR10N	207

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 6-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8	_	_	FCMEN	IESO	CLKOUTEN	BORE	N<1:0>	CPD	54
CONFIGI	7:0	CP	MCLRE	PWRTE	WDTE	E<1:0>		FOSC<2:0>		54

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

Note 1: PIC16F1784/6/7 only.

8.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

This chapter contains the following information for Interrupts:

- · Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- · Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 8-1.

FIGURE 8-1: INTERRUPT LOGIC



12.4 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

- 1. Load the starting address of the row to be modified.
- 2. Read the existing data from the row into a RAM image.
- 3. Modify the RAM image to contain the new data to be written into program memory.
- 4. Load the starting address of the row to be rewritten.
- 5. Erase the program memory row.
- 6. Load the write latches with data from the RAM image.
- 7. Initiate a programming operation.
- 8. Repeat steps 6 and 7 as many times as required to reprogram the erased row.

12.5 User ID, Device ID and Configuration Word Access

Instead of accessing program memory or EEPROM data memory, the User ID's, Device ID/Revision ID and Configuration Words can be accessed when CFGS = 1 in the EECON1 register. This is the region that would be pointed to by PC<15> = 1, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 12-2.

When read access is initiated on an address outside the parameters listed in Table 12-2, the EEDATH:EEDATL register pair is cleared.

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8006h	Device ID/Revision ID	Yes	No
8007h-8008h	Configuration Words 1 and 2	Yes	No

TABLE 12-2: USER ID, DEVICE ID AND CONFIGURATION WORD ACCESS (CFGS = 1)

EXAMPLE 12-6: CONFIGURATION WORD AND DEVICE ID ACCESS

* This code block will read 1 word of program memory at the memory address:

```
* PROG_ADDR_LO (must be 00h-08h) data will be returned in the variables;
```

* PROG_DATA_HI, PROG_DATA_LO

BANKSEL MOVLW MOVWF CLRF	EEADRL PROG_ADDR_LO EEADRL EEADRH	; ; ; ;	Select correct Bank Store LSB of address Clear MSB of address
BSF BCF BSF NOP BSF	EECON1,CFGS INTCON,GIE EECON1,RD INTCON,GIE	;;;;;;	Select Configuration Space Disable interrupts Initiate read Executed (See Figure 12-1) Ignored (See Figure 12-1) Restore interrupts
MOVF MOVWF MOVF MOVWF	EEDATL,W PROG_DATA_LO EEDATH,W PROG_DATA_HI	; ; ; ;	Get LSB of word Store in user location Get MSB of word Store in user location

REGISTER 17-6: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
	ADS	SIGN			AD<	11:8>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				

bit 3-0 AD<11:8>: ADC Result Register bits Most Significant 4 bits of 12-bit conversion result

REGISTER 17-7: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

| R/W-x/u |
|---------|---------|---------|---------|---------|---------|---------|---------|
| | | | AD< | 7:0> | | | |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 AD<7:0>: ADC Result Register bits Least Significant 8 bits of 12-bit conversion result

22.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 22-1 displays the Timer1 enable selections.

TABLE 22-1:	TIMER1 ENABLE
	SELECTIONS

TMR10N	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

22.2 Clock Source Selection

The TMR1CS<1:0> and T1OSCEN bits of the T1CON register are used to select the clock source for Timer1. Table 22-2 displays the clock source selections.

22.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of Fosc as determined by the Timer1 prescaler.

When the Fosc internal clock source is selected, the Timer1 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1 value. To utilize the full resolution of Timer1, an asynchronous input signal must be used to gate the Timer1 clock input.

The following asynchronous sources may be used:

- Asynchronous event on the T1G pin to Timer1 gate
- C1 or C2 comparator input to Timer1 gate

22.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI, which can be synchronized to the microcontroller system clock or can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated internal oscillator circuit.

- **Note:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:
 - · Timer1 enabled after POR
 - Write to TMR1H or TMR1L
 - Timer1 is disabled
 - Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON=1) when T1CKI is low.

ONS

TMR1CS<1:0>	T10SCEN	Clock Source
11	x	Reserved
10	1	Timer1 Oscillator
10	0	External Clocking on T1CKI Pin
01	x	System Clock (Fosc)
00	x	Instruction Clock (FOSC/4)

REGISTER 24-26: PSMCxDBR: PSMC RISING EDGE DEAD-BAND TIME REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
	PSMCxDBR<7:0>									
bit 7							bit 0			
Legend:										
R = Readable b	oit	W = Writable	bit	U = Unimplei	mented bit, rea	d as '0'				
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BC	R/Value at all c	other Resets			
'1' = Bit is set		'0' = Bit is clea	ared							

bit 7-0

—

PSMCxDBR<7:0>: Rising Edge Dead-Band Time bits

= Unsigned number of PSMCx psmc_clk clock periods in rising edge dead band

REGISTER 24-27: PSMCxDBF: PSMC FALLING EDGE DEAD-BAND TIME REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
PSMCxDBF<7:0>									
bit 7 bit									

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PSMCxDBF<7:0>:** Falling Edge Dead-Band Time bits

Unsigned number of PSMCx psmc_clk clock periods in falling edge dead band

REGISTER 24-28: PSMCxFFA: PSMC FRACTIONAL FREQUENCY ADJUST REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	PSMCxFFA<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 Unimplemented: Read as '0'

=

bit 3-0 **PSMCxFFA<3:0>:** Fractional Frequency Adjustment bits

 Unsigned number of fractional PSMCx psmc_clk clock periods to add to each period event time. The fractional time period = 1/(16*psmc_clk)

25.1 Capture Mode

The Capture mode function described in this section is available and identical for all CCP modules.

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCPx pin, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- · Every falling edge
- · Every rising edge
- · Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 25-1 shows a simplified diagram of the capture operation.

25.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Also, the CCP2 pin function can be moved to alternative pins using the APFCON register. Refer to **Section 13.1 "Alternate Pin Function"** for more details.

Note: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 25-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



25.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See Section 22.0 "Timer1 Module with Gate Control" for more information on configuring Timer1.

25.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIEx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

Note:	Clocking Timer1 from the system clock
	(Fosc) should not be used in Capture
	mode. In order for Capture mode to
	recognize the trigger event on the CCPx
	pin, Timer1 must be clocked from the
	instruction clock (Fosc/4) or from an
	external clock source.

25.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. Equation 25-1 demonstrates the code to perform this function.

EXAMPLE 25-1: CHANGING BETWEEN CAPTURE PRESCALERS

BANKSEL CCPxCON	;Set Bank bits to point
	;to CCPxCON
CLRF CCPxCON	;Turn CCP module off
MOVLW NEW_CAPT_P	S;Load the W reg with
	;the new prescaler
	;move value and CCP ON
MOVWF CCPxCON	;Load CCPxCON with this
	;value

26.5.2 SLAVE RECEPTION

When the R/\overline{W} bit of a matching received address byte is clear, the R/\overline{W} bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPSTAT register is set, or bit SSPOV of the SSPCON1 register is set. The BOEN bit of the SSPCON3 register modifies this operation. For more information see Register 26-4.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSP1IF, must be cleared by software.

When the SEN bit of the SSPCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPCON1 register, except sometimes in 10-bit mode. See **Section 26.2.3 "SPI Master Mode"** for more detail.

26.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I^2C Slave in 7-bit Addressing mode. All decisions made by hardware or software and their effect on reception. Figure 26-13 and Figure 26-14 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

- 1. Start bit detected.
- 2. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- 3. Matching address with R/\overline{W} bit clear is received.
- 4. The slave pulls SDA low sending an ACK to the master, and sets SSP1IF bit.
- 5. Software clears the SSP1IF bit.
- 6. Software reads received address from SSPBUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDA low sending an ACK to the master, and sets SSP1IF bit.
- 10. Software clears SSP1IF.
- 11. Software reads the received byte from SSPBUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the master.
- 13. Master sends Stop condition, setting P bit of SSPSTAT, and the bus goes idle.

26.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus[™] that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 26-15 displays a module using both address and data holding. Figure 26-16 includes the operation with the SEN bit of the SSPCON2 register set.

- 1. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit clear is clocked in. SSP1IF is set and CKP cleared after the 8th falling edge of SCL.
- 3. Slave clears the SSP1IF.
- Slave can look at the ACKTIM bit of the SSP-CON3 register to determine if the SSP1IF was after or before the ACK.
- 5. Slave reads the address value from SSPBUF, clearing the BF flag.
- 6. Slave sets ACK value clocked out to the master by setting ACKDT.
- 7. Slave releases the clock by setting CKP.
- 8. SSP1IF is set after an ACK, not after a NACK.
- 9. If SEN = 1 the slave hardware will stretch the clock after the ACK.

10. Slave clears SSP1IF.

Note: SSP1IF is still set after the 9th falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSP1IF not set

- 11. SSP1IF set and CKP cleared after 8th falling edge of SCL for a received data byte.
- 12. Slave looks at ACKTIM bit of SSPCON3 to determine the source of the interrupt.
- 13. Slave reads the received data from SSPBUF clearing BF.
- 14. Steps 7-14 are the same for each received data byte.
- 15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.





26.6.10 SLEEP OPERATION

While in Sleep mode, the I²C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

26.6.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

26.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit of the SSPSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCL1IF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

26.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCL1IF and reset the I²C port to its Idle state (Figure 26-31).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSP1IF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is Idle and the S and P bits are cleared.

26.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- SDA or SCL are sampled low at the beginning of the Start condition (Figure 26-32).
- b) SCL is sampled low before SDA is asserted low (Figure 26-33).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the Start condition is aborted,
- · the BCL1IF flag is set and
- · the MSSP module is reset to its Idle state (Figure 26-32).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 26-34). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.



FIGURE 26-33: **BUS COLLISION DURING START CONDITION (SDA ONLY)**

FIGURE 27-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 27-1, Register 27-2 and Register 27-3, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.





TABLE 27-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	127
BAUDCON	ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN	347
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	346
SPBRGL	BRG<7:0>								
SPBRGH	BRG<15:8>								348
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
TXREG	EUSART Tra	nsmit Data R	legister						337*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	345

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous transmission.

* Page provides register information.

- 27.1.2.8 Asynchronous Reception Set-up:
- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.4 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
- 10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

27.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.4 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Enable reception by setting the CREN bit.
- The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
- 10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.



FIGURE 27-5: ASYNCHRONOUS RECEPTION



FIGURE 27-10: SYNCHRONOUS TRANSMISSION

FIGURE 27-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



TABLE 27-7:SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER
TRANSMISSION

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	127
ABDOVF	RCIDL	_	SCKP	BRG16	—	WUE	ABDEN	347
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	346
BRG<7:0>								348
BRG<15:8>							348	
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
EUSART Transmit Data Register								337*
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	345
	Bit 7 C2OUTSEL ABDOVF GIE TMR1GIE SPEN SPEN TRISC7 CSRC	Bit 7Bit 6C2OUTSELCC1PSELABDOVFRCIDLGIEPEIETMR1GIEADIFTMR1GIFADIFSPENRX9TRISC7TRISC6TRSRC4TX9	Bit 7Bit 6Bit 5C2OUTSELCC1PSELSDOSELABDOVFRCIDLImmodelGIEPEIETMR0IETMR1GIEADIERCIETMR1GIFADIFRCIFSPENRX9SRENTRISC7TRISC6TRISC5CSRCTX9TXEN	Bit 7Bit 6Bit 5Bit 4C2OUTSELCC1PSELSDOSELSCKSELABDOVFRCIDLJONSELSCKPGIEPEIETMR0IEINTETMR1GIEADIERCIETXIETMR1GIFADIFRCIETXIESPENRX9SRENCRENSPENTRISC6TRISC6SRENTRISC7TRISC6TRISC5TRISC6CSRCTX9SXENSYNC	Bit 7Bit 6Bit 5Bit 4Bit 3C2OUTSEICC1PSEISDOSEISCKSEISDISEIABDOVFRCIDL-SCKPBRG16GIEPEIETMR0IEINTEIOCIETMR1GIEADIERCIETXIESSP11ETMR1GIFADIFRCIFTXIFSSP11FSPENRX9SRENCRENADDENSPENRX9SRENCRENADDENTRISC7TRISC6TRISC5TRISC4TRISC3CSRCTX9TXENSYNCSENDB	Bit 7Bit 6Bit 5Bit 4Bit 3Bit 2C2OUTSELCC1PSELSDOSELSCKSELSDISELTXSELABDOVFRCIDL-SCKPBRG16-GIEPEIETMR0IEINTEIOCIETMR0IFTMR1GIEADIERCIETXIESSP1IECCP1IETMR1GIFADIFRCIFTXIFSSP1IFCCP1IFSPENRX9SRENCRENADDENFERRSPENRX9SRENCRENADDENFERRTRISC7TRISC6TRISC5TRISC4TRISC3TRISC4CSRCTX9TXENSYNCSENDBBRGH	Bit 7Bit 6Bit 5Bit 4Bit 3Bit 2Bit 1C2OUTSELCC1PSELSDOSELSCKSELSDISELTXSELRXSELABDOVFRCIDL-SCKPBRG16-WUEGIEPEIETMROIEINTEIOCIETMROIFINTFTMR1GIEADIERCIETXIESSP1IECCP1IETMR2IETMR1GIFADIFRCIFTXIFSSP1IECCP1IFTMR2IESPENRX9SRENCRENADDENFERROERRBRGYSRENCRENADDENFERROERRTISC7TRISC6TRISC5TRISC4TRISC5TRISC4TRISC5TRISC4CSRC4TX9SYNCSENDBBRGHTRM1	Bit 7Bit 6Bit 5Bit 4Bit 3Bit 2Bit 1Bit 0C2OUTSELCC1PSELSDOSELSCKSELSDISELTXSELRXSELCCP2SELABDOVFRCIDL-SCKPBRG16-WUEABDENGIEPEIETMR0IEINTEIOCIETMR0IFINTEIOCIFTMR1GIEADIERCIETXIESSP1IECCP1IETMR2IETMR1IETMR1GIFADIFRCIFTXIFSSP1IFCCP1IFTMR2IETMR1IESPENRX9SRENCRENADDENFERROERRRX9DSPENRX9SRENCRENADDENFERROERRRX9DTRISC7TRISC6TRISC5TRISC4TRISC3TRISC4TRISC4TRISC4TRISC4CSRCTX9TXENSYNCSENDBBRGHTRMTTX9D

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master transmission.

* Page provides register information.

TABLE 30-7: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)									
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Тур†	Max.	Units	Conditions	
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽²⁾	±2% ±3%	_	16.0 16.0		MHz MHz	$0^{\circ}C \le TA \le +60^{\circ}C, VDD \ge 2.5V$ $60^{\circ}C \le TA \le 85^{\circ}C, VDD \ge 2.5V$	
			±5%	_	16.0	_	MHZ	$-40^{\circ}C \le IA \le +125^{\circ}C$	
OS08A	MFosc	Internal Calibrated MFINTOSC Frequency ⁽²⁾	±2% ±3%	_	500 500	_	kHz kHz	$\begin{array}{l} 0^{\circ}C \leq TA \leq +60^{\circ}C, \ VDD \geq 2.5V \\ 60^{\circ}C \leq TA \leq 85^{\circ}C, \ VDD \geq 2.5V \end{array}$	
			±5%	—	500	—	kHz	$-40^\circ C \leq T_A \leq +125^\circ C$	
OS09	LFosc	Internal LFINTOSC Frequency	—	_	31	_	kHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$	
OS10*	Tiosc st	HFINTOSC Wake-up from Sleep Start-up Time MFINTOSC Wake-up from Sleep Start-up Time		_	3.2 24	8 35	μs μs	VREGPM = 0 VREGPM = 0	

These parameters are characterized but not tested.

t Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μ F and 0.01 μ F values in parallel are recommended.

3: By design.

FIGURE 30-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



Temperature, VDD = 1.8V, PIC16LF1784/6/7 Only.



FIGURE 31-57: LFINTOSC Frequency, PIC16LF1784/6/7 Only.



Temperature, VDD = 1.8V, PIC16LF1784/6/7 Only.



FIGURE 31-58: LFINTOSC Frequency, PIC16F1784/6/7 Only.



FIGURE 31-59: WDT Time-Out Period, PIC16F1784/6/7 Only.



PIC16LF1784/6/7 Only.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension Limits		MIN	NOM	MAX		
Number of Pins	N	44				
Pitch	е	0.65 BSC				
Overall Height	A	0.80	0.90	1.00		
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3	0.20 REF				
Overall Width	E	8.00 BSC				
Exposed Pad Width	E2	6.25	6.45	6.60		
Overall Length	D	8.00 BSC				
Exposed Pad Length	D2	6.25	6.45	6.60		
Terminal Width	b	0.20	0.30	0.35		
Terminal Length	L	0.30	0.40	0.50		
Terminal-to-Exposed-Pad	K	0.20	_	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimensior	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	W2			6.60	
Optional Center Pad Length	T2			6.60	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.85	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B