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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	5
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908qt4cdw

Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History (Sheet 1 of 3)

Date	Revision Level	Description	Page Number(s)
September, 2002	N/A	Initial release	N/A
December, 2002	0.1	1.2 Features — Added 8-pin dual flat no lead (DFN) packages to features list.	19
		Figure 1-2. MCU Pin Assignments — Figure updated to include DFN packages.	21
		Figure 2-1. Memory Map — Clarified illegal address and unimplemented memory.	27
		Figure 2-2. Control, Status, and Data Registers — Corrected bit definitions for Port A Data Register (PTA) and Data Direction Register A (DDRA).	27
		Table 13-3. Interrupt Sources — Corrected vector addresses for keyboard interrupt and ADC conversion complete interrupt.	118
		Chapter 13 System Integration Module (SIM) — Removed reference to break status register as it is duplicated in break module.	113
		11.3.1 Internal Oscillator and 11.3.1.1 Internal Oscillator Trimming — Clarified oscillator trim option ordering information and what to expect with untrimmed device.	92
		Figure 11-5. Oscillator Trim Register (OSCTRIM) — Bit 1 designation corrected.	98
		Figure 15-13. Monitor Mode Circuit (Internal Clock, No High Voltage) — Diagram updated for clarity.	150
		Figure 12-1. I/O Port Register Summary — Corrected bit definitions for PTA7, DDRA7, and DDRA6.	99
		Figure 12-2. Port A Data Register (PTA) — Corrected bit definition for PTA7.	100
		Figure 12-3. Data Direction Register A (DDRA) — Corrected bit definitions for DDRA7 and DDRA6.	101
		Figure 12-6. Port B Data Register (PTB) — Corrected bit definition for PTB1	103
		Chapter 9 Keyboard Interrupt Module (KBI) — Section reworked after deletion of auto wakeup for clarity.	83
		Chapter 4 Auto Wakeup Module (AWU) — New section added for clarity.	49
		Figure 10-1. LVI Module Block Diagram — Corrected LVI stop representation.	87
		Chapter 16 Electrical Specifications — Extensive changes made to electrical specifications.	169
		17.5 8-Pin Dual Flat No Lead (DFN) Package (Case #1452) — Added case outline drawing for DFN package.	177
		Chapter 17 Ordering Information and Mechanical Specifications — Added ordering information for DFN package.	185
January, 2003	0.2	4.2 Features — Corrected third bulleted item.	49

Revision History (Sheet 3 of 3)

Date	Revision Level	Description	Page Number(s)
November, 2004	4.0	Reformatted to meet current documentation standards	Throughout
		6.3.1 BUSCLKX4 — Clarified description of BUSCLKX4	58
		Chapter 7 Central Processor Unit (CPU) — In 7.7 Instruction Set Summary : Reworked definitions for STOP instruction Added WAIT instruction	70 71
		13.8.1 SIM Reset Status Register — Clarified SRSR flag setting	117
		14.9.1 TIM Status and Control Register — Added information to TSTOP note	127
		16.8 5-V Oscillator Characteristics — Added values for deviation from trimmed internal oscillator	155
		16.12 3-V Oscillator Characteristics — Added values for deviation from trimmed internal oscillator	158
July, 2005	5.0	Figure 5-2. Configuration Register 1 (CONFIG1) — Clarified bit definitions for COPRS.	54
		Chapter 8 External Interrupt (IRQ) — Reworked for clarification.	73
		11.3.4 RC Oscillator — Improved RC oscillator wording.	93
		12.1 Introduction — Added note pertaining to non-bonded port pins.	97
		17.3 Package Dimensions — Updated package information.	165
March, 2010	6.0	Clarify internal oscillator trim register information.	26, 27, 31, 34, 35, 38, 91, 96

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Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
<div> <div>Lowest</div> <div>↑</div> <div>↓</div> <div>Highest</div> </div>	IF15	\$FFDE	ADC conversion complete vector (high)
		\$FFDF	ADC conversion complete vector (low)
	IF14	\$FFE0	Keyboard vector (high)
		\$FFE1	Keyboard vector (low)
	IF13 ↓ IF6	—	Not used
	IF5	\$FFF2	TIM overflow vector (high)
		\$FFF3	TIM overflow vector (low)
	IF4	\$FFF4	TIM Channel 1 vector (high)
		\$FFF5	TIM Channel 1 vector (low)
	IF3	\$FFF6	TIM Channel 0 vector (high)
		\$FFF7	TIM Channel 0 vector (low)
	IF2	—	Not used
	IF1	\$FFFA	$\overline{\text{IRQ}}$ vector (high)
		\$FFFB	$\overline{\text{IRQ}}$ vector (low)
	—	\$FFFC	SWI vector (high)
		\$FFFD	SWI vector (low)
	—	\$FFFE	Reset vector (high)
		\$FFFF	Reset vector (low)

2.5 Random-Access Memory (RAM)

Addresses \$0080–\$00FF are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

NOTE

For correct operation, the stack pointer must point only to RAM locations.

Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers.

NOTE

For M6805, M146805, and M68HC05 compatibility, the H register is not stacked.

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE

Be careful when using nested subroutines. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.



Analog-to-Digital Converter (ADC)

AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when ADR is read or ADSCR is written. Reset clears the AIEN bit.

- 1 = ADC interrupt enabled
- 0 = ADC interrupt disabled

ADCO — ADC Continuous Conversion Bit

When set, the ADC will convert samples continuously and update ADR at the end of each conversion. Only one conversion is allowed when this bit is cleared. Reset clears the ADCO bit.

- 1 = Continuous ADC conversion
- 0 = One ADC conversion

CH[4:0] — ADC Channel Select Bits

CH4, CH3, CH2, CH1, and CH0 form a 5-bit field which is used to select one of the four ADC channels. The five select bits are detailed in [Table 3-1](#). Care should be taken when using a port pin as both an analog and a digital input simultaneously to prevent switching noise from corrupting the analog signal. The ADC subsystem is turned off when the channel select bits are all set to 1. This feature allows for reduced power consumption for the MCU when the ADC is not used. Reset sets all of these bits to 1.

NOTE

Recovery from the disabled state requires one conversion cycle to stabilize.

Table 3-1. MUX Channel Select

CH4	CH3	CH2	CH1	CH0	ADC Channel	Input Select
0	0	0	0	0	ADC0	PTA0
0	0	0	0	1	ADC1	PTA1
0	0	0	1	0	ADC2	PTA4
0	0	0	1	1	ADC3	PTA5
0	0	1	0	0	—	Unused ⁽¹⁾
↓	↓	↓	↓	↓	—	
1	1	0	1	0	—	
1	1	0	1	1	—	Reserved
1	1	1	0	0	—	Unused
1	1	1	0	1	—	V _{DDA} ⁽²⁾
1	1	1	1	0	—	V _{SSA} ⁽²⁾
1	1	1	1	1	—	ADC power off

1. If any unused channels are selected, the resulting ADC conversion will be unknown.
2. The voltage levels supplied from internal reference nodes, as specified in the table, are used to verify the operation of the ADC converter both in production test and for user applications.

Z — Zero Flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of \$00.

1 = Zero result

0 = Non-zero result

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7

0 = No carry out of bit 7

7.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

7.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

7.5.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

7.5.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

7.6 CPU During Break Interrupts

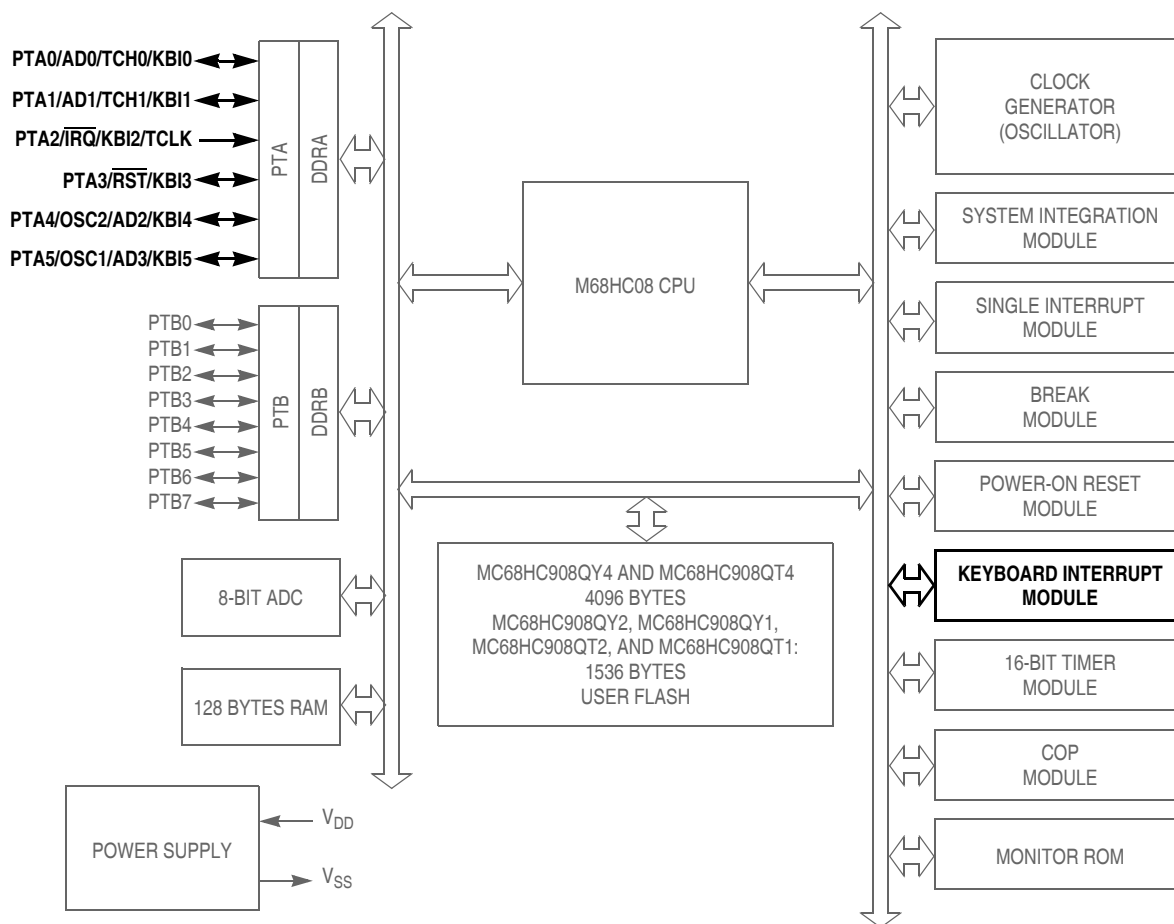
If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC:\$FFFD or with \$FEFC:\$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

Keyboard Interrupt Module (KBI)



\overline{RST} , \overline{IRQ} : Pins have internal (about 30K Ohms) pull up

PTA[0:5]: High current sink and source capability

PTA[0:5]: Pins have programmable keyboard interrupt and pull up

PTB[0:7]: Not available on 8-pin devices – MC68HC908QT1, MC68HC908QT2, and MC68HC908QT4 (see note in [12.1 Introduction](#))

ADC: Not available on the MC68HC908QY1 and MC68HC908QT1

Figure 9-1. Block Diagram Highlighting KBI Block and Pins

Low-Voltage Inhibit (LVI)

V_{TRIPF} . Setting the LVI enable in stop mode bit, LVISTOP, enables the LVI to operate in stop mode. Setting the LVI 5-V or 3-V trip point bit, LVI5OR3, enables the trip point voltage, V_{TRIPF} , to be configured for 5-V operation. Clearing the LVI5OR3 bit enables the trip point voltage, V_{TRIPF} , to be configured for 3-V operation. The actual trip thresholds are specified in [16.5 5-V DC Electrical Characteristics](#) and [16.9 3-V DC Electrical Characteristics](#).

NOTE

After a power-on reset, the LVI's default mode of operation is 3 volts. If a 5-V system is used, the user must set the LVI5OR3 bit to raise the trip point to 5-V operation.

If the user requires 5-V mode and sets the LVI5OR3 bit after power-on reset while the V_{DD} supply is not above the V_{TRIPR} for 5-V mode, the microcontroller unit (MCU) will immediately go into reset. The next time the LVI releases the reset, the supply will be above the V_{TRIPR} for 5-V mode.

Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR} , which causes the MCU to exit reset. See [Chapter 13 System Integration Module \(SIM\)](#) for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

10.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be cleared to enable the LVI module, and the LVIRSTD bit must be set to disable LVI resets.

10.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be cleared to enable the LVI module and to enable LVI resets.

10.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR} . This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF} . V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS} .

10.3.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

NOTE

The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point (V_{TRIPF} [5 V] or V_{TRIPF} [3 V]) may be lower than this. See [16.5 5-V DC Electrical Characteristics](#) and [16.9 3-V DC Electrical Characteristics](#) for the actual trip point voltages.

10.4 LVI Status Register

The LVI status register (LVISR) indicates if the V_{DD} voltage was detected below the V_{TRIPF} level while LVI resets have been disabled.

Address: \$FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	R
Write:								
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented
 R = Reserved

Figure 10-2. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage and is cleared when V_{DD} voltage rises above V_{TRIPR} . The difference in these threshold levels results in a hysteresis that prevents oscillation into and out of reset (see [Table 10-1](#)). Reset clears the LVIOUT bit.

Table 10-1. LVIOUT Bit Indication

V_{DD}	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

10.5 LVI Interrupts

The LVI module does not generate interrupt requests.

10.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

10.6.1 Wait Mode

If enabled, the LVI module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

10.6.2 Stop Mode

When the LVIPWRD bit in the configuration register is cleared and the LVISTOP bit in the configuration register is set, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

11.3.3 XTAL Oscillator

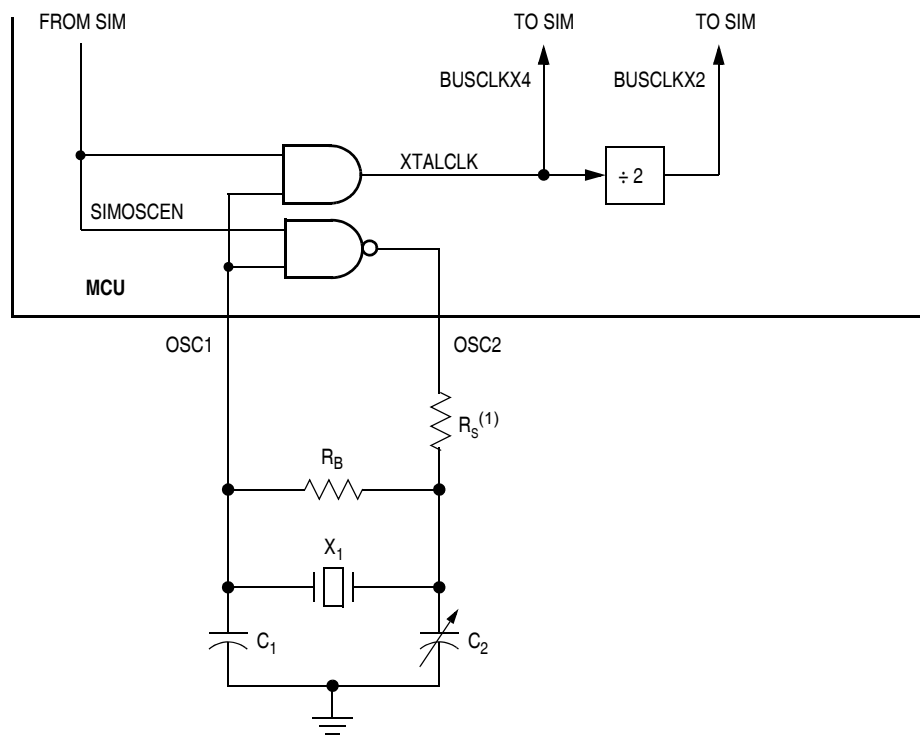
The XTAL oscillator circuit is designed for use with an external crystal or ceramic resonator to provide an accurate clock source. In this configuration, the OSC2 pin is dedicated to the external crystal circuit. The OSC2EN bit in the port A pullup enable register has no effect when this clock mode is selected.

In its typical configuration, the XTAL oscillator is connected in a Pierce oscillator configuration, as shown in [Figure 11-2](#). This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X_1
- Fixed capacitor, C_1
- Tuning capacitor, C_2 (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S (optional)

NOTE

The series resistor (R_S) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.



Note 1.

R_S can be zero (shorted) when used with higher-frequency crystals. Refer to manufacturer's data. See [Chapter 16 Electrical Specifications](#) for component value recommendations.

Figure 11-2. XTAL Oscillator External Connections

Chapter 12

Input/Output Ports (PORTS)

12.1 Introduction

The MC68HC908QT1, MC68HC908QT2, and MC68HC908QT4 have five bidirectional input-output (I/O) pins and one input only pin. The MC68HC908QY1, MC68HC908QY2, and MC68HC908QY4 have thirteen bidirectional pins and one input only pin. All I/O pins are programmable as inputs or outputs.

NOTE

Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS} . Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.

8-pin devices have non-bonded pins. These pins should be configured either as outputs driving low or high, or as inputs with internal pullups enabled. Configuring these non-bonded pins in this manner will prevent any excess current consumption caused by floating inputs.

12.2 Port A

Port A is a 6-bit special function port that shares all six of its pins with the keyboard interrupt (KBI) module (see [Chapter 9 Keyboard Interrupt Module \(KBI\)](#)). Each port A pin also has a software configurable pullup device if the corresponding port pin is configured as an input port.

NOTE

PTA2 is input only.

When the \overline{IRQ} function is enabled in the configuration register 2 (CONFIG2), bit 2 of the port A data register (PTA) will always read a 0. In this case, the BIH and BIL instructions can be used to read the logic level on the PTA2 pin. When the \overline{IRQ} function is disabled, these instructions will behave as if the PTA2 pin is a logic 1. However, reading bit 2 of PTA will read the actual logic level on the pin.

13.4.1 External Pin Reset

The $\overline{\text{RST}}$ pin circuits include an internal pullup device. Pulling the asynchronous $\overline{\text{RST}}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{\text{RST}}$ is held low for at least the minimum t_{RL} time. Figure 13-3 shows the relative timing. The $\overline{\text{RST}}$ pin function is only available if the RSTEN bit is set in the CONFIG2 register.

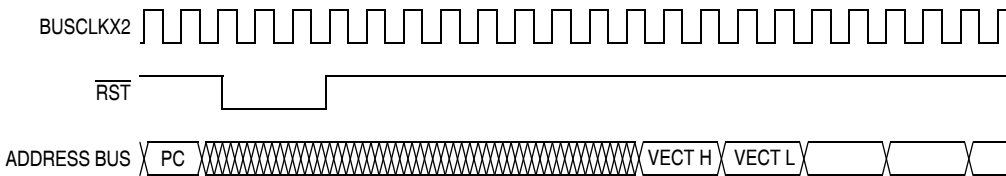


Figure 13-3. External Reset Timing

13.4.2 Active Resets from Internal Sources

The $\overline{\text{RST}}$ pin is initially setup as a general-purpose input after a POR. Setting the RSTEN bit in the CONFIG2 register enables the pin for the reset function. This section assumes the RSTEN bit is set when describing activity on the $\overline{\text{RST}}$ pin.

NOTE

For POR and LVI resets, the SIM cycles through 4096 BUSCLKX4 cycles during which the SIM forces the $\overline{\text{RST}}$ pin low. The internal reset signal then follows the sequence from the falling edge of $\overline{\text{RST}}$ shown in Figure 13-4.

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

All internal reset sources actively pull the $\overline{\text{RST}}$ pin low for 32 BUSCLKX4 cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (see Figure 13-4). An internal reset can be caused by an illegal address, illegal opcode, COP time out, LVI, or POR (see Figure 13-5).

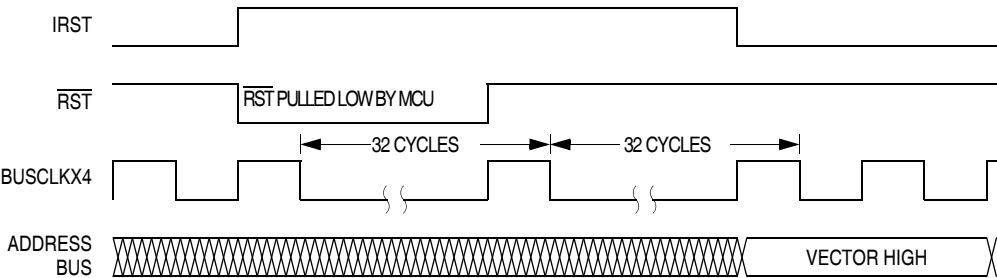


Figure 13-4. Internal Reset Timing

14.4.4.3 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use the following initialization procedure:

1. In the TIM status and control register (TSC):
 - a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
 - b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH:TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH:TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):
 - a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB:MSxA. See [Table 14-3](#).
 - b. Write 1 to the toggle-on-overflow bit, TOVx.
 - c. Write 1:0 (polarity 1 — to clear output on compare) or 1:1 (polarity 0 — to set output on compare) to the edge/level select bits, ELSxB:ELSxA. The output action on compare must force the output to the complement of the pulse width level. See [Table 14-3](#).

NOTE

In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare can also cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.

5. In the TIM status control register (TSC), clear the TIM stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H:TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSCR0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0% duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100% duty cycle output. See [14.9.4 TIM Channel Status and Control Registers](#).

14.5 Interrupts

The following TIM sources can generate interrupt requests:

- TIM overflow flag (TOF) — The TOF bit is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow CPU interrupt requests. TOF and TOIE are in the TIM status and control register.
- TIM channel flags (CH1F:CH0F) — The CHxF bit is set when an input capture or output compare occurs on channel x. Channel x TIM CPU interrupt requests are controlled by the channel x interrupt enable bit, CHxIE. Channel x TIM CPU interrupt requests are enabled when CHxIE = 1. CHxF and CHxIE are in the TIM channel x status and control register.

Timer Interface Module (TIM)

Address: \$0025	TSC0						
	Bit 7	6	5	4	3	2	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0
Write:	0						
Reset:	0	0	0	0	0	0	0

Address: \$0028	TSC1						
	Bit 7	6	5	4	3	2	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1
Write:	0						
Reset:	0	0	0	0	0	0	0

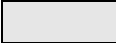
 = Unimplemented

Figure 14-7. TIM Channel Status and Control Registers (TSC0:TSC1)

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM counter registers matches the value in the TIM channel x registers.

Clear CHxF by reading the TIM channel x status and control register with CHxF set and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing a 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

- 1 = Input capture or output compare on channel x
- 0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM CPU interrupt service requests on channel x. Reset clears the CHxIE bit.

- 1 = Channel x CPU interrupt requests enabled
- 0 = Channel x CPU interrupt requests disabled

MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM channel 0 status and control register.

Setting MS0B disables the channel 1 status and control register and reverts TCH1 to general-purpose I/O.

Reset clears the MSxB bit.

- 1 = Buffered output compare/PWM operation enabled
- 0 = Buffered output compare/PWM operation disabled

MSxA — Mode Select Bit A

When ELSxB:A ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation. See [Table 14-3](#).

- 1 = Unbuffered output compare/PWM operation
- 0 = Input capture operation

Table 15-1. Monitor Mode Signal Requirements and Options

Mode	$\overline{\text{IRQ}}$ (PTA2)	$\overline{\text{RST}}$ (PTA3)	Reset Vector	Serial Communication	Mode Selection		COP	Communication Speed			Comments
				PTA0	PTA1	PTA4		External Clock	Bus Frequency	Baud Rate	
Normal Monitor	V_{TST}	V_{DD}	X	1	1	0	Disabled	9.8304 MHz	2.4576 MHz	9600	Provide external clock at OSC1.
Forced Monitor	V_{DD}	X	\$FFFF (blank)	1	X	X	Disabled	9.8304 MHz	2.4576 MHz	9600	Provide external clock at OSC1.
	V_{SS}	X	\$FFFF (blank)	1	X	X	Disabled	X	3.2 MHz (Trimmed)	9600	Internal clock is active.
User	X	X	Not \$FFFF	X	X	X	Enabled	X	X	X	
MON08 Function [Pin No.]	V_{TST} [6]	$\overline{\text{RST}}$ [4]	—	COM [8]	MOD0 [12]	MOD1 [10]	—	OSC1 [13]	—	—	

1. PTA0 must have a pullup resistor to V_{DD} in monitor mode.
2. Communication speed in the table is an example to obtain a baud rate of 9600. Baud rate using external oscillator is bus frequency / 256 and baud rate using internal oscillator is bus frequency / 335.
3. External clock is a 9.8304 MHz oscillator on OSC1.
4. X = don't care
5. MON08 pin refers to P&E Microcomputer Systems' MON08-Cyclone 2 by 8-pin connector.

NC	1	2	GND
NC	3	4	$\overline{\text{RST}}$
NC	5	6	$\overline{\text{IRQ}}$
NC	7	8	PTA0
NC	9	10	PTA4
NC	11	12	PTA1
OSC1	13	14	NC
V_{DD}	15	16	NC

The rising edge of the internal $\overline{\text{RST}}$ signal latches the monitor mode. Once monitor mode is latched, the values on PTA1 and PTA4 pins can be changed.

Once out of reset, the MCU waits for the host to send eight security bytes (see [15.3.2 Security](#)). After the security bytes, the MCU sends a break signal (10 consecutive logic 0s) to the host, indicating that it is ready to receive a command.

15.3.1.1 Normal Monitor Mode

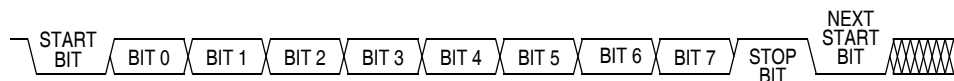
$\overline{\text{RST}}$ and OSC1 functions will be active on the PTA3 and PTA5 pins respectively as long as V_{TST} is applied to the $\overline{\text{IRQ}}$ pin. If the $\overline{\text{IRQ}}$ pin is lowered (no longer V_{TST}) then the chip will still be operating in monitor mode, but the pin functions will be determined by the settings in the configuration registers (see [Chapter 5 Configuration Register \(CONFIG\)](#)) when V_{TST} was lowered. With V_{TST} lowered, the BIH and BIL instructions will read the $\overline{\text{IRQ}}$ pin state only if IRQEN is set in the CONFIG2 register.

Table 15-2. Mode Difference

Modes	Functions					
	Reset Vector High	Reset Vector Low	Break Vector High	Break Vector Low	SWI Vector High	SWI Vector Low
User	\$FFFE	\$FFFF	\$FFFC	\$FFFD	\$FFFC	\$FFFD
Monitor	\$FEFE	\$FEFF	\$FEFC	\$FEFD	\$FEFC	\$FEFD

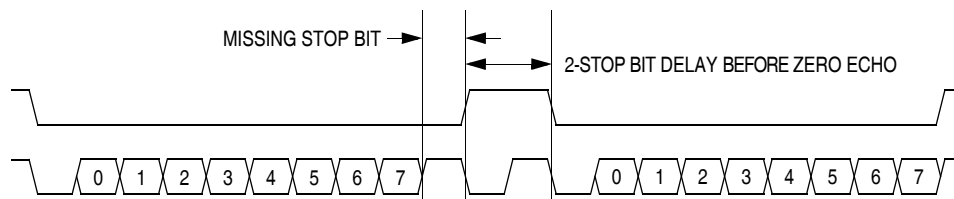
15.3.1.4 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. Transmit and receive baud rates must be identical.


Figure 15-13. Monitor Data Format

15.3.1.5 Break Signal

A start bit (logic 0) followed by nine logic 0 bits is a break signal. When the monitor receives a break signal, it drives the PTA0 pin high for the duration of two bits and then echoes back the break signal.


Figure 15-14. Break Transaction

15.3.1.6 Baud Rate

The monitor communication baud rate is controlled by the frequency of the external or internal oscillator and the state of the appropriate pins as shown in [Table 15-1](#).

[Table 15-1](#) also lists the bus frequencies to achieve standard baud rates. The effective baud rate is the bus frequency divided by 256 when using an external oscillator. When using the internal oscillator in forced monitor mode, the effective baud rate is the bus frequency divided by 335.

15.3.1.7 Commands

The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

16.9 3-V DC Electrical Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Output high voltage $I_{Load} = -0.6 \text{ mA}$, all I/O pins $I_{Load} = -4.0 \text{ mA}$, all I/O pins $I_{Load} = -10.0 \text{ mA}$, PTA0, PTA1, PTA3–PTA5 only	V_{OH}	$V_{DD} - 0.3$ $V_{DD} - 1.0$ $V_{DD} - 0.8$	— — —	— — —	V
Maximum combined I_{OH} (all I/O pins)	I_{OHT}	—	—	50	mA
Output low voltage $I_{Load} = 0.5 \text{ mA}$, all I/O pins $I_{Load} = 6.0 \text{ mA}$, all I/O pins $I_{Load} = 10.0 \text{ mA}$, PTA0, PTA1, PTA3–PTA5 only	V_{OL}	— — —	— — —	0.3 1.0 0.8	V
Maximum combined I_{OL} (all I/O pins)	I_{OLT}	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PTA0–PTA5, PTB0–PTB7	V_{IL}	V_{SS}	—	$0.3 \times V_{DD}$	V
Input hysteresis	V_{HYS}	$0.06 \times V_{DD}$	—	—	V
DC injection current, all ports	I_{INJ}	–2	—	+2	mA
Total dc current injection (sum of all I/O)	I_{INJTOT}	–25	—	+25	mA
Ports Hi-Z leakage current	I_{IL}	–1	± 0.1	+1	μA
Capacitance Ports (as input) Ports (as input)	C_{IN} C_{OUT}	— —	— —	12 8	pF
POR rearm voltage ⁽³⁾	V_{POR}	0	—	100	mV
POR rise time ramp rate ⁽⁴⁾	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	V_{TST}	$V_{DD} + 2.5$	—	$V_{DD} + 4.0$	V
Pullup resistors ⁽⁵⁾ PTA0–PTA5, PTB0–PTB7	R_{PU}	16	26	36	k Ω
Low-voltage inhibit reset, trip falling voltage	V_{TRIPF}	2.40	2.55	2.70	V
Low-voltage inhibit reset, trip rising voltage	V_{TRIPR}	2.50	2.65	2.80	V
Low-voltage inhibit reset/recover hysteresis	V_{HYS}	—	60	—	mV

1. $V_{DD} = 2.7$ to 3.3 Vdc , $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted.

2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.

3. Maximum is highest voltage that POR is guaranteed.

4. If minimum V_{DD} is not reached before the internal POR reset is released, the LVI will hold the part in reset until minimum V_{DD} is reached.

5. R_{PU} are measured at $V_{DD} = 3.0 \text{ V}$



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NOTES:

1. DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.

4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

5. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46mm.

TITLE:

8 LEAD MFP

CASE NUMBER: 968–02

STANDARD: EIAJ

PACKAGE CODE: 6003

SHEET: 3 OF 4