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#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc68hc908qy2mpe">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc68hc908qy2mpe</a>

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## Memory

8. Wait for time,  $t_{PROG}$  (minimum 30  $\mu$ s).
9. Repeat step 7 and 8 until all desired bytes within the row are programmed.
10. Clear the PGM bit<sup>(1)</sup>.
11. Wait for time,  $t_{NVH}$  (minimum 5  $\mu$ s).
12. Clear the HVEN bit.
13. After time,  $t_{RCV}$  (typical 1  $\mu$ s), the memory can be accessed in read mode again.

### NOTE

*The COP register at location \$FFFF should not be written between steps 5–12, when the HVEN bit is set. Since this register is located at a valid FLASH address, unpredictable behavior may occur if this location is written while HVEN is set.*

This program sequence is repeated throughout the memory until all data is programmed.

### NOTE

*Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps. Do not exceed  $t_{PROG}$  maximum, see [16.16 Memory Characteristics](#).*

## 2.6.5 FLASH Protection

Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made to protect blocks of memory from unintentional erase or program operations due to system malfunction. This protection is done by use of a FLASH block protect register (FLBPR). The FLBPR determines the range of the FLASH memory which is to be protected. The range of the protected area starts from a location defined by FLBPR and ends to the bottom of the FLASH memory (\$FFF). When the memory is protected, the HVEN bit cannot be set in either ERASE or PROGRAM operations.

### NOTE

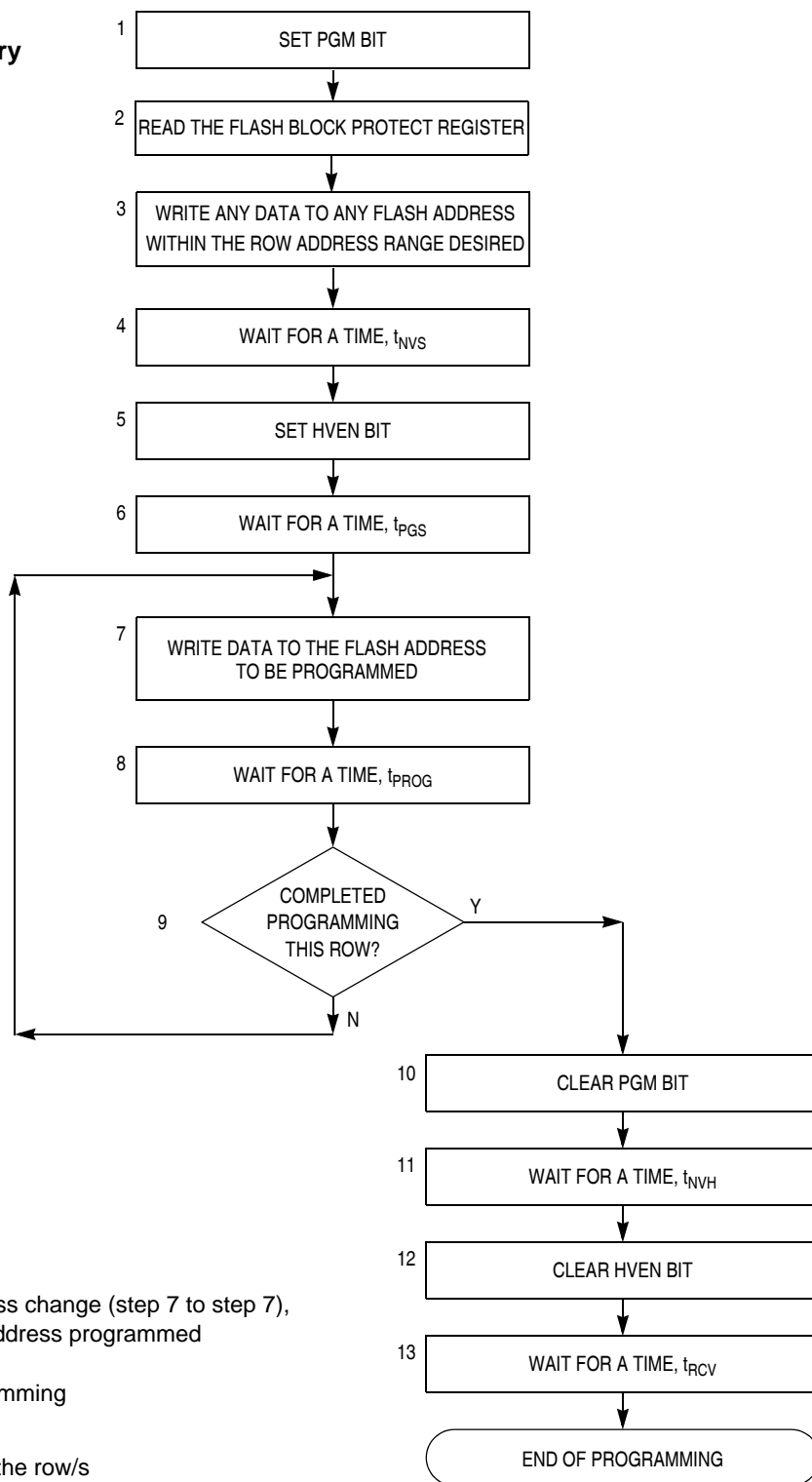
*In performing a program or erase operation, the FLASH block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.*

When the FLBPR is programmed with all 0's, the entire memory is protected from being programmed and erased. When all the bits are erased (all 1's), the entire memory is accessible for program and erase.

When bits within the FLBPR are programmed, they lock a block of memory. The address ranges are shown in [2.6.6 FLASH Block Protect Register](#). Once the FLBPR is programmed with a value other than \$FF, any erase or program of the FLBPR or the protected block of FLASH memory is prohibited. Mass erase is disabled whenever any block is protected (FLBPR does not equal \$FF). The FLBPR itself can be erased or programmed only with an external voltage,  $V_{TST}$ , present on the  $\overline{IRQ}$  pin. This voltage also allows entry from reset into the monitor mode.

2. The time between each FLASH address change, or the time between the last FLASH address programmed to clearing PGM bit, must not exceed the maximum programming time,  $t_{PROG}$  maximum.

**Algorithm for Programming a Row (32 Bytes) of FLASH Memory**



**NOTES:**

The time between each FLASH address change (step 7 to step 7), or the time between the last FLASH address programmed to clearing PGM bit (step 7 to step 10) must not exceed the maximum programming time,  $t_{PROG\ max}$ .

This row program algorithm assumes the row/s to be programmed are initially erased.

**Figure 2-4. FLASH Programming Flowchart**

## Chapter 3

# Analog-to-Digital Converter (ADC)

### 3.1 Introduction

This section describes the analog-to-digital converter (ADC). The ADC is an 8-bit, 4-channel analog-to-digital converter. The ADC module is only available on the MC68HC908QY2, MC68HC908QT2, MC68HC908QY4, and MC68HC908QT4.

### 3.2 Features

Features of the ADC module include:

- 4 channels with multiplexed input
- Linear successive approximation with monotonicity
- 8-bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock frequency

### 3.3 Functional Description

Four ADC channels are available for sampling external sources at pins PTA0, PTA1, PTA4, and PTA5. An analog multiplexer allows the single ADC converter to select one of the four ADC channels as an ADC voltage input (ADCVIN). ADCVIN is converted by the successive approximation register-based counters. The ADC resolution is eight bits. When the conversion is completed, ADC puts the result in the ADC data register and sets a flag or generates an interrupt.

Figure 3-2 shows a block diagram of the ADC.

#### 3.3.1 ADC Port I/O Pins

PTA0, PTA1, PTA4, and PTA5 are general-purpose I/O pins that are shared with the ADC channels. The channel select bits (ADC status and control register (ADSCR), \$003C), define which ADC channel/port pin will be used as the input signal. The ADC overrides the port I/O logic by forcing that pin as input to the ADC. The remaining ADC channels/port pins are controlled by the port I/O logic and can be used as general-purpose I/O. Writes to the port register or data direction register (DDR) will not have any effect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return a 0 if the corresponding DDR bit is at 0. If the DDR bit is at 1, the value in the port data latch is read.

**LVIPWRD — LVI Power Disable Bit**

LVIPWRD disables the LVI module.

- 1 = LVI module power disabled
- 0 = LVI module power enabled

**LVI5OR3 — LVI 5-V or 3-V Operating Mode Bit**

LVI5OR3 selects the voltage operating mode of the LVI module. The voltage mode selected for the LVI should match the operating  $V_{DD}$  for the LVI's voltage trip points for each of the modes.

- 1 = LVI operates in 5-V mode
- 0 = LVI operates in 3-V mode

**NOTE**

*The LVI5OR3 bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.*

**SSREC — Short Stop Recovery Bit**

SSREC enables the CPU to exit stop mode with a delay of 32 BUSCLKX4 cycles instead of a 4096 BUSCLKX4 cycle delay.

- 1 = Stop mode recovery after 32 BUSCLKX4 cycles
- 0 = Stop mode recovery after 4096 BUSCLKX4 cycles

**NOTE**

*Exiting stop mode by an LVI reset will result in the long stop recovery.*

The system stabilization time for power-on reset and long stop recovery (both 4096 BUSCLKX4 cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32 BUSCLKX4 delay must be greater than the LVI's turn on time to avoid a period in startup where the LVI is not protecting the MCU.

**STOP — STOP Instruction Enable Bit**

STOP enables the STOP instruction.

- 1 = STOP instruction enabled
- 0 = STOP instruction treated as illegal opcode

**COPD — COP Disable Bit**

COPD disables the COP module.

- 1 = COP module disabled
- 0 = COP module enabled

### 7.3.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	V	1	1	H	I	N	Z	C
Write:								
Reset:	X	1	1	X	1	X	X	X

X = Indeterminate

**Figure 7-6. Condition Code Register (CCR)**

#### V — Overflow Flag

The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.

- 1 = Overflow
- 0 = No overflow

#### H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C flags to determine the appropriate correction factor.

- 1 = Carry between bits 3 and 4
- 0 = No carry between bits 3 and 4

#### I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

- 1 = Interrupts disabled
- 0 = Interrupts enabled

**NOTE**

*To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.*

After the I bit is cleared, the highest-priority interrupt request is serviced first.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

#### N — Negative Flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

- 1 = Negative result
- 0 = Non-negative result



### 8.7.1 IRQ Input Pins ( $\overline{\text{IRQ}}$ )

The  $\overline{\text{IRQ}}$  pin provides a maskable external interrupt source. The  $\overline{\text{IRQ}}$  pin contains an internal pullup device.

## 8.8 Registers


The IRQ status and control register (INTSCR) controls and monitors operation of the IRQ module. See [Chapter 5 Configuration Register \(CONFIG\)](#).

The INTSCR has the following functions:

- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks the IRQ interrupt request
- Controls triggering sensitivity of the  $\overline{\text{IRQ}}$  interrupt pin

Address: \$001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF	0	IMASK	MODE
Write:						ACK		
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 8-3. IRQ Status and Control Register (INTSCR)**

#### IRQF — IRQ Flag

This read-only status bit is set when the IRQ interrupt is pending.

1 =  $\overline{\text{IRQ}}$  interrupt pending

0 =  $\overline{\text{IRQ}}$  interrupt not pending

#### ACK — IRQ Interrupt Request Acknowledge Bit

Writing a 1 to this write-only bit clears the IRQ latch. ACK always reads as 0.

#### IMASK — IRQ Interrupt Mask Bit

Writing a 1 to this read/write bit disables the IRQ interrupt request.

1 = IRQ interrupt request disabled

0 = IRQ interrupt request enabled

#### MODE — IRQ Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the  $\overline{\text{IRQ}}$  pin.

1 =  $\overline{\text{IRQ}}$  interrupt request on falling edges and low levels

0 =  $\overline{\text{IRQ}}$  interrupt request on falling edges only

### 11.4.2 Crystal Amplifier Output Pin (OSC2/PTA4/BUSCLKX4)

For the XTAL oscillator device, the OSC2 pin is the crystal oscillator inverting amplifier output.

For the external clock option, the OSC2 pin is dedicated to the PTA4 I/O function. The OSC2EN bit has no effect.

For the internal oscillator or RC oscillator options, the OSC2 pin can assume other functions according to [Table 1-3. Function Priority in Shared Pins](#), or the output of the oscillator clock (BUSCLKX4).

**Table 11-1. OSC2 Pin Function**

Option	OSC2 Pin Function
XTAL oscillator	Inverting OSC1
External clock	PTA4 I/O
Internal oscillator or RC oscillator	Controlled by OSC2EN bit in PTAPUE register OSC2EN = 0: PTA4 I/O OSC2EN = 1: BUSCLKX4 output

### 11.4.3 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal comes from the system integration module (SIM) and enables/disables either the XTAL oscillator circuit, the RC oscillator, or the internal oscillator.

### 11.4.4 XTAL Oscillator Clock (XTALCLK)

XTALCLK is the XTAL oscillator output signal. It runs at the full speed of the crystal ( $f_{XCLK}$ ) and comes directly from the crystal oscillator circuit. [Figure 11-2](#) shows only the logical relation of XTALCLK to OSC1 and OSC2 and may not represent the actual circuitry. The duty cycle of XTALCLK is unknown and may depend on the crystal and other external factors. Also, the frequency and amplitude of XTALCLK can be unstable at start up.

### 11.4.5 RC Oscillator Clock (RCCLK)

RCCLK is the RC oscillator output signal. Its frequency is directly proportional to the time constant of external R and internal C. [Figure 11-3](#) shows only the logical relation of RCCLK to OSC1 and may not represent the actual circuitry.

### 11.4.6 Internal Oscillator Clock (INTCLK)

INTCLK is the internal oscillator output signal. Its nominal frequency is fixed to 12.8 MHz, but it can be also trimmed using the oscillator trimming feature of the OSCTRIM register (see [11.3.1.1 Internal Oscillator Trimming](#)).

### 11.4.7 Oscillator Out 2 (BUSCLKX4)

BUSCLKX4 is the same as the input clock (XTALCLK, RCCLK, or INTCLK). This signal is driven to the SIM module and is used to determine the COP cycles.

### 11.4.8 Oscillator Out (BUSCLKX2)

The frequency of this signal is equal to half of the BUSCLKX4, this signal is driven to the SIM for generation of the bus clocks used by the CPU and other modules on the MCU. BUSCLKX2 will be divided



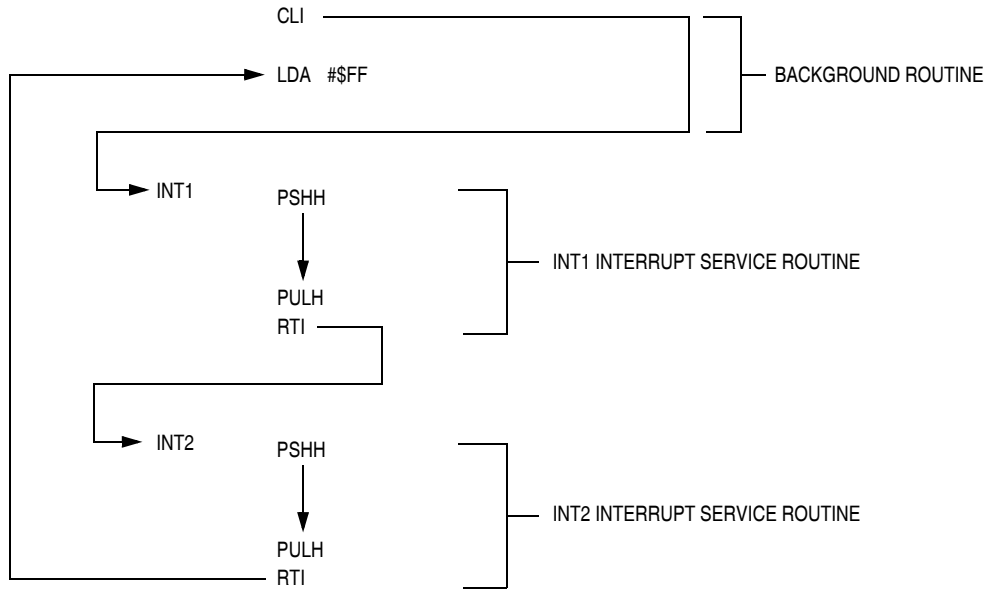


Figure 13-10. Interrupt Recognition Example

### 13.6.1.2 SWI Instruction

The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

**NOTE**

*A software interrupt pushes PC onto the stack. A software interrupt does **not** push PC - 1, as a hardware interrupt does.*

### 13.6.2 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. [Table 13-3](#) summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

Table 13-3. Interrupt Sources

Priority	Source	Flag	Mask <sup>(1)</sup>	INT Register Flag	Vector Address
Highest ↑ ↓ Lowest	Reset	—	—	—	\$FFFE-\$FFFF
	SWI instruction	—	—	—	\$FFFC-\$FFFD
	$\overline{\text{IRQ}}$ pin	IRQF	IMASK	IF1	\$FFFA-\$FFFB
	Timer channel 0 interrupt	CH0F	CH0IE	IF3	\$FFF6-\$FFF7
	Timer channel 1 interrupt	CH1F	CH1IE	IF4	\$FFF4-\$FFF5
	Timer overflow interrupt	TOF	TOIE	IF5	\$FFF2-\$FFF3
	Keyboard interrupt	KEYF	IMASKK	IF14	\$FFE0-\$FFE1
	ADC conversion complete interrupt	COCO	AIEN	IF15	\$FFDE-\$FFDF

1. The I bit in the condition code register is a global mask for all interrupt sources except the SWI instruction.

### 13.6.2.1 Interrupt Status Register 1

Address: \$FE04

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	IF5	IF4	IF3	0	IF1	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 13-11. Interrupt Status Register 1 (INT1)**

#### IF1 and IF3–IF5 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

#### Bit 0, 1, 3, and 7 — Always read 0

### 13.6.2.2 Interrupt Status Register 2

Address: \$FE05

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IF14	0	0	0	0	0	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 13-12. Interrupt Status Register 2 (INT2)**

#### IF14 — Interrupt Flags

This flag indicates the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

#### Bit 0–6 — Always read 0

### 13.6.2.3 Interrupt Status Register 3

Address: \$FE06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	IF15
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 13-13. Interrupt Status Register 3 (INT3)**

#### IF15 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

#### Bit 1–7 — Always read 0

### 13.6.3 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

### 13.6.4 Break Interrupts

The break module can stop normal program flow at a software programmable break point by asserting its break interrupt output. (See [Chapter 15 Development Support](#).) The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

### 13.6.5 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

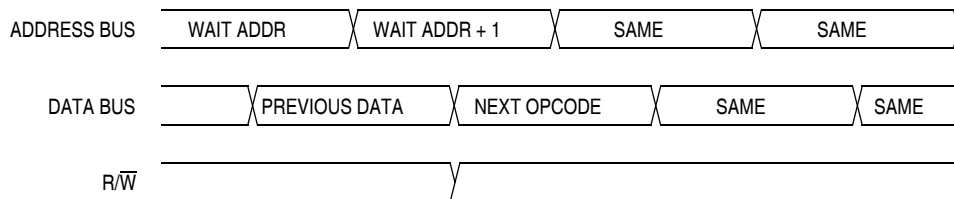
Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a two-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

## 13.7 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power- consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described below. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

### 13.7.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. [Figure 13-14](#) shows the timing for wait mode entry.



NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

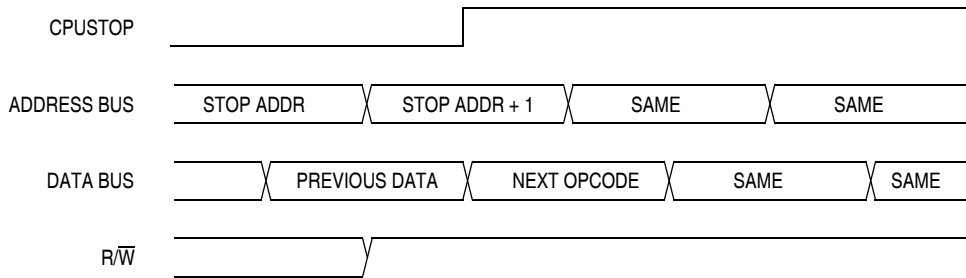
**Figure 13-14. Wait Mode Entry Timing**

## System Integration Module (SIM)

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. [Figure 13-17](#) shows stop mode entry timing and [Figure 13-18](#) shows the stop mode recovery time from interrupt or break.

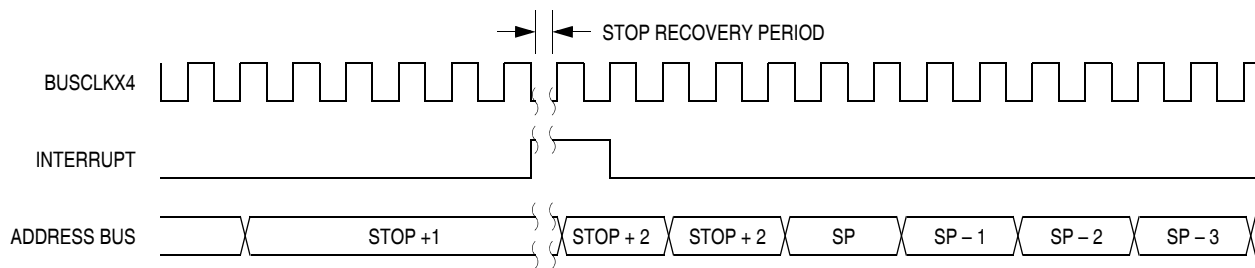
### NOTE

To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.



NOTE: Previous data can be operand data or the STOP opcode, depending on the last instruction.

**Figure 13-17. Stop Mode Entry Timing**



**Figure 13-18. Stop Mode Recovery from Interrupt**

## 13.8 SIM Registers

The SIM has three memory mapped registers. [Table 13-4](#) shows the mapping of these registers.

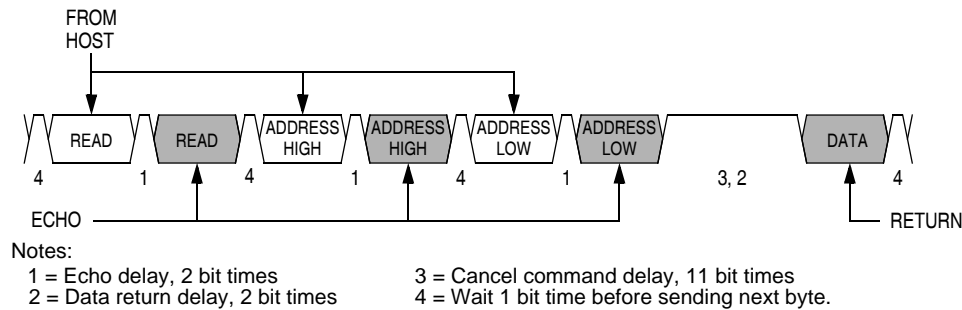
**Table 13-4. SIM Registers**

Address	Register	Access Mode
\$FE00	BSR	User
\$FE01	SRSR	User
\$FE03	BFCR	User

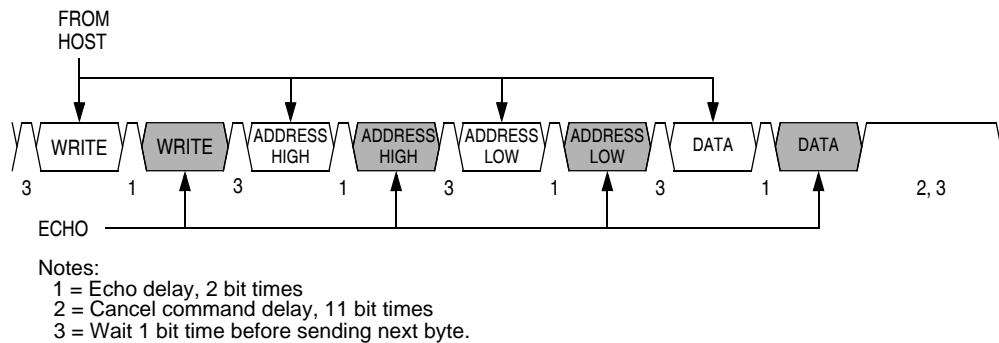
The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

**NOTE**

*Wait one bit time after each echo before sending the next byte.*



**Figure 15-15. Read Transaction**



**Figure 15-16. Write Transaction**

A brief description of each monitor mode command is given in [Table 15-3](#) through [Table 15-8](#).

**Table 15-3. READ (Read Memory) Command**

<b>Description</b>	Read byte from memory
<b>Operand</b>	2-byte address in high-byte:low-byte order
<b>Data Returned</b>	Returns contents of specified address
<b>Opcode</b>	\$4A
<b>Command Sequence</b>	



### 16.3 Functional Operating Range

Characteristic	Symbol	Value	Unit	Temp. Code
Operating temperature range	$T_A$	-40 to +125 -40 to +105 -40 to +85	•C	M V C
Operating voltage range	$V_{DD}$	2.7 to 5.5	V	—

### 16.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance	$\theta_{JA}$		•C/W
8-pin PDIP		105	
8-pin SOIC		142	
8-pin DFN		173	
16-pin PDIP		76	
16-pin SOIC 16-pin TSSOP		90 133	
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation <sup>(1)</sup>	$P_D$	$P_D = (I_{DD} \times V_{DD})$ $+ P_{I/O} = K/(T_J + 273 \cdot C)$	W
Constant <sup>(2)</sup>	K	$P_D \times (T_A + 273 \cdot C)$ $+ P_D^2 \times \theta_{JA}$	W/•C
Average junction temperature	$T_J$	$T_A + (P_D \times \theta_{JA})$	•C
Maximum junction temperature	$T_{JM}$	150	•C

1. Power dissipation is a function of temperature.
2. K constant unique to the device. K can be determined for a known  $T_A$  and measured  $P_D$ . With this value of K,  $P_D$  and  $T_J$  can be determined for any value of  $T_A$ .

### 16.11 3-V Control Timing

Characteristic <sup>(1)</sup>	Symbol	Min	Max	Unit
Internal operating frequency	$f_{OP}$ ( $f_{Bus}$ )	—	4	MHz
Internal clock period ( $1/f_{OP}$ )	$t_{cyc}$	250	—	ns
$\overline{RST}$ input pulse width low	$t_{RL}$	200	—	ns
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	$t_{LIH}$	200	—	ns
$\overline{IRQ}$ interrupt pulse period	$t_{LIL}$	Note <sup>(2)</sup>	—	$t_{cyc}$

- $V_{DD} = 2.7$  to  $3.3$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ ; timing shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.
- The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1  $t_{cyc}$ .

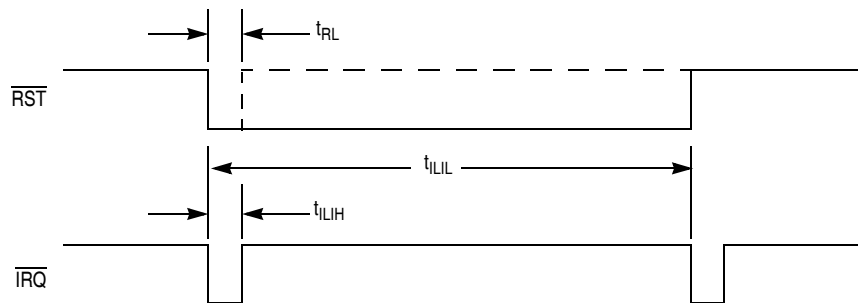


Figure 16-7.  $\overline{RST}$  and  $\overline{IRQ}$  Timing



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**MECHANICAL OUTLINES  
 DICTIONARY**


DOCUMENT NO: 98ARL10557D

PAGE: 1452

DO NOT SCALE THIS DRAWING

REV: A

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HP-VDFDP-N.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

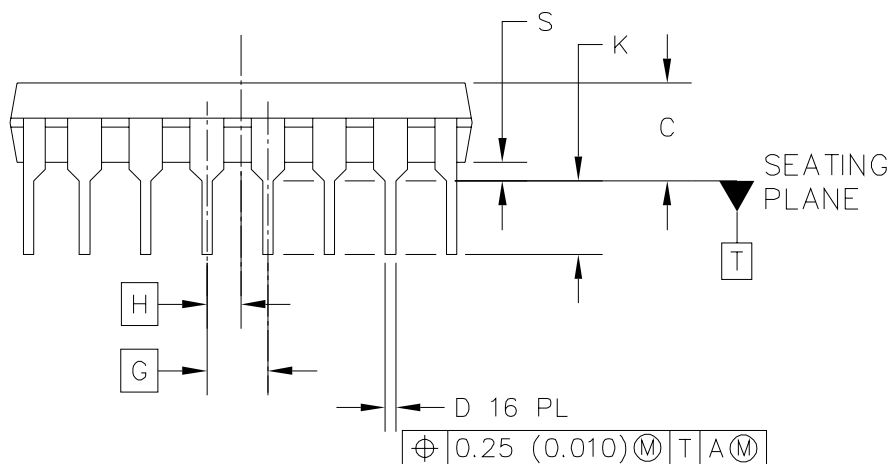
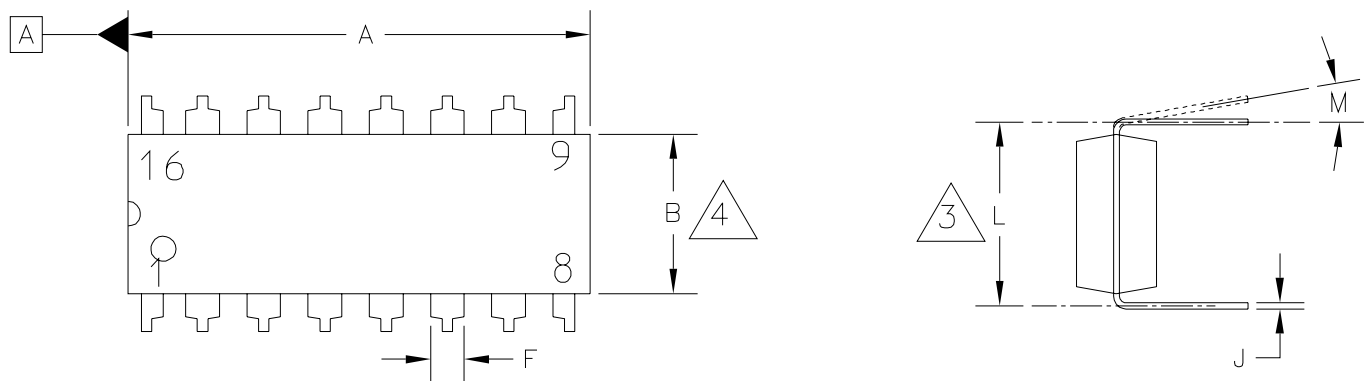
TITLE:THERMALLY ENHANCED DUAL  
 FLAT NO LEAD PACKAGE (DFN)  
 8 TERMINAL, 0.8 PITCH(4 X 4 X 1)

CASE NUMBER: 1452-01

STANDARD: NON-JEDEC

PACKAGE CODE: 6165

SHEET: 4 OF 5



TITLE:

16 LD PDIP

CASE NUMBER: 648-08

STANDARD: NON-JEDEC

PACKAGE CODE: 0006

SHEET: 1 OF 4



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MECHANICAL OUTLINES  
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DOCUMENT NO: 98ASH70247A

PAGE: 948F

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REV: B

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

TITLE:  
 16 LD TSSOP, PITCH 0.65MM

CASE NUMBER: 948F-01

STANDARD: JEDEC

PACKAGE CODE: 6117

SHEET: 3 OF 4