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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	5
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908qt2cdwer

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List of Chapters



Chapter 1 General Description

1.1 Introduction

The MC68HC908QY4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Device	FLASH Memory Size	Analog-to-Digital Converter	Pin Count
MC68HC908QT1	1536 bytes	_	8 pins
MC68HC908QT2	1536 bytes	4 ch, 8 bit	8 pins
MC68HC908QT4	4096 bytes	4 ch, 8 bit	8 pins
MC68HC908QY1	1536 bytes	—	16 pins
MC68HC908QY2	1536 bytes	4 ch, 8 bit	16 pins
MC68HC908QY4	4096 bytes	4 ch, 8 bit	16 pins

Table 1-1. Summary of Device Variations

1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- 5-V and 3-V operating voltages (V_{DD})
- 8-MHz internal bus operation at 5 V, 4-MHz at 3 V
- Trimmable internal oscillator
 - 3.2 MHz internal bus operation
 - 8-bit trim capability allows 0.4% accuracy⁽¹⁾
 - ± 25% untrimmed
- Auto wakeup from STOP capability
- Configuration (CONFIG) register for MCU configuration options, including:
 - Low-voltage inhibit (LVI) trip point
- In-system FLASH programming
- FLASH security⁽²⁾

^{1.} The oscillator frequency is guaranteed to $\pm 5\%$ over temperature and voltage range after trimming.

No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.



General Description

Input/Output (I/O) Section



2.4 Input/Output (I/O) Section

Addresses \$0000–\$003F, shown in Figure 2-2, contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- \$FE00 Break status register, BSR
- \$FE01 Reset status register, SRSR
- \$FE02 Break auxiliary register, BRKAR
- \$FE03 Break flag control register, BFCR
- \$FE04 Interrupt status register 1, INT1
- \$FE05 Interrupt status register 2, INT2
- \$FE06 Interrupt status register 3, INT3
- \$FE07 Reserved
- \$FE08 FLASH control register, FLCR
- \$FE09 Break address register high, BRKH
- \$FE0A Break address register low, BRKL
- \$FE0B Break status and control register, BRKSCR
- \$FE0C LVI status register, LVISR
- \$FE0D Reserved
- \$FFBE FLASH block protect register, FLBPR
- \$FFC0 Internal OSC trim value (factory programmed, VDD = 5.0 V)
- \$FFC1 Internal OSC trim value (factory programmed, VDD = 3.0 V)
- \$FFFF COP control register, COPCTL

Addr.	Register Name	_	Bit 7	6	5	4	3	2	1	Bit 0
	Port A Data Register	Read:	В	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
\$0000	(PTA) See page 98.	Write: Reset:				Unaffecte	d by reset			
¢0001	Port B Data Register	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
φυυυι	See page 100.	Reset:				Unaffecte	d by reset			
\$0002	Unimplemented	[
\$0003	Unimplemented	[
	Data Direction Register A	Read:	B	B	DDBA5	DDRA4	DDBA3	0	DDBA1	
\$0004	(DDRA)	Write:			DDTINO	BBIIN	DDI II IO		DBIII	DDTINO
	See page 98.	Reset:	0	0	0	0	0	0	0	0
\$0005	Data Direction Register B (DDRB)	Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
	See page 101.	Reset:	0	0	0	0	0	0	0	0
				= Unimplem	ented	R	= Reserved	U = Unafi	ected	

Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 5)

Analog-to-Digital Converter (ADC)



RST, IRQ: Pins have internal (about 30K Ohms) pull up

PTA[0:5]: High current sink and source capability

PTA[0:5]: Pins have programmable keyboard interrupt and pull up

PTB[0:7]: Not available on 8-pin devices – MC68HC908QT1, MC68HC908QT2, and MC68HC908QT4 (see note in 12.1 Introduction)

ADC: Not available on the MC68HC908QY1 and MC68HC908QT1

Figure 3-1. Block Diagram Highlighting ADC Block and Pins



Computer Operating Properly (COP)

The COP counter is a free-running 6-bit counter preceded by the 12-bit system integration module (SIM) counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after 262,128 or 8176 BUSCLKX4 cycles; depending on the state of the COP rate select bit, COPRS, in configuration register 1. With a 262,128 BUSCLKX4 cycle overflow option, the internal 12.8-MHz oscillator gives a COP timeout period of 20.48 ms. Writing any value to location \$FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12–5 of the SIM counter.

NOTE

Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.

A COP reset pulls the $\overline{\text{RST}}$ pin low (if the RSTEN bit is set in the CONFIG1 register) for 32 × BUSCLKX4 cycles and sets the COP bit in the reset status register (RSR). See 13.8.1 SIM Reset Status Register.

NOTE

Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.

6.3 I/O Signals

The following paragraphs describe the signals shown in Figure 6-1.

6.3.1 BUSCLKX4

BUSCLKX4 is the oscillator output signal. BUSCLKX4 frequency is equal to the internal oscillator frequency, the crystal frequency, or the RC-oscillator frequency.

6.3.2 STOP Instruction

The STOP instruction clears the SIM counter.

6.3.3 COPCTL Write

Writing any value to the COP control register (COPCTL) (see 6.4 COP Control Register) clears the COP counter and clears stages 12–5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector.

6.3.4 Power-On Reset

The power-on reset (POR) circuit in the SIM clears the SIM counter $4096 \times BUSCLKX4$ cycles after power up.

6.3.5 Internal Reset

An internal reset clears the SIM counter and the COP counter.

6.3.6 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register 1 (CONFIG1). See Chapter 5 Configuration Register (CONFIG).



Central Processor Unit (CPU)



Figure 7-1. CPU Registers

7.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.



Figure 7-2. Accumulator (A)

7.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.



Figure 7-3. Index Register (H:X)





Source				o	Eff	ec CC	t R		ess	ode	and	Se
Form	Operation	Description	v	н	1	N	z	С	Addr Node	Dpco	Dper	Sycle
JMP opr JMP opr JMP opr,X JMP opr,X JMP ,X	Jump	PC ← Jump Address	_	_	_	_	_	_	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh II ee ff ff	2 3 4 3 2
JSR opr JSR opr JSR opr,X JSR opr,X JSR ,X	Jump to Subroutine	$PC \leftarrow (PC) + n (n = 1, 2, or 3)$ $Push (PCL); SP \leftarrow (SP) - 1$ $Push (PCH); SP \leftarrow (SP) - 1$ $PC \leftarrow Unconditional Address$	_	-	-	_	_	_	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	45654
LDA #opr LDA opr LDA opr,X LDA opr,X LDA opr,X LDA ,X LDA opr,SP LDA opr,SP	Load A from M	A ← (M)	0	_	_	ţ	ţ	_	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh II ee ff ff ee ff	2 3 4 3 2 4 5
LDHX #opr LDHX opr	Load H:X from M	$H:X \leftarrow (M:M+1)$	0	-	-	ţ	ţ	-	IMM DIR	45 55	ii jj dd	3 4
LDX #opr LDX opr LDX opr LDX opr,X LDX opr,X LDX opr,SP LDX opr,SP LDX opr,SP	Load X from M	X ← (M)	0	_	_	ţ	ţ	_	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh II ee ff ff ff ee ff	2 3 4 3 2 4 5
LSL opr LSLA LSLX LSL opr,X LSL ,X LSL ,A LSL opr,SP	Logical Shift Left (Same as ASL)	Image: Contract of the second sec	ţ	_	_	ţ	ţ	ţ	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 4 3 5
LSR opr LSRA LSRX LSR opr,X LSR ,X LSR opr,SP	Logical Shift Right	$0 \rightarrow \boxed{\begin{array}{c} & & \\ & & \\ & & \\ & & \\ & b7 & b0 \end{array}} \rightarrow \boxed{C}$	ţ	_	_	0	ţ	ţ	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	4 1 4 3 5
MOV opr,opr MOV opr,X+ MOV #opr,opr MOV X+,opr	Move	$(M)_{\text{Destination}} \leftarrow (M)_{\text{Source}}$ $H:X \leftarrow (H:X) + 1 \text{ (IX+D, DIX+)}$	0	_	_	t	t	-	DD DIX+ IMD IX+D	4E 5E 6E 7E	dd dd dd ii dd dd	5 4 4 4
MUL	Unsigned multiply	$X:A \leftarrow (X) \times (A)$	-	0	-	-	-	0	INH	42		5
NEG opr NEGA NEGX NEG opr,X NEG ,X NEG opr,SP	Negate (Two's Complement)	$\begin{array}{l} M \leftarrow -(M) = \$00 - (M) \\ A \leftarrow -(A) = \$00 - (A) \\ X \leftarrow -(X) = \$00 - (X) \\ M \leftarrow -(M) = \$00 - (M) \\ M \leftarrow -(M) = \$00 - (M) \end{array}$	ţ	-	-	ţ	ţ	ţ	DIR INH INH IX1 IX SP1	30 40 50 60 70 9E60	dd ff ff	4 1 4 3 5
NOP	No Operation	None		-	-	-	-	-	INH	9D		1
NSA	Nibble Swap A	A ← (A[3:0]:A[7:4])	-	-	-	-	-	-	INH	62		3
ORA #opr ORA opr ORA opr ORA opr,X ORA opr,X ORA opr,SP ORA opr,SP	Inclusive OR A and M	A ← (A) (M)	0	_	_	ţ	ţ	_	IMM DIR EXT IX2 IX1 IX SP1 SP2	AA BA CA DA EA FA 9EEA 9EDA	ii dd hh II ee ff ff ee ff	2 3 4 4 3 2 4 5
PSHA	Push A onto Stack	Push (A); SP \leftarrow (SP) – 1	_	_	-	-	-	-	INH	87		2
PSHH	Push H onto Stack	Push (H); SP ← (SP) – 1	-	-	-	-	-	-	INH	8B		2
PSHX	Push X onto Stack	Push (X); SP \leftarrow (SP) – 1	-	-	-	-	-	-	INH	89		2



Functional Description



Figure 9-2. Keyboard Interrupt Block Diagram

If the MODEK bit is set, the keyboard interrupt inputs are both falling edge and low-level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt inputs and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt inputs. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the central processor unit (CPU) loads the program counter with the vector address at locations \$FFE0 and \$FFE1.
- Return of all enabled keyboard interrupt inputs to logic 1 As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set. The auto wakeup interrupt input, AWUIREQ, will be cleared only by writing to ACKK bit in KBSCR or reset.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

If the MODEK bit is clear, the keyboard interrupt pin is falling-edge sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt input stays at logic 0.

The keyboard flag bit (KEYF) in the keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

Oscillator Module (OSC)



ADC: Not available on the MC68HC908QY1 and MC68HC908QT1

Figure 11-1. Block Diagram Highlighting OSC Block and Pins

11.3.1 Internal Oscillator

The internal oscillator circuit is designed for use with no external components to provide a clock source with tolerance less than $\pm 25\%$ untrimmed. An 8-bit trimming register allows adjustment to a tolerance of less than $\pm 5\%$.

The internal oscillator will generate a clock of 12.8 MHz typical (INTCLK) resulting in a bus speed (internal clock \div 4) of 3.2 MHz. 3.2 MHz came from the maximum bus speed guaranteed at 3 V which is 4 MHz.Since the internal oscillator will have a ±25% tolerance (pre-trim), then the +25% case should not allow a frequency higher than 4 MHz:

3.2 MHz + 25% = 4 MHz

Figure 11-3 shows how BUSCLKX4 is derived from INTCLK and, like the RC oscillator, OSC2 can output BUSCLKX4 by setting OSC2EN in PTAPUE register. See Chapter 12 Input/Output Ports (PORTS)



Oscillator Module (OSC)

11.3.3 XTAL Oscillator

The XTAL oscillator circuit is designed for use with an external crystal or ceramic resonator to provide an accurate clock source. In this configuration, the OSC2 pin is dedicated to the external crystal circuit. The OSC2EN bit in the port A pullup enable register has no effect when this clock mode is selected.

In its typical configuration, the XTAL oscillator is connected in a Pierce oscillator configuration, as shown in Figure 11-2. This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X₁
- Fixed capacitor, C₁
- Tuning capacitor, C₂ (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_s (optional)

NOTE

The series resistor (R_s) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.



Note 1.

 R_s can be zero (shorted) when used with higher-frequency crystals. Refer to manufacturer's data. See Chapter 16 Electrical Specifications for component value recommendations.





Oscillator Module (OSC)

11.4.2 Crystal Amplifier Output Pin (OSC2/PTA4/BUSCLKX4)

For the XTAL oscillator device, the OSC2 pin is the crystal oscillator inverting amplifier output.

For the external clock option, the OSC2 pin is dedicated to the PTA4 I/O function. The OSC2EN bit has no effect.

For the internal oscillator or RC oscillator options, the OSC2 pin can assume other functions according to Table 1-3. Function Priority in Shared Pins, or the output of the oscillator clock (BUSCLKX4).

Option	OSC2 Pin Function
XTAL oscillator	Inverting OSC1
External clock	PTA4 I/O
Internal oscillator or RC oscillator	Controlled by OSC2EN bit in PTAPUE register OSC2EN = 0: PTA4 I/O OSC2EN = 1: BUSCLKX4 output

Table 11-1. OSC2 Pin Function

11.4.3 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal comes from the system integration module (SIM) and enables/disables either the XTAL oscillator circuit, the RC oscillator, or the internal oscillator.

11.4.4 XTAL Oscillator Clock (XTALCLK)

XTALCLK is the XTAL oscillator output signal. It runs at the full speed of the crystal (f_{XCLK}) and comes directly from the crystal oscillator circuit. Figure 11-2 shows only the logical relation of XTALCLK to OSC1 and OSC2 and may not represent the actual circuitry. The duty cycle of XTALCLK is unknown and may depend on the crystal and other external factors. Also, the frequency and amplitude of XTALCLK can be unstable at start up.

11.4.5 RC Oscillator Clock (RCCLK)

RCCLK is the RC oscillator output signal. Its frequency is directly proportional to the time constant of external R and internal C. Figure 11-3 shows only the logical relation of RCCLK to OSC1 and may not represent the actual circuitry.

11.4.6 Internal Oscillator Clock (INTCLK)

INTCLK is the internal oscillator output signal. Its nominal frequency is fixed to 12.8 MHz, but it can be also trimmed using the oscillator trimming feature of the OSCTRIM register (see 11.3.1.1 Internal Oscillator Trimming).

11.4.7 Oscillator Out 2 (BUSCLKX4)

BUSCLKX4 is the same as the input clock (XTALCLK, RCCLK, or INTCLK). This signal is driven to the SIM module and is used to determine the COP cycles.

11.4.8 Oscillator Out (BUSCLKX2)

The frequency of this signal is equal to half of the BUSCLKX4, this signal is driven to the SIM for generation of the bus clocks used by the CPU and other modules on the MCU. BUSCLKX2 will be divided





control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE

In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.

14.4.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM can generate a PWM signal. The value in the TIM counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM counter modulo registers. The time between overflows is the period of the PWM signal

As Figure 14-3 shows, the output compare value in the TIM channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM to clear the channel pin on output compare if the state of the PWM pulse is logic 1 (ELSxA = 0). Program the TIM to set the pin if the state of the PWM pulse is logic 0 (ELSxA = 1).

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output The frequency of an 8-bit PWM signal is variable in 256 increments. Writing \$00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000. See 14.9.1 TIM Status and Control Register.

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing \$0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.



Figure 14-3. PWM Period and Pulse Width



Input/Output Registers

When ELSxB:A = 00, this read/write bit selects the initial output level of the TCHx pin (see Table 14-3). Reset clears the MSxA bit.

1 = Initial output level low

0 = Initial output level high

NOTE

Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).

MSxB	MSxA	ELSxB	ELSxA	Mode	Configuration
Х	0	0	0		Pin under port control; initial output level high
Х	1	0	0	Output preset	Pin under port control; initial output level low
0	0	0	1		Capture on rising edge only
0	0	1	0	Input capture	Capture on falling edge only
0	0	1	1		Capture on rising or falling edge
0	1	0	0		Software compare only
0	1	0	1	Output compare	Toggle output on compare
0	1	1	0	or PWM	Clear output on compare
0	1	1	1		Set output on compare
1	Х	0	1	Buffered output	Toggle output on compare
1	Х	1	0	compare or	Clear output on compare
1	Х	1	1	buffered PWM	Set output on compare

Table 14-3. Mode, Edge, and Level Selection

ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to an I/O port, and pin TCHx is available as a general-purpose I/O pin. Table 14-3 shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

NOTE

After initially enabling a TIM channel register for input capture operation and selecting the edge sensitivity, clear CHxF to ignore any erroneous edge detection flags.

TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM counter overflows. When channel x is an input capture channel, TOVx has no effect Reset clears the TOVx bit.

1 = Channel x pin toggles on TIM counter overflow.

0 = Channel x pin does not toggle on TIM counter overflow.

NOTE

When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.

Development Support



RST, IRQ: Pins have internal (about 30K Ohms) pull up

PTA[0:5]: High current sink and source capability

PTA[0:5]: Pins have programmable keyboard interrupt and pull up

PTB[0:7]: Not available on 8-pin devices – MC68HC908QT1, MC68HC908QT2, and MC68HC908QT4 (see note in 12.1 Introduction)

ADC: Not available on the MC68HC908QY1 and MC68HC908QT1

Figure 15-1. Block Diagram Highlighting BRK and MON Blocks









Figure 15-10. Monitor Mode Circuit (External Clock, with High Voltage)



Figure 15-11. Monitor Mode Circuit (External Clock, No High Voltage)



16.9 3-V DC Electrical Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Мах	Unit
Output high voltage $I_{Load} = -0.6 \text{ mA}$, all I/O pins $I_{Load} = -4.0 \text{ mA}$, all I/O pins $I_{Load} = -10.0 \text{ mA}$, PTA0, PTA1, PTA3–PTA5 only	V _{OH}	V _{DD} -0.3 V _{DD} -1.0 V _{DD} -0.8			V
Maximum combined I _{OH} (all I/O pins)	I _{OHT}	—	—	50	mA
Output low voltage I _{Load} = 0.5 mA, all I/O pins I _{Load} = 6.0 mA, all I/O pins I _{Load} = 10.0 mA, PTA0, PTA1, PTA3–PTA5 only	V _{OL}			0.3 1.0 0.8	V
Maximum combined I _{OL} (all I/O pins)	I _{OLT}	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	V _{IH}	0.7 x V _{DD}	_	V _{DD}	V
Input low voltage PTA0–PTA5, PTB0–PTB7	V _{IL}	V _{SS}	—	0.3 x V _{DD}	V
Input hysteresis	V _{HYS}	0.06 x V _{DD}	—	—	V
DC injection current, all ports	I _{INJ}	-2	—	+2	mA
Total dc current injection (sum of all I/O)	I _{INJTOT}	-25	—	+25	mA
Ports Hi-Z leakage current	۱ _{IL}	-1	±0.1	+1	μA
Capacitance Ports (as input) Ports (as input)	C _{IN} C _{OUT}	—	_	12 8	pF
POR rearm voltage ⁽³⁾	V _{POR}	0	—	100	mV
POR rise time ramp rate ⁽⁴⁾	R _{POR}	0.035	_	—	V/ms
Monitor mode entry voltage	V _{TST}	V _{DD} + 2.5	—	V _{DD} + 4.0	V
Pullup resistors ⁽⁵⁾ PTA0–PTA5, PTB0–PTB7	R _{PU}	16	26	36	kΩ
Low-voltage inhibit reset, trip falling voltage	V _{TRIPF}	2.40	2.55	2.70	V
Low-voltage inhibit reset, trip rising voltage	V _{TRIPR}	2.50	2.65	2.80	V
Low-voltage inhibit reset/recover hysteresis	V _{HYS}		60	—	mV

1. V_{DD} = 2.7 to 3.3 Vdc, V_{SS} = 0 Vdc, T_A = T_L to $T_H,$ unless otherwise noted.

2. Typical values reflect average measurements at midpoint of voltage range, 25•C only.

3. Maximum is highest voltage that POR is guaranteed.

4. If minimum V_{DD} is not reached before the internal POR reset is released, the LVI will hold the part in reset until minimum V_{DD} is reached. 5. R_{PU} are measured at V_{DD} = 3.0 V





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NOTES :				
1. CONTROLLING DIMENSI	ON: MILLIMETE	R		
2. DIMENSIONS AND TOLE	RANCES PER AN	ISI Y14.5M-19	82.	
DIMENSION DOES NOT BURRS. MOLD FLASH C	INCLUDE MOLD DR GATE BURRS	FLASH, PROTRI SHALL NOT EX	JSIONS CEED 0	OR GATE 15 PER SIDE.
DIMENSION DOES NOT INTERLEAD FLASH OR	INCLUDE INTER PROTRUSION SH	RLEAD FLASH O IALL NOT EXCE	r prote Ed 0.25	RUSION. 5 PER SIDE.
5 DIMENSION DOES NOT DAMBAR PROTRUSION S THE DIMENSION AT MA	INCLUDE DAMB Shall be 0.08 Aximum materi	AR PROTRUSION TOTAL IN EXC AL CONDITION.	N. ALLO ESS OF	DWABLE
6. TERMINAL NUMBERS AR	RE SHOWN FOR F	REFERENCE ONL	Υ.	
$\overline{2}$ dimensions are to b	e determined	AT DATUM PLAN	VE -W-].
ITLE:		CASE NUMBER: S	948F-01	
ITLE: 16 I.D. TSSOP, PITCH	0.65MM	CASE NUMBER: S STANDARD: JEDE	948F-01	