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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908qy2vdwe">https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908qy2vdwe</a>

**MC68HC908QY4**  
**MC68HC908QT4**  
**MC68HC908QY2**  
**MC68HC908QT2**  
**MC68HC908QY1**  
**MC68HC908QT1**

**Data Sheet**

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## ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. ERASE is interlocked with the PGM bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Erase operation selected
- 0 = Erase operation unselected

## PGM — Program Control Bit

This read/write bit configures the memory for program operation. PGM is interlocked with the ERASE bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Program operation selected
- 0 = Program operation unselected

## 2.6.2 FLASH Page Erase Operation

Use the following procedure to erase a page of FLASH memory. A page consists of 64 consecutive bytes starting from addresses \$XX00, \$XX40, \$XX80, or \$XXC0. The 48-byte user interrupt vectors area also forms a page. Any FLASH memory page can be erased alone.

1. Set the ERASE bit and clear the MASS bit in the FLASH control register.
2. Read the FLASH block protect register.
3. Write any data to any FLASH location within the address range of the block to be erased.
4. Wait for a time,  $t_{NVS}$  (minimum 10  $\mu$ s).
5. Set the HVEN bit.
6. Wait for a time,  $t_{Erase}$  (minimum 1 ms or 4 ms).
7. Clear the ERASE bit.
8. Wait for a time,  $t_{NVH}$  (minimum 5  $\mu$ s).
9. Clear the HVEN bit.
10. After time,  $t_{RCV}$  (typical 1  $\mu$ s), the memory can be accessed in read mode again.

### NOTE

*Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.*

### CAUTION

*A page erase of the vector page will erase the internal oscillator trim values at \$FFC0 and \$FFC1.*

In applications that require more than 1000 program/erase cycles, use the 4 ms page erase specification to get improved long-term reliability. Any application can use this 4 ms page erase specification. However, in applications where a FLASH location will be erased and reprogrammed less than 1000 times, and speed is important, use the 1 ms page erase specification to get a shorter cycle time.

## Memory

8. Wait for time,  $t_{\text{PROG}}$  (minimum 30  $\mu\text{s}$ ).
9. Repeat step 7 and 8 until all desired bytes within the row are programmed.
10. Clear the PGM bit<sup>(1)</sup>.
11. Wait for time,  $t_{\text{NVH}}$  (minimum 5  $\mu\text{s}$ ).
12. Clear the HVEN bit.
13. After time,  $t_{\text{RCV}}$  (typical 1  $\mu\text{s}$ ), the memory can be accessed in read mode again.

### NOTE

*The COP register at location \$FFFF should not be written between steps 5–12, when the HVEN bit is set. Since this register is located at a valid FLASH address, unpredictable behavior may occur if this location is written while HVEN is set.*

This program sequence is repeated throughout the memory until all data is programmed.

### NOTE

*Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps. Do not exceed  $t_{\text{PROG}}$  maximum, see [16.16 Memory Characteristics](#).*

## 2.6.5 FLASH Protection

Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made to protect blocks of memory from unintentional erase or program operations due to system malfunction. This protection is done by use of a FLASH block protect register (FLBPR). The FLBPR determines the range of the FLASH memory which is to be protected. The range of the protected area starts from a location defined by FLBPR and ends to the bottom of the FLASH memory (\$FFF). When the memory is protected, the HVEN bit cannot be set in either ERASE or PROGRAM operations.

### NOTE

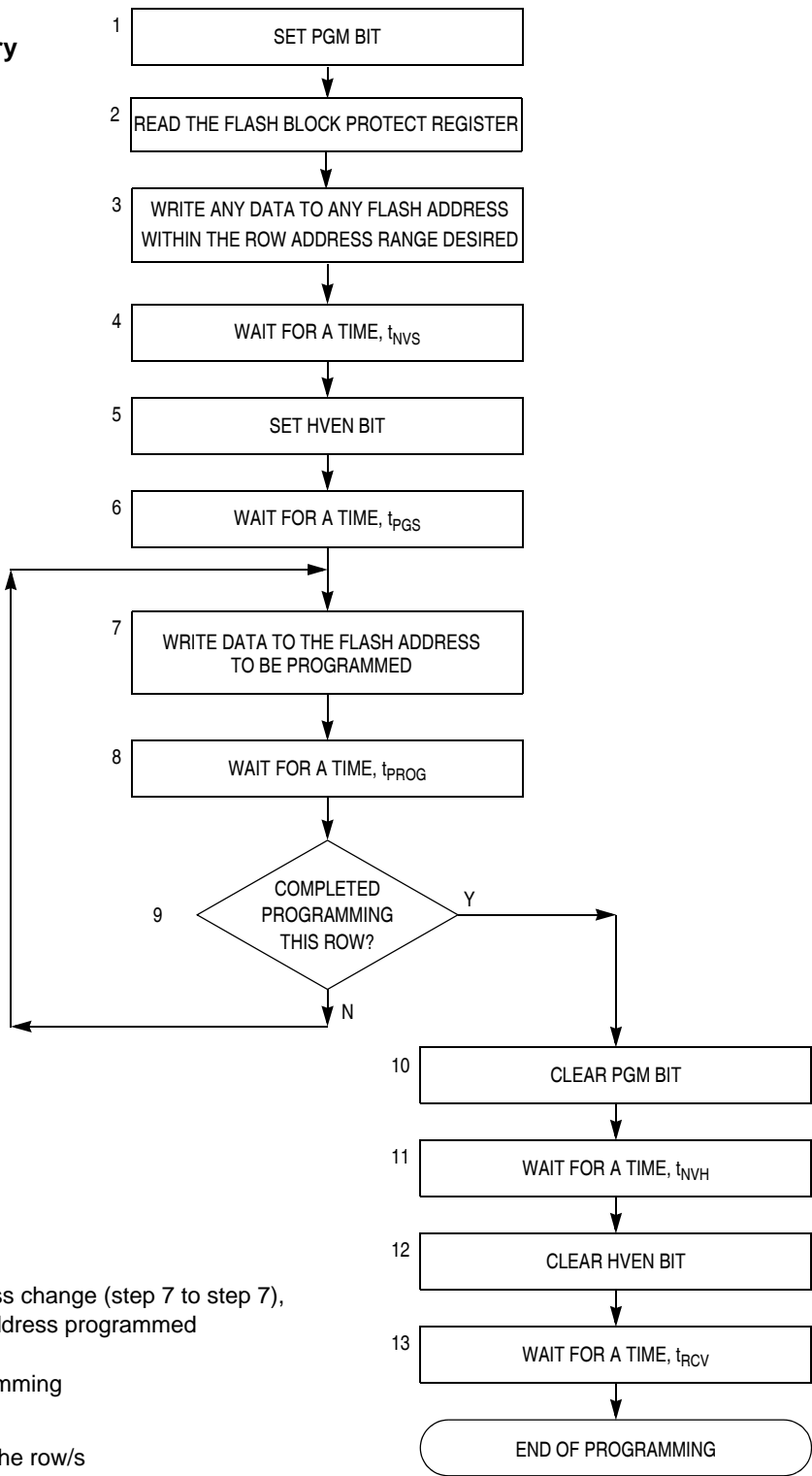
*In performing a program or erase operation, the FLASH block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.*

When the FLBPR is programmed with all 0's, the entire memory is protected from being programmed and erased. When all the bits are erased (all 1's), the entire memory is accessible for program and erase.

When bits within the FLBPR are programmed, they lock a block of memory. The address ranges are shown in [2.6.6 FLASH Block Protect Register](#). Once the FLBPR is programmed with a value other than \$FF, any erase or program of the FLBPR or the protected block of FLASH memory is prohibited. Mass erase is disabled whenever any block is protected (FLBPR does not equal \$FF). The FLBPR itself can be erased or programmed only with an external voltage,  $V_{\text{TST}}$ , present on the  $\overline{\text{IRQ}}$  pin. This voltage also allows entry from reset into the monitor mode.

2. The time between each FLASH address change, or the time between the last FLASH address programmed to clearing PGM bit, must not exceed the maximum programming time,  $t_{\text{PROG}}$  maximum.

**Algorithm for Programming  
a Row (32 Bytes) of FLASH Memory**



**NOTES:**

The time between each FLASH address change (step 7 to step 7), or the time between the last FLASH address programmed to clearing PGM bit (step 7 to step 10) must not exceed the maximum programming time,  $t_{PROG}$  max.

This row program algorithm assumes the row/s to be programmed are initially erased.

**Figure 2-4. FLASH Programming Flowchart**

## Configuration Register (CONFIG)

### IRQPUD — $\overline{\text{IRQ}}$ Pin Pullup Control Bit

- 1 = Internal pullup is disconnected
- 0 = Internal pullup is connected between  $\overline{\text{IRQ}}$  pin and  $V_{DD}$

### IRQEN — $\overline{\text{IRQ}}$ Pin Function Selection Bit

- 1 = Interrupt request function active in pin
- 0 = Interrupt request function inactive in pin

### OSCOPT1 and OSCOPT0 — Selection Bits for Oscillator Option

- (0, 0) Internal oscillator
- (0, 1) External oscillator
- (1, 0) External RC oscillator
- (1, 1) External XTAL oscillator

### RSTEN — $\overline{\text{RST}}$ Pin Function Selection

- 1 = Reset function active in pin
- 0 = Reset function inactive in pin

#### NOTE

The RSTEN bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.

Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

U = Unaffected

**Figure 5-2. Configuration Register 1 (CONFIG1)**

### COPRS (Out of STOP Mode) — COP Reset Period Selection Bit

- 1 = COP reset short cycle =  $8176 \times \text{BUSCLKX4}$
- 0 = COP reset long cycle =  $262,128 \times \text{BUSCLKX4}$

### COPRS (In STOP Mode) — Auto Wakeup Period Selection Bit

- 1 = Auto wakeup short cycle =  $512 \times \text{INTRCOSC}$
- 0 = Auto wakeup long cycle =  $16,384 \times \text{INTRCOSC}$

### LVISTOP — LVI Enable in Stop Mode Bit

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

- 1 = LVI enabled during stop mode
- 0 = LVI disabled during stop mode

### LVIRSTD — LVI Reset Disable Bit

LVIRSTD disables the reset signal from the LVI module.

- 1 = LVI module resets disabled
- 0 = LVI module resets enabled



**Configuration Register (CONFIG)**

# Chapter 6

## Computer Operating Properly (COP)

### 6.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration 1 (CONFIG1) register.

### 6.2 Functional Description

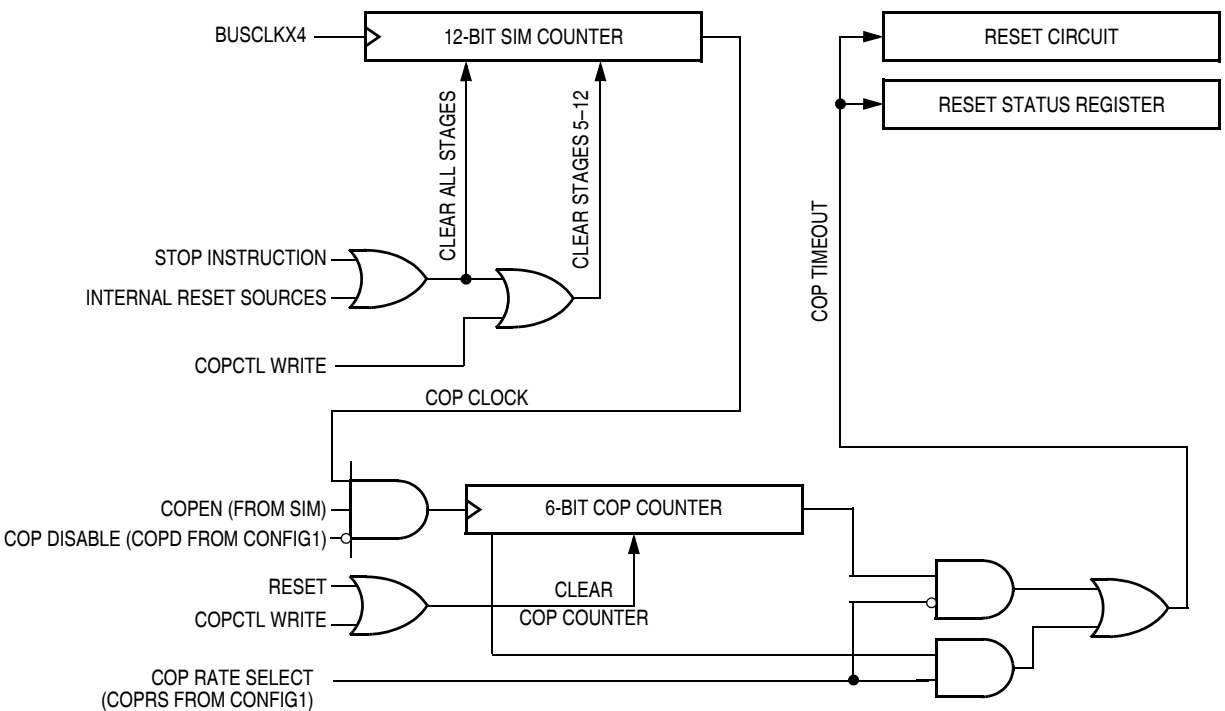


Figure 6-1. COP Block Diagram



# Chapter 11

## Oscillator Module (OSC)

### 11.1 Introduction

The oscillator module is used to provide a stable clock source for the microcontroller system and bus. The oscillator module generates two output clocks, BUSCLKX2 and BUSCLKX4. The BUSCLKX4 clock is used by the system integration module (SIM) and the computer operating properly module (COP). The BUSCLKX2 clock is divided by two in the SIM to be used as the bus clock for the microcontroller. Therefore the bus frequency will be one fourth of the BUSCLKX4 frequency.

### 11.2 Features

The oscillator has these four clock source options available:

1. Internal oscillator: An internally generated, fixed frequency clock, trimmable to  $\pm 5\%$ . This is the default option out of reset.
2. External oscillator: An external clock that can be driven directly into OSC1.
3. External RC: A built-in oscillator module (RC oscillator) that requires an external R connection only. The capacitor is internal to the chip.
4. External crystal: A built-in oscillator module (XTAL oscillator) that requires an external crystal or ceramic-resonator.

### 11.3 Functional Description

The oscillator contains these major subsystems:

- Internal oscillator circuit
- Internal or external clock switch control
- External clock circuit
- External crystal circuit
- External RC clock circuit

### 11.3.1.1 Internal Oscillator Trimming

The 8-bit trimming register, OSCTRIM, allows a clock period adjust of +127 and –128 steps. Increasing OSCTRIM value increases the clock period. Trimming allows the internal clock frequency to be set to 12.8 MHz  $\pm$  5%.

All devices are factory programmed with trim values in reserved FLASH memory locations \$FFC0 and \$FFC1. The trim value is not automatically loaded into the OSCTRIM register. User software must copy the trim value from \$FFC0 or \$FFC1 into OSCTRIM if needed. The factory trim value provides the accuracy required for communication using forced monitor mode. Some production programmers erase the factory trim values, so confirm with your programmer vendor that the trim values at \$FFC0 and \$FFC1 are preserved, or are re-trimmed. Trimming the device in the user application board will provide the most accurate trim value.

### 11.3.1.2 Internal to External Clock Switching

When external clock source (external OSC, RC, or XTAL) is desired, the user must perform the following steps:

1. For external crystal circuits only, OSCOPT[1:0] = 1:1: To help precharge an external crystal oscillator, set PTA4 (OSC2) as an output and drive high for several cycles. This may help the crystal circuit start more robustly.
2. Set CONFIG2 bits OSCOPT[1:0] according to . The oscillator module control logic will then set OSC1 as an external clock input and, if the external crystal option is selected, OSC2 will also be set as the clock output.
3. Create a software delay to wait the stabilization time needed for the selected clock source (crystal, resonator, RC) as recommended by the component manufacturer. A good rule of thumb for crystal oscillators is to wait 4096 cycles of the crystal frequency, i.e., for a 4-MHz crystal, wait approximately 1 msec.
4. After the manufacturer's recommended delay has elapsed, the ECGON bit in the OSC status register (OSCSTAT) needs to be set by the user software.
5. After ECGON set is detected, the OSC module checks for oscillator activity by waiting two external clock rising edges.
6. The OSC module then switches to the external clock. Logic provides a glitch free transition.
7. The OSC module first sets the ECGST bit in the OSCSTAT register and then stops the internal oscillator.

#### NOTE

*Once transition to the external clock is done, the internal oscillator will only be reactivated with reset. No post-switch clock monitor feature is implemented (clock does not switch back to internal if external clock dies).*

### 11.3.2 External Oscillator

The external clock option is designed for use when a clock signal is available in the application to provide a clock source to the microcontroller. The OSC1 pin is enabled as an input by the oscillator module. The clock signal is used directly to create BUSCLKX4 and also divided by two to create BUSCLKX2.

In this configuration, the OSC2 pin cannot output BUSCLKX4. So the OSC2EN bit in the port A pullup enable register will be clear to enable PTA4 I/O functions on the pin

# Chapter 13

## System Integration Module (SIM)

### 13.1 Introduction

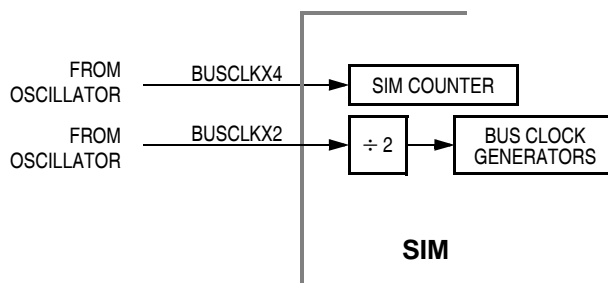
This section describes the system integration module (SIM), which supports up to 24 external and/or internal interrupts. Together with the central processor unit (CPU), the SIM controls all microcontroller unit (MCU) activities. A block diagram of the SIM is shown in [Figure 13-1](#). The SIM is a system state controller that coordinates CPU and exception timing.

The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals
  - Stop/wait/reset/break entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and computer operating properly (COP) timeout
- Interrupt control:
  - Acknowledge timing
  - Arbitration control timing
  - Vector address generation
- CPU enable/disable timing

**Table 13-1. Signal Name Conventions**

Signal Name	Description
BUSCLKX4	Buffered clock from the internal, RC or XTAL oscillator circuit.
BUSCLKX2	The BUSCLKX4 frequency divided by two. This signal is again divided by two in the SIM to generate the internal bus clocks (bus clock = $BUSCLKX4 \div 4$ ).
Address bus	Internal address bus
Data bus	Internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/ $\overline{W}$	Read/write signal



**Figure 13-2. SIM Clock Signals**

### 13.3.1 Bus Timing

In user mode, the internal bus frequency is the oscillator frequency (BUSCLKX4) divided by four.

### 13.3.2 Clock Start-Up from POR

When the power-on reset module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 BUSCLKX4 cycle POR time out has completed. The IBUS clocks start upon completion of the time out.

### 13.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt or reset, the SIM allows BUSCLKX4 to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay time out. This time out is selectable as 4096 or 32 BUSCLKX4 cycles. See [13.7.2 Stop Mode](#).

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

## 13.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ( $\overline{\text{RST}}$ )
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

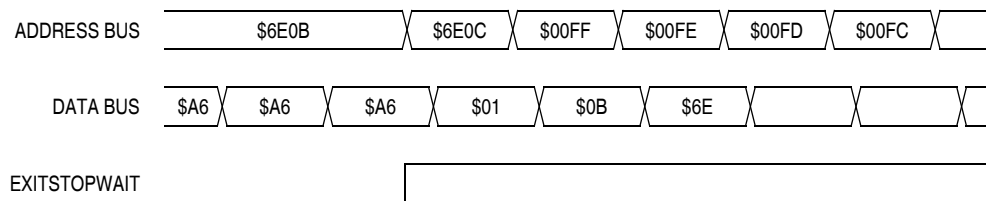
All of these resets produce the vector \$FFFE–FFFF (\$FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see [13.5 SIM Counter](#)), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See [13.8 SIM Registers](#).

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

Wait mode can also be exited by a reset (or break in emulation mode). A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the break status register (BSR). If the COP disable bit, COPD, in the configuration register is 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.

Figure 13-15 and Figure 13-16 show the timing for wait recovery.



NOTE: EXITSTOPWAIT =  $\overline{\text{RST}}$  pin OR CPU interrupt OR break interrupt

Figure 13-15. Wait Recovery from Interrupt

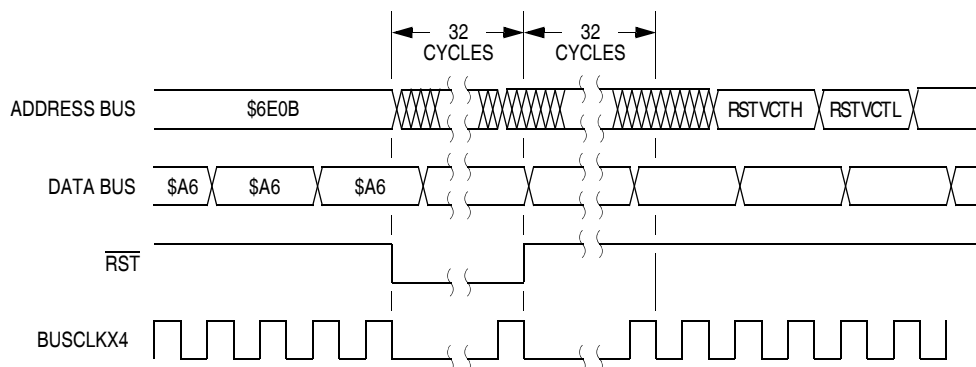


Figure 13-16. Wait Recovery from Internal Reset

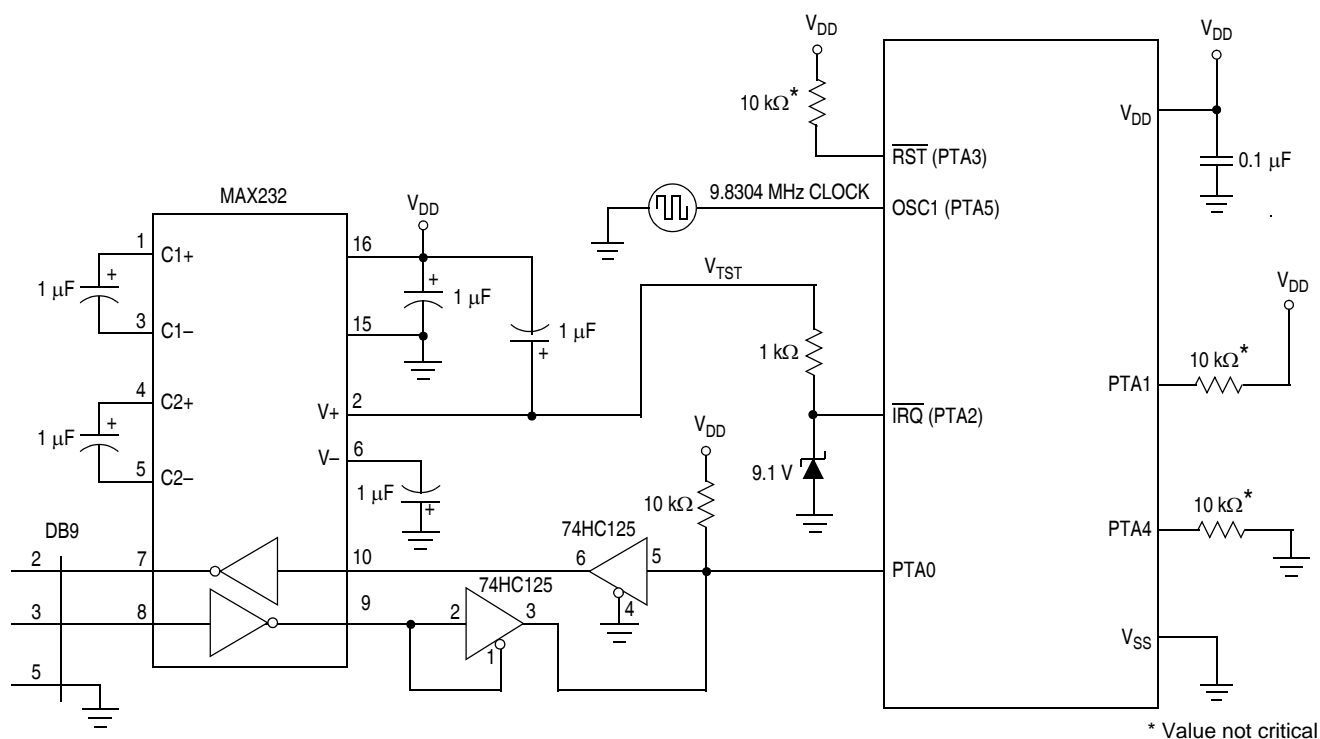
### 13.7.2 Stop Mode

In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

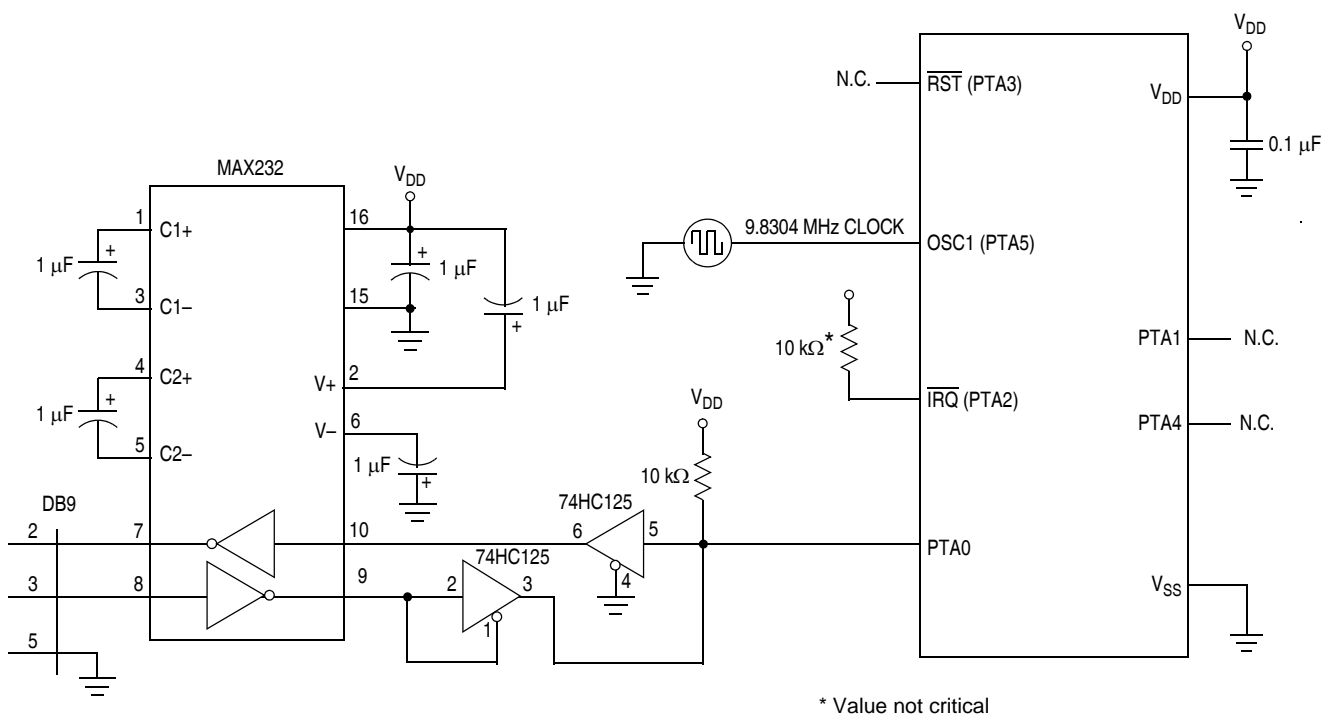
The SIM disables the oscillator signals (BUSCLKX2 and BUSCLKX4) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register 1 (CONFIG1). If SSREC is set, stop recovery is reduced from the normal delay of 4096 BUSCLKX4 cycles down to 32. This is ideal for the internal oscillator, RC oscillator, and external oscillator options which do not require long start-up times from stop mode.

#### NOTE

*External crystal applications should use the full stop recovery time by clearing the SSREC bit.*



**Figure 15-10. Monitor Mode Circuit (External Clock, with High Voltage)**



**Figure 15-11. Monitor Mode Circuit (External Clock, No High Voltage)**

## 16.5 5-V DC Electrical Characteristics

Characteristic <sup>(1)</sup>	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Output high voltage $I_{Load} = -2.0$ mA, all I/O pins $I_{Load} = -10.0$ mA, all I/O pins $I_{Load} = -15.0$ mA, PTA0, PTA1, PTA3–PTA5 only	$V_{OH}$	$V_{DD}-0.4$ $V_{DD}-1.5$ $V_{DD}-0.8$	— — —	— — —	V
Maximum combined $I_{OH}$ (all I/O pins)	$I_{OHT}$	—	—	50	mA
Output low voltage $I_{Load} = 1.6$ mA, all I/O pins $I_{Load} = 10.0$ mA, all I/O pins $I_{Load} = 15.0$ mA, PTA0, PTA1, PTA3–PTA5 only	$V_{OL}$	— — —	— — —	0.4 1.5 0.8	V
Maximum combined $I_{OL}$ (all I/O pins)	$I_{OLT}$	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	$V_{IH}$	$0.7 \times V_{DD}$	—	$V_{DD}$	V
Input low voltage PTA0–PTA5, PTB0–PTB7	$V_{IL}$	$V_{SS}$	—	$0.3 \times V_{DD}$	V
Input hysteresis	$V_{HYS}$	$0.06 \times V_{DD}$	—	—	V
DC injection current, all ports	$I_{INJ}$	–2	—	+2	mA
Total dc current injection (sum of all I/O)	$I_{INJTOT}$	–25	—	+25	mA
Ports Hi-Z leakage current	$I_{IL}$	–1	$\pm 0.1$	+1	$\mu$ A
Capacitance Ports (as input) Ports (as input)	$C_{IN}$ $C_{OUT}$	— —	— —	12 8	pF
POR rearm voltage <sup>(3)</sup>	$V_{POR}$	0	—	100	mV
POR rise time ramp rate <sup>(4)</sup>	$R_{POR}$	0.035	—	—	V/ms
Monitor mode entry voltage	$V_{TST}$	$V_{DD} + 2.5$	—	9.1	V
Pullup resistors <sup>(5)</sup> PTA0–PTA5, PTB0–PTB7	$R_{PU}$	16	26	36	k $\Omega$
Low-voltage inhibit reset, trip falling voltage	$V_{TRIPF}$	3.90	4.20	4.50	V
Low-voltage inhibit reset, trip rising voltage	$V_{TRIPR}$	4.00	4.30	4.60	V
Low-voltage inhibit reset/recover hysteresis	$V_{HYS}$	—	100	—	mV

1.  $V_{DD} = 4.5$  to  $5.5$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ , unless otherwise noted.

2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.

3. Maximum is highest voltage that POR is guaranteed.

4. If minimum  $V_{DD}$  is not reached before the internal POR reset is released, the LVI will hold the part in reset until minimum  $V_{DD}$  is reached.

5.  $R_{PU}$  is measured at  $V_{DD} = 5.0$  V.

# 16.11 3-V Control Timing

Characteristic <sup>(1)</sup>	Symbol	Min	Max	Unit
Internal operating frequency	$f_{OP} (f_{Bus})$	—	4	MHz
Internal clock period ( $1/f_{OP}$ )	$t_{cyc}$	250	—	ns
$\overline{RST}$ input pulse width low	$t_{RL}$	200	—	ns
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	$t_{ILIH}$	200	—	ns
$\overline{IRQ}$ interrupt pulse period	$t_{ILIL}$	Note <sup>(2)</sup>	—	$t_{cyc}$

- $V_{DD} = 2.7$  to  $3.3$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ ; timing shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.
- The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1  $t_{cyc}$ .

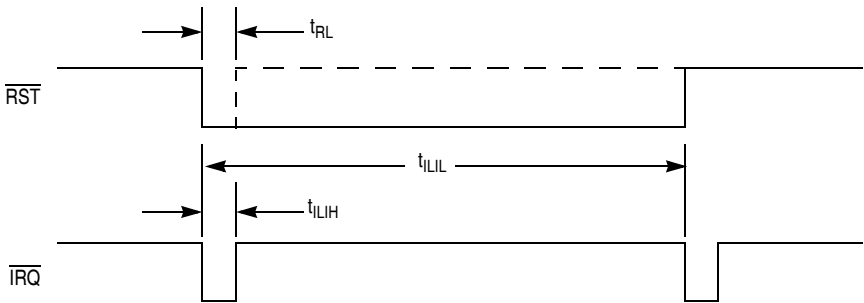


Figure 16-7.  $\overline{RST}$  and  $\overline{IRQ}$  Timing



## 16.12 3-V Oscillator Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator frequency <sup>(1)</sup>	$f_{\text{INTCLK}}$	—	12.8	—	MHz
Deviation from trimmed Internal oscillator <sup>(2)(3)</sup> 12.8 MHz, fixed voltage, fixed temp 12.8 MHz, $V_{\text{DD}} \pm 10\%$ , 0 to 70°C 12.8 MHz, $V_{\text{DD}} \pm 10\%$ , -40 to 125°C	$\text{ACC}_{\text{INT}}$	— — —	$\pm 0.4$ $\pm 2$ —	— — $\pm 5$	%
Crystal frequency, XTALCLK <sup>(1)</sup>	$f_{\text{OSCCLK}}$	1	—	16	MHz
External RC oscillator frequency, RCCLK <sup>(1)</sup>	$f_{\text{RCCLK}}$	2	—	10	MHz
External clock reference frequency <sup>(1) (4)</sup>	$f_{\text{OSCCLK}}$	dc	—	16	MHz
Crystal load capacitance <sup>(5)</sup>	$C_L$	—	20	—	pF
Crystal fixed capacitance <sup>(3)</sup>	$C_1$	—	$2 \times C_L$	—	—
Crystal tuning capacitance <sup>(3)</sup>	$C_2$	—	$2 \times C_L$	—	—
Feedback bias resistor	$R_B$	0.5	1	10	MΩ
RC oscillator external resistor	$R_{\text{EXT}}$	See Figure 16-8			—
Crystal series damping resistor $f_{\text{OSCCLK}} = 1 \text{ MHz}$ $f_{\text{OSCCLK}} = 4 \text{ MHz}$ $f_{\text{OSCCLK}} = > 8 \text{ MHz}$	$R_S$	— — —	10 5 0	— — —	kΩ

1. Bus frequency,  $f_{\text{OP}}$ , is oscillator frequency divided by 4.
2. Deviation values assumes trimming @25°C and midpoint of voltage range.
3. Values are based on characterization results, not tested in production.
4. No more than 10% duty cycle deviation from 50%
5. Consult crystal vendor data sheet

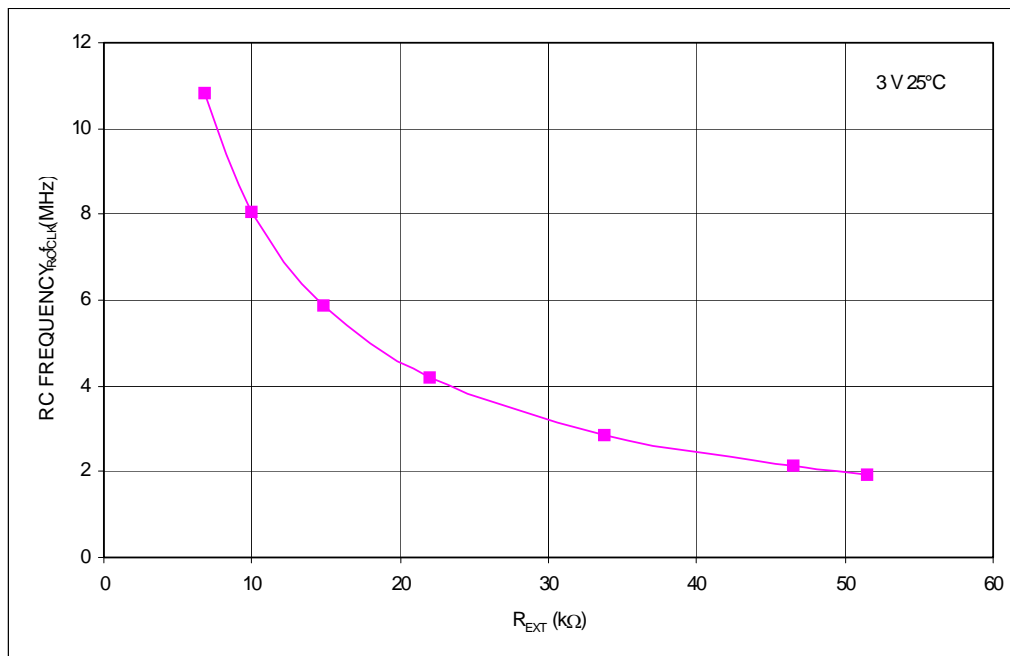
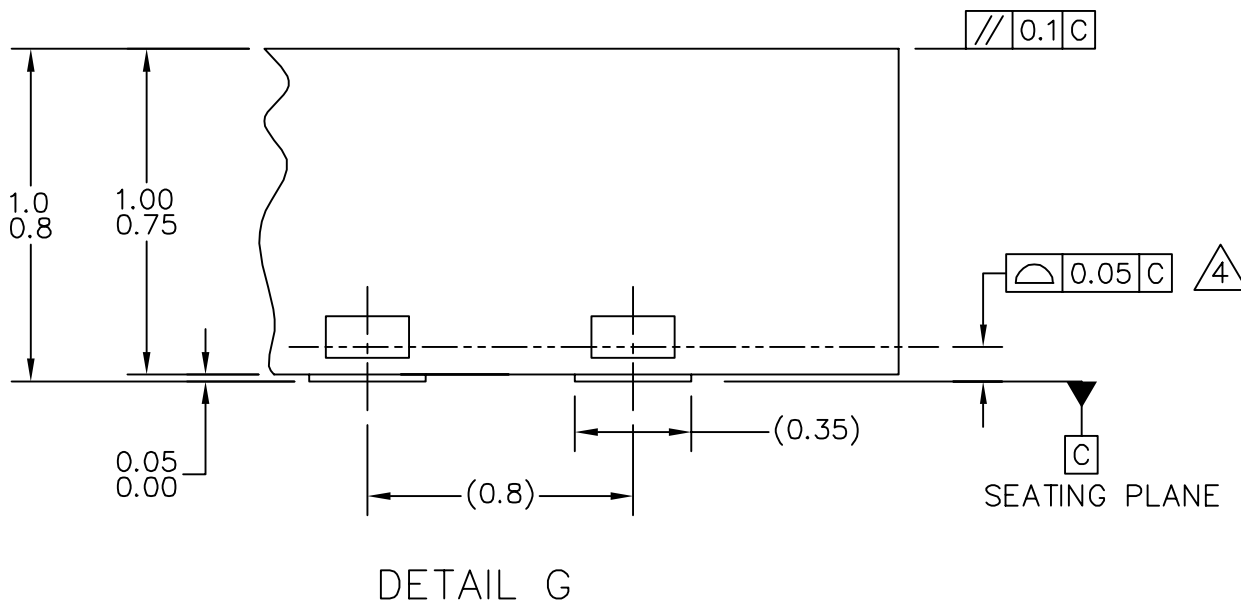


Figure 16-8. RC versus Frequency (3 Volts @ 25°C)



SHEET: 2 OF 5



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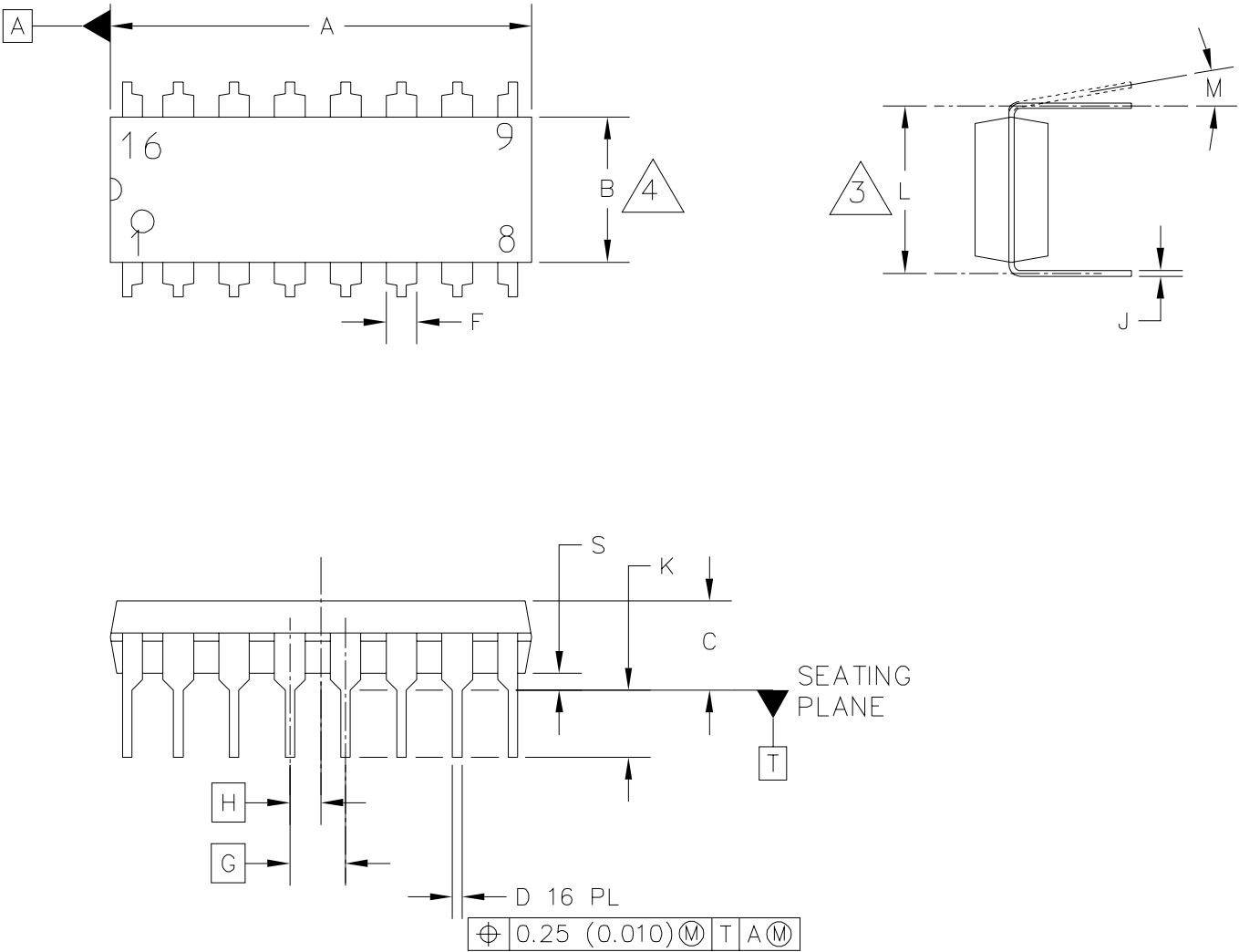
TITLE:THERMALLY ENHANCED DUAL  
FLAT NO LEAD PACKAGE (DFN)  
8 TERMINAL, 0.8 PITCH(4 X 4 X 1)

CASE NUMBER: 1452-01

STANDARD: NON-JEDEC

PACKAGE CODE: 6165

SHEET: 4 OF 5



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