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Details

Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchc908qy4mdwer



Chapter 1

General Description

1.1 Introduction

The MC68HC908QY4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	FLASH Memory Size	Analog-to-Digital Converter	Pin Count
MC68HC908QT1	1536 bytes	—	8 pins
MC68HC908QT2	1536 bytes	4 ch, 8 bit	8 pins
MC68HC908QT4	4096 bytes	4 ch, 8 bit	8 pins
MC68HC908QY1	1536 bytes	—	16 pins
MC68HC908QY2	1536 bytes	4 ch, 8 bit	16 pins
MC68HC908QY4	4096 bytes	4 ch, 8 bit	16 pins

1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- 5-V and 3-V operating voltages (V_{DD})
- 8-MHz internal bus operation at 5 V, 4-MHz at 3 V
- Trimmable internal oscillator
 - 3.2 MHz internal bus operation
 - 8-bit trim capability allows 0.4% accuracy⁽¹⁾
 - $\pm 25\%$ untrimmed
- Auto wakeup from STOP capability
- Configuration (CONFIG) register for MCU configuration options, including:
 - Low-voltage inhibit (LVI) trip point
- In-system FLASH programming
- FLASH security⁽²⁾

1. The oscillator frequency is guaranteed to $\pm 5\%$ over temperature and voltage range after trimming.

2. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

1.6 Pin Function Priority

Table 1-3 is meant to resolve the priority if multiple functions are enabled on a single pin.

NOTE

Upon reset all pins come up as input ports regardless of the priority table.

Table 1-3. Function Priority in Shared Pins

Pin Name	Highest-to-Lowest Priority Sequence
PTA0	AD0 → TCH0 → KBI0 → PTA0
PTA1	AD1 → TCH1 → KBI1 → PTA1
PTA2	$\overline{\text{IRQ}}$ → KBI2 → TCLK → PTA2
PTA3	$\overline{\text{RST}}$ → KBI3 → PTA3
PTA4	OSC2 → AD2 → KBI4 → PTA4
PTA5	OSC1 → AD3 → KBI5 → PTA5

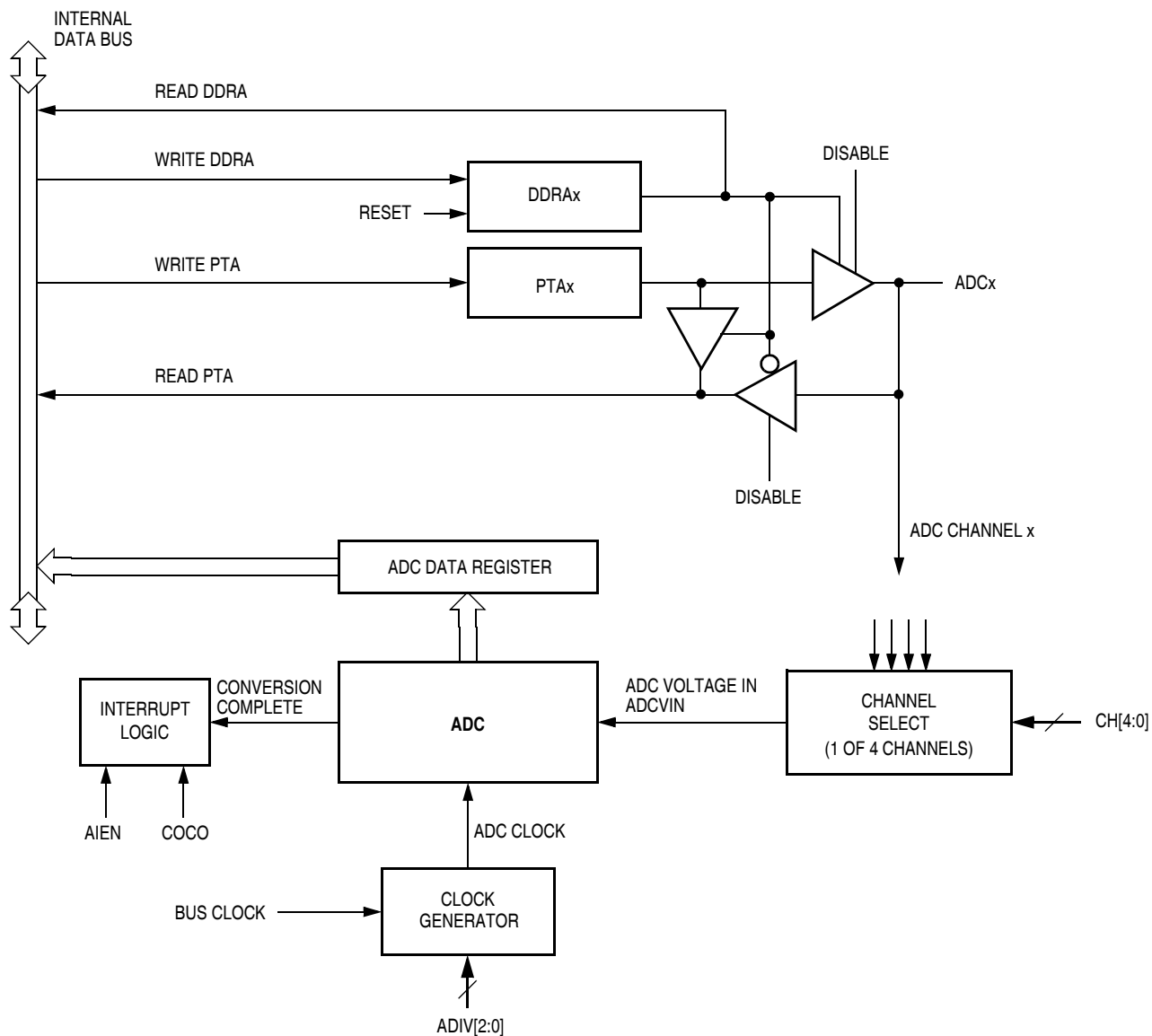


Figure 3-2. ADC Block Diagram

Configuration Register (CONFIG)

IRQPUD — $\overline{\text{IRQ}}$ Pin Pullup Control Bit

- 1 = Internal pullup is disconnected
- 0 = Internal pullup is connected between $\overline{\text{IRQ}}$ pin and V_{DD}

IRQEN — $\overline{\text{IRQ}}$ Pin Function Selection Bit

- 1 = Interrupt request function active in pin
- 0 = Interrupt request function inactive in pin

OSCOPT1 and OSCOPT0 — Selection Bits for Oscillator Option

- (0, 0) Internal oscillator
- (0, 1) External oscillator
- (1, 0) External RC oscillator
- (1, 1) External XTAL oscillator

RSTEN — $\overline{\text{RST}}$ Pin Function Selection

- 1 = Reset function active in pin
- 0 = Reset function inactive in pin

NOTE

The RSTEN bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.

Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVI PWRD	LVI5OR3	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

U = Unaffected

Figure 5-2. Configuration Register 1 (CONFIG1)

COPRS (Out of STOP Mode) — COP Reset Period Selection Bit

- 1 = COP reset short cycle = $8176 \times \text{BUSCLKX4}$
- 0 = COP reset long cycle = $262,128 \times \text{BUSCLKX4}$

COPRS (In STOP Mode) — Auto Wakeup Period Selection Bit

- 1 = Auto wakeup short cycle = $512 \times \text{INTRCOSC}$
- 0 = Auto wakeup long cycle = $16,384 \times \text{INTRCOSC}$

LVISTOP — LVI Enable in Stop Mode Bit

When the LVI PWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

- 1 = LVI enabled during stop mode
- 0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable Bit

LVIRSTD disables the reset signal from the LVI module.

- 1 = LVI module resets disabled
- 0 = LVI module resets enabled

Z — Zero Flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of \$00.

1 = Zero result

0 = Non-zero result

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7

0 = No carry out of bit 7

7.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

7.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

7.5.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

7.5.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

7.6 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC:\$FFFD or with \$FEFC:\$FEFD in monitor mode

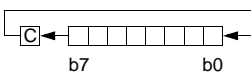
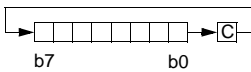
The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

Table 7-1. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BHS <i>rel</i>	Branch if Higher or Same (Same as BCC)	$PC \leftarrow (PC) + 2 + rel ? (C) = 0$	–	–	–	–	–	REL	24	rr	3	
BIH <i>rel</i>	Branch if \overline{IRQ} Pin High	$PC \leftarrow (PC) + 2 + rel ? \overline{IRQ} = 1$	–	–	–	–	–	REL	2F	rr	3	
BIL <i>rel</i>	Branch if \overline{IRQ} Pin Low	$PC \leftarrow (PC) + 2 + rel ? \overline{IRQ} = 0$	–	–	–	–	–	REL	2E	rr	3	
BIT # <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> ,X BIT <i>opr</i> ,X BIT .X BIT <i>opr</i> ,SP BIT <i>opr</i> ,SP	Bit Test	(A) & (M)	0	–	–	↑	↑	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE <i>opr</i>	Branch if Less Than or Equal To (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (Z) (N \oplus V) = 1$	–	–	–	–	–	REL	93	rr	3	
BLO <i>rel</i>	Branch if Lower (Same as BCS)	$PC \leftarrow (PC) + 2 + rel ? (C) = 1$	–	–	–	–	–	REL	25	rr	3	
BLS <i>rel</i>	Branch if Lower or Same	$PC \leftarrow (PC) + 2 + rel ? (C) (Z) = 1$	–	–	–	–	–	REL	23	rr	3	
BLT <i>opr</i>	Branch if Less Than (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (N \oplus V) = 1$	–	–	–	–	–	REL	91	rr	3	
BMC <i>rel</i>	Branch if Interrupt Mask Clear	$PC \leftarrow (PC) + 2 + rel ? (I) = 0$	–	–	–	–	–	REL	2C	rr	3	
BMI <i>rel</i>	Branch if Minus	$PC \leftarrow (PC) + 2 + rel ? (N) = 1$	–	–	–	–	–	REL	2B	rr	3	
BMS <i>rel</i>	Branch if Interrupt Mask Set	$PC \leftarrow (PC) + 2 + rel ? (I) = 1$	–	–	–	–	–	REL	2D	rr	3	
BNE <i>rel</i>	Branch if Not Equal	$PC \leftarrow (PC) + 2 + rel ? (Z) = 0$	–	–	–	–	–	REL	26	rr	3	
BPL <i>rel</i>	Branch if Plus	$PC \leftarrow (PC) + 2 + rel ? (N) = 0$	–	–	–	–	–	REL	2A	rr	3	
BRA <i>rel</i>	Branch Always	$PC \leftarrow (PC) + 2 + rel$	–	–	–	–	–	REL	20	rr	3	
BRCLR <i>n,opr,rel</i>	Branch if Bit <i>n</i> in M Clear	$PC \leftarrow (PC) + 3 + rel ? (Mn) = 0$	–	–	–	–	–	↑	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN <i>rel</i>	Branch Never	$PC \leftarrow (PC) + 2$	–	–	–	–	–	REL	21	rr	3	
BRSET <i>n,opr,rel</i>	Branch if Bit <i>n</i> in M Set	$PC \leftarrow (PC) + 3 + rel ? (Mn) = 1$	–	–	–	–	–	↑	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET <i>n,opr</i>	Set Bit <i>n</i> in M	$Mn \leftarrow 1$	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR <i>rel</i>	Branch to Subroutine	$PC \leftarrow (PC) + 2$; push (PCL) $SP \leftarrow (SP) - 1$; push (PCH) $SP \leftarrow (SP) - 1$ $PC \leftarrow (PC) + rel$	–	–	–	–	–	REL	AD	rr	4	
CBEQ <i>opr,rel</i> CBEQA # <i>opr,rel</i> CBEQX # <i>opr,rel</i> CBEQ <i>opr,X+,rel</i> CBEQ <i>X+,rel</i> CBEQ <i>opr,SP,rel</i>	Compare and Branch if Equal	$PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \00 $PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \00 $PC \leftarrow (PC) + 3 + rel ? (X) - (M) = \00 $PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \00 $PC \leftarrow (PC) + 2 + rel ? (A) - (M) = \00 $PC \leftarrow (PC) + 4 + rel ? (A) - (M) = \00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	$C \leftarrow 0$	–	–	–	–	–	0	INH	98		1

Table 7-1. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z	C					
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	INH	86			2	
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	INH	8A			2	
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	INH	88			2	
ROL <i>opr</i> ROLA ROLX ROL <i>opr</i> ,X ROL ,X ROL <i>opr</i> ,SP	Rotate Left through Carry		↑	–	–	↑	↑	↑	DIR INH INH IX1 IX SP1 9E69	39 49 59 69 79 ff	dd ff	4 1 1 4 3 5	
ROR <i>opr</i> RORA RORX ROR <i>opr</i> ,X ROR ,X ROR <i>opr</i> ,SP	Rotate Right through Carry		↑	–	–	↑	↑	↑	DIR INH INH IX1 IX SP1 9E66	36 46 56 66 76 ff	dd ff	4 1 1 4 3 5	
RSP	Reset Stack Pointer	SP ← \$FF	–	–	–	–	–	INH	9C			1	
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↑	↑	↑	↑	↑	↑	INH	80			7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	INH	81				4
SBC # <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> ,X SBC <i>opr</i> ,X SBC ,X SBC <i>opr</i> ,SP SBC <i>opr</i> ,SP	Subtract with Carry	A ← (A) – (M) – (C)	↑	–	–	↑	↑	↑	IMM DIR EXT IX2 D2 IX1 E2 IX F2 SP1 SP2 9EE2 9ED2	A2 B2 C2 D2 E2 F2 9EE2 9ED2 ff	ii dd hh ll ee ff ff ff ff ff ff	2 3 4 4 3 2 4 4 5	
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99			1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B			2
STA <i>opr</i> STA <i>opr</i> STA <i>opr</i> ,X STA <i>opr</i> ,X STA ,X STA <i>opr</i> ,SP STA <i>opr</i> ,SP	Store A in M	M ← (A)	0	–	–	↑	↑	–	DIR EXT IX2 D7 IX1 E7 IX F7 SP1 SP2 9EE7 9ED7	B7 C7 D7 E7 F7 9EE7 9ED7 ff	dd hh ll ee ff ff ff ff ff ff	3 4 4 3 2 4 4 5	
STHX <i>opr</i>	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↑	↑	–	DIR	35	dd		4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	I ← 0; Stop Processing	–	–	0	–	–	–	INH	8E			1
STX <i>opr</i> STX <i>opr</i> STX <i>opr</i> ,X STX <i>opr</i> ,X STX ,X STX <i>opr</i> ,SP STX <i>opr</i> ,SP	Store X in M	M ← (X)	0	–	–	↑	↑	–	DIR EXT IX2 IX1 IX SP1 SP2 9EEF 9EDF	BF CF DF EF FF 9EEF 9EDF ff	dd hh ll ee ff ff ff ff ff ff	3 4 4 3 2 4 4 5	
SUB # <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> ,X SUB <i>opr</i> ,X SUB ,X SUB <i>opr</i> ,SP SUB <i>opr</i> ,SP	Subtract	A ← (A) – (M)	↑	–	–	↑	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2 9EE0 9ED0	A0 B0 C0 D0 E0 F0 9EE0 9ED0 ff	ii dd hh ll ee ff ff ff ff ff ff	2 3 4 4 3 2 4 4 5	

To protect the latch during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect.

9.7 Input/Output Registers

The following I/O registers control and monitor operation of the keyboard interrupt module:

- Keyboard interrupt status and control register (KBSCR)
- Keyboard interrupt enable register (KBIER)

9.7.1 Keyboard Status and Control Register

The keyboard status and control register (KBSCR):

- Flags keyboard interrupt requests
- Acknowledges keyboard interrupt requests
- Masks keyboard interrupt requests
- Controls keyboard interrupt triggering sensitivity

Address: \$001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:						ACKK		
Reset:	0	0	0	0	0	0	0	0


 = Unimplemented

Figure 9-3. Keyboard Status and Control Register (KBSCR)

Bits 7–4 — Not used

These read-only bits always read as 0s.

KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending on port A or auto wakeup. Reset clears the KEYF bit.

- 1 = Keyboard interrupt pending
- 0 = No keyboard interrupt pending

ACKK — Keyboard Acknowledge Bit

Writing a 1 to this write-only bit clears the keyboard interrupt request on port A and auto wakeup logic. ACKK always reads as 0. Reset clears ACKK.

IMASKK— Keyboard Interrupt Mask Bit

Writing a 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests on port A or auto wakeup. Reset clears the IMASKK bit.

- 1 = Keyboard interrupt requests masked
- 0 = Keyboard interrupt requests not masked

MODEK — Keyboard Triggering Sensitivity Bit

This read/write bit controls the triggering sensitivity of the keyboard interrupt pins on port A and auto wakeup. Reset clears MODEK.

- 1 = Keyboard interrupt requests on falling edges and low levels
- 0 = Keyboard interrupt requests on falling edges only

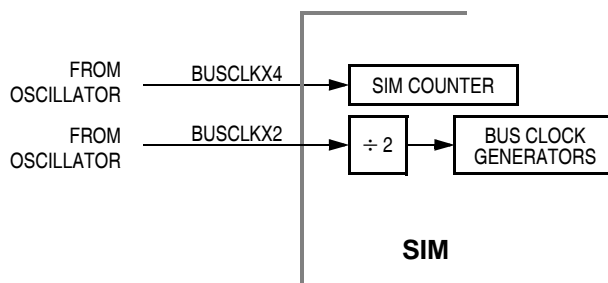


Figure 13-2. SIM Clock Signals

13.3.1 Bus Timing

In user mode, the internal bus frequency is the oscillator frequency (BUSCLKX4) divided by four.

13.3.2 Clock Start-Up from POR

When the power-on reset module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 BUSCLKX4 cycle POR time out has completed. The IBUS clocks start upon completion of the time out.

13.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt or reset, the SIM allows BUSCLKX4 to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay time out. This time out is selectable as 4096 or 32 BUSCLKX4 cycles. See [13.7.2 Stop Mode](#).

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

13.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector \$FFFE–FFFF (\$FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see [13.5 SIM Counter](#)), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See [13.8 SIM Registers](#).

TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from \$0000. TRST is cleared automatically after the TIM counter is reset and always reads as a 0. Reset clears the TRST bit.

- 1 = Prescaler and TIM counter cleared
- 0 = No effect

NOTE

Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of \$0000.

PS[2:0] — Prescaler Select Bits

These read/write bits select either the PTA2/TCLK pin or one of the seven prescaler outputs as the input to the TIM counter as [Table 14-2](#) shows. Reset clears the PS[2:0] bits.

Table 14-2. Prescaler Selection

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal bus clock ÷ 1
0	0	1	Internal bus clock ÷ 2
0	1	0	Internal bus clock ÷ 4
0	1	1	Internal bus clock ÷ 8
1	0	0	Internal bus clock ÷ 16
1	0	1	Internal bus clock ÷ 32
1	1	0	Internal bus clock ÷ 64
1	1	1	PTA2/TCLK

14.9.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

NOTE

If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.

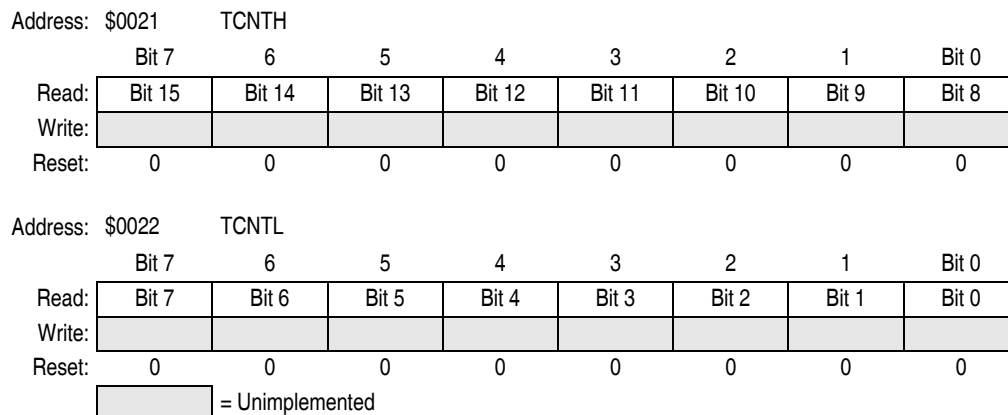


Figure 14-5. TIM Counter Registers (TCNTH:TCNTL)

Table 15-1. Monitor Mode Signal Requirements and Options

Mode	$\overline{\text{IRQ}}$ (PTA2)	$\overline{\text{RST}}$ (PTA3)	Reset Vector	Serial Communication	Mode Selection		COP	Communication Speed			Comments
				PTA0	PTA1	PTA4		External Clock	Bus Frequency	Baud Rate	
Normal Monitor	V_{TST}	V_{DD}	X	1	1	0	Disabled	9.8304 MHz	2.4576 MHz	9600	Provide external clock at OSC1.
Forced Monitor	V_{DD}	X	\$FFFF (blank)	1	X	X	Disabled	9.8304 MHz	2.4576 MHz	9600	Provide external clock at OSC1.
	V_{SS}	X	\$FFFF (blank)	1	X	X	Disabled	X	3.2 MHz (Trimmed)	9600	Internal clock is active.
User	X	X	Not \$FFFF	X	X	X	Enabled	X	X	X	
MON08 Function [Pin No.]	V_{TST} [6]	$\overline{\text{RST}}$ [4]	—	COM [8]	MOD0 [12]	MOD1 [10]	—	OSC1 [13]	—	—	

1. PTA0 must have a pullup resistor to V_{DD} in monitor mode.
2. Communication speed in the table is an example to obtain a baud rate of 9600. Baud rate using external oscillator is bus frequency / 256 and baud rate using internal oscillator is bus frequency / 335.
3. External clock is a 9.8304 MHz oscillator on OSC1.
4. X = don't care
5. MON08 pin refers to P&E Microcomputer Systems' MON08-Cyclone 2 by 8-pin connector.

NC	1	2	GND
NC	3	4	$\overline{\text{RST}}$
NC	5	6	$\overline{\text{IRQ}}$
NC	7	8	PTA0
NC	9	10	PTA4
NC	11	12	PTA1
OSC1	13	14	NC
V_{DD}	15	16	NC

The rising edge of the internal $\overline{\text{RST}}$ signal latches the monitor mode. Once monitor mode is latched, the values on PTA1 and PTA4 pins can be changed.

Once out of reset, the MCU waits for the host to send eight security bytes (see [15.3.2 Security](#)). After the security bytes, the MCU sends a break signal (10 consecutive logic 0s) to the host, indicating that it is ready to receive a command.

15.3.1.1 Normal Monitor Mode

$\overline{\text{RST}}$ and OSC1 functions will be active on the PTA3 and PTA5 pins respectively as long as V_{TST} is applied to the $\overline{\text{IRQ}}$ pin. If the $\overline{\text{IRQ}}$ pin is lowered (no longer V_{TST}) then the chip will still be operating in monitor mode, but the pin functions will be determined by the settings in the configuration registers (see [Chapter 5 Configuration Register \(CONFIG\)](#)) when V_{TST} was lowered. With V_{TST} lowered, the BIH and BIL instructions will read the $\overline{\text{IRQ}}$ pin state only if IRQEN is set in the CONFIG2 register.

Table 15-4. WRITE (Write Memory) Command

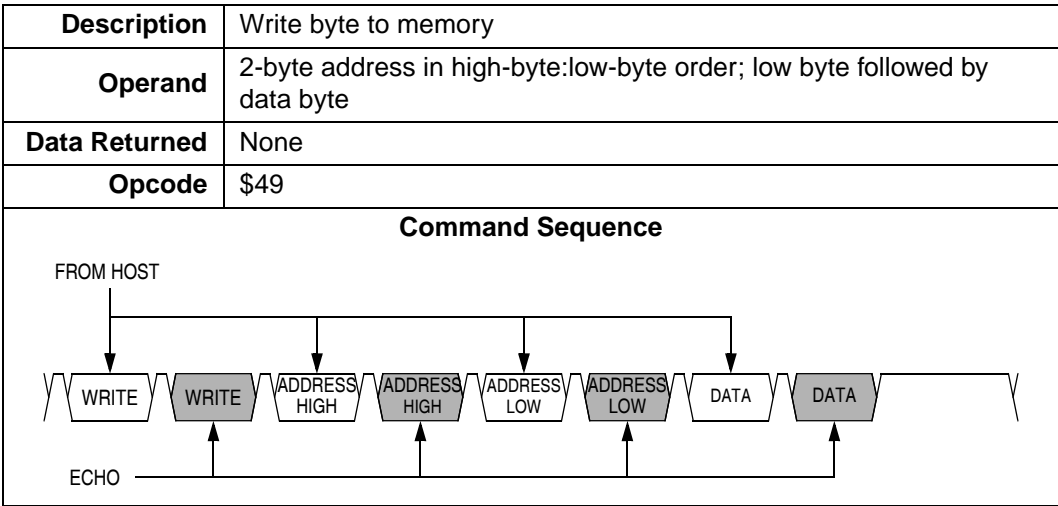


Table 15-5. IREAD (Indexed Read) Command

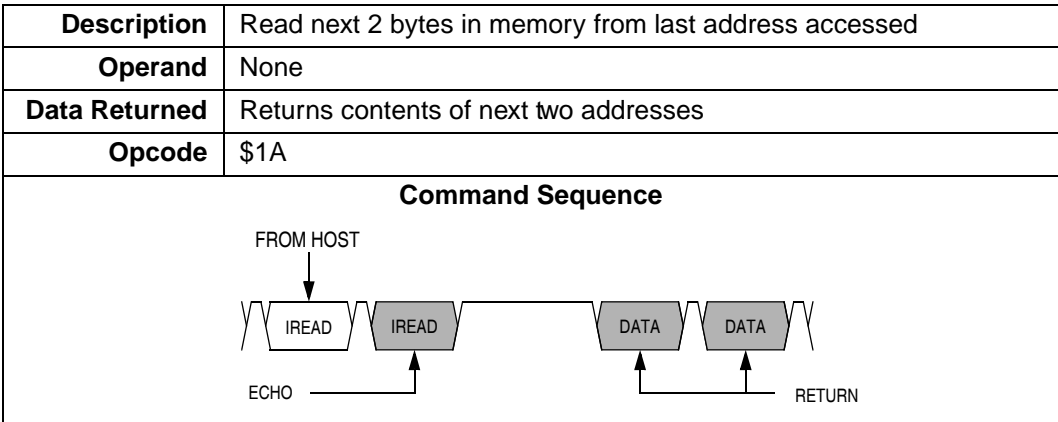
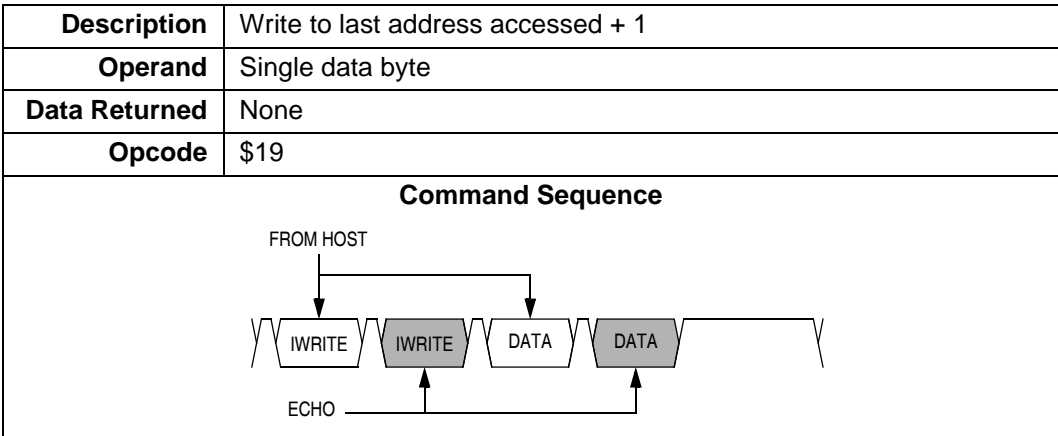


Table 15-6. IWRITE (Indexed Write) Command



A sequence of IREAD or IWRITE commands can access a block of memory sequentially over the full 64-Kbyte memory map.

Chapter 16

Electrical Specifications

16.1 Introduction

This section contains electrical and timing specifications.

16.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to [16.5 5-V DC Electrical Characteristics](#) and [16.9 3-V DC Electrical Characteristics](#) for guaranteed operating conditions.

Characteristic ⁽¹⁾	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to +6.0	V
Input voltage	V_{IN}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Mode entry voltage, \overline{IRQ} pin	V_{TST}	$V_{SS} - 0.3$ to +9.1	V
Maximum current per pin excluding PTA0–PTA5, V_{DD} , and V_{SS}	I	±15	mA
Maximum current for pins PTA0–PTA5	$I_{PTA0} - I_{PTA5}$	±25	mA
Storage temperature	T_{STG}	-55 to +150	°C
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA

1. Voltages references to V_{SS} .

NOTE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD} .)

16.8 5-V Oscillator Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator frequency ⁽¹⁾	f_{INTCLK}	—	12.8	—	MHz
Deviation from trimmed Internal oscillator ⁽²⁾⁽³⁾ 12.8 MHz, fixed voltage, fixed temp 12.8 MHz, $V_{\text{DD}} \pm 10\%$, 0 to 70°C 12.8 MHz, $V_{\text{DD}} \pm 10\%$, -40 to 125°C	ACC_{INT}	— — —	± 0.4 ± 2 —	— — ± 5	%
Crystal frequency, XTALCLK ⁽¹⁾	f_{OSCCLK}	1	—	24	MHz
External RC oscillator frequency, RCCLK ⁽¹⁾	f_{RCCLK}	2	—	12	MHz
External clock reference frequency ^{(1) (4)}	f_{OSCCLK}	dc	—	32	MHz
Crystal load capacitance ⁽⁵⁾	C_L	—	20	—	pF
Crystal fixed capacitance ⁽³⁾	C_1	—	$2 \times C_L$	—	—
Crystal tuning capacitance ⁽³⁾	C_2	—	$2 \times C_L$	—	—
Feedback bias resistor	R_B	0.5	1	10	MΩ
RC oscillator external resistor	R_{EXT}	See Figure 16-4			—
Crystal series damping resistor $f_{\text{OSCCLK}} = 1 \text{ MHz}$ $f_{\text{OSCCLK}} = 4 \text{ MHz}$ $f_{\text{OSCCLK}} = > 8 \text{ MHz}$	R_S	— — —	20 10 0	— — —	kΩ

1. Bus frequency, f_{OP} , is oscillator frequency divided by 4.
2. Deviation values assumes trimming @25°C and midpoint of voltage range.
3. Values are based on characterization results, not tested in production.
4. No more than 10% duty cycle deviation from 50%.
5. Consult crystal vendor data sheet.

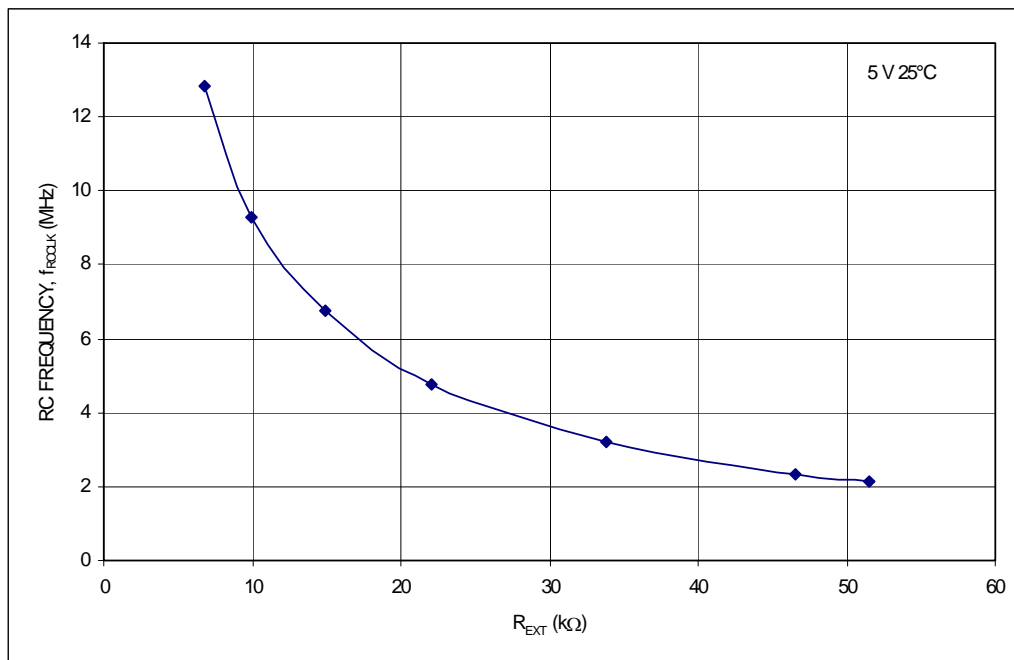


Figure 16-4. RC versus Frequency (5 Volts @ 25°C)

16.11 3-V Control Timing

Characteristic ⁽¹⁾	Symbol	Min	Max	Unit
Internal operating frequency	$f_{OP} (f_{Bus})$	—	4	MHz
Internal clock period ($1/f_{OP}$)	t_{cyc}	250	—	ns
\overline{RST} input pulse width low	t_{RL}	200	—	ns
\overline{IRQ} interrupt pulse width low (edge-triggered)	t_{ILIH}	200	—	ns
\overline{IRQ} interrupt pulse period	t_{ILIL}	Note ⁽²⁾	—	t_{cyc}

- $V_{DD} = 2.7$ to 3.3 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H ; timing shown with respect to 20% V_{DD} and 70% V_{DD} , unless otherwise noted.
- The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{cyc} .

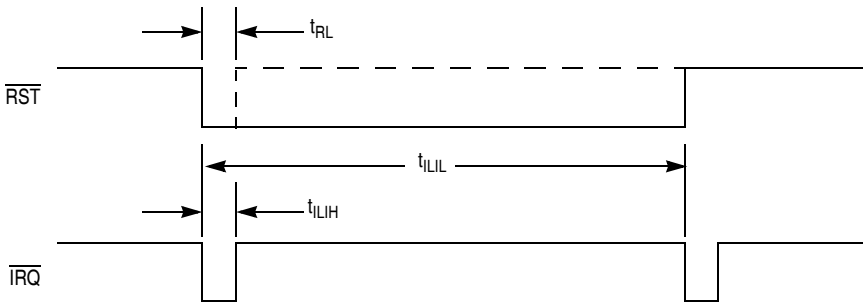


Figure 16-7. \overline{RST} and \overline{IRQ} Timing

16.16 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH read bus clock frequency	$f_{Read}^{(1)}$	0	—	8 M	Hz
FLASH page erase time <1 k cycles >1 k cycles	t_{Erase}	0.9 3.6	1 4	1.1 5.5	ms
FLASH mass erase time	t_{MErase}	4	—	—	ms
FLASH PGM/ERASE to HVEN setup time	t_{NVS}	10	—	—	μ s
FLASH high-voltage hold time	t_{NVH}	5	—	—	μ s
FLASH high-voltage hold time (mass erase)	t_{NVHL}	100	—	—	μ s
FLASH program hold time	t_{PGS}	5	—	—	μ s
FLASH program time	t_{PROG}	30	—	40	μ s
FLASH return to read time	$t_{RCV}^{(2)}$	1	—	—	μ s
FLASH cumulative program HV period	$t_{HV}^{(3)}$	—	—	4	ms
FLASH endurance ⁽⁴⁾	—	10 k	100 k	—	Cycles
FLASH data retention time ⁽⁵⁾	—	15	100	—	Years

1. f_{Read} is defined as the frequency range for which the FLASH memory can be read.

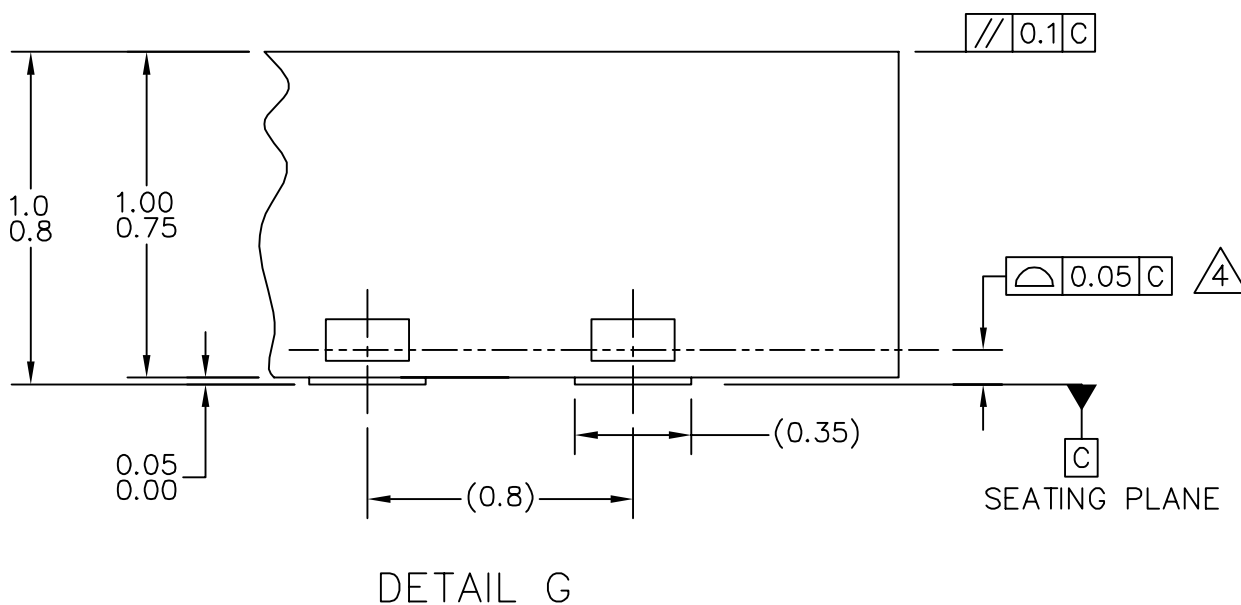
2. t_{RCV} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to 0.

3. t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase.

t_{HV} must satisfy this condition: $t_{NVS} + t_{NVH} + t_{PGS} + (t_{PROG} \times 32) \leq t_{HV}$ maximum.

4. Typical endurance was evaluated for this product family. For additional information on how Freescale defines *Typical Endurance*, please refer to Engineering Bulletin EB619.

5. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines *Typical Data Retention*, please refer to Engineering Bulletin EB618.





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MECHANICAL OUTLINES
DICTIONARY

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DO NOT SCALE THIS DRAWING

REV: B

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE
BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF
THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

TITLE:

16 LD TSSOP, PITCH 0.65MM

CASE NUMBER: 948F-01

STANDARD: JEDEC

PACKAGE CODE: 6117

SHEET: 3 OF 4

