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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 7x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	80-PQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc836bsz

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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ADuC836 SPECIFICATIONS (continued)

Parameter	ADuC836	Test Conditions/Comments	Unit
INTERNAL REFERENCE			
ADC Reference			
Reference Voltage	$1.25 \pm 1\%$	Initial Tolerance @ 25° C, V _{DD} = 5 V	V min/max
Power Supply Rejection	45		dBs typ
Reference Tempco	100		ppm/°C typ
DAC Reference	0.5.1.10/		TT • /
Reference Voltage	$2.5 \pm 1\%$	Initial Tolerance (a) 25° C, $V_{DD} = 5^{\circ}$ V	V min/max
Power Supply Rejection	50		dBs typ
Reference Tempco	±100		ppm/°C typ
ANALOG INPUTS/REFERENCE INPUTS			
Primary ADC			
Differential Input Voltage Ranges ^{3, 10}		External Reference Voltage = 2.5 V	
$\mathbf{D}_{\mathbf{n}}^{\prime}$	+20	RN2, RN1, RN0 of ADCUCUN Set to	
Bipolar Mode (ADC0CON3 $= 0$)	± 20	0.0.1 (Unipolar Mode 0 mV to 20 mV)	mV mV
	+90	0.1.0 (Unipolar Mode 0 mV to 80 mV)	mV
	± 160	0.1.1 (Unipolar Mode 0 mV to 160 mV)	mV
	+320	1.0.0 (Unipolar Mode 0 mV to 320 mV)	mV
	+640	1.0.1 (Unipolar Mode 0 mV to 640 mV)	mV
	±1.28	1 1 0 (Unipolar Mode 0 V to 1.28V)	V
	±2.56	1 1 1 (Unipolar Mode 0 V to 2.56 V)	V
Analog Input Current ²	±1	$T_{MAX} = 85^{\circ}C$	nA max
	±5	$T_{MAX} = 125^{\circ}C$	nA max
Analog Input Current Drift	±5	$T_{MAX} = 85^{\circ}C$	pA/°C typ
	±15	$T_{MAX} = 125^{\circ}C$	pA/°C typ
Absolute AIN Voltage Limits ²	AGND + 100 mV		V min
	$AV_{DD} - 100 \text{ mV}$		V max
Auxiliary ADC			
Input Voltage Range ^{9, 10}	0 to V _{REF}	Unipolar Mode, for Bipolar Mode	V
	105	See Note 11	A /X 7 .
Average Analog Input Current	125	Valtage on the Universities ADC	nA/V typ
Average Analog Input Current Drift Absolute AINIVoltage Limits ² , ¹¹	$\frac{12}{4}$	voltage on the Unbullered Auxiliary ADC	V min
Absolute AIN voltage Linits	$AV_{res} + 30 \text{ mV}$		V max
External Reference Inputs			v IIIdx
REFIN(+) to $REFIN(-)$ Range ²	1		V min
	AV _{DD}		V max
Average Reference Input Current	1	Both ADCs Enabled	μA/V typ
Average Reference Input Current Drift	±0.1		nA/V/°C typ
"NO Ext. REF" Trigger Voltage	0.3	NOXREF Bit Active if $V_{REF} < 0.3 V$	V min
	0.65	NOXREF Bit Inactive if $V_{REF} > 0.65 V$	V max
ADC SYSTEM CALIBRATION			
Full-Scale Calibration Limit	$1.05 \times FS$		V max
Zero-Scale Calibration Limit	-1.05 imes FS		V min
Input Span	0.8 imes FS		V min
	$2.1 \times FS$		V max
ANALOG (DAC) OUTPUT			
Voltage Range	0 to V _{REF}	DACRN = 0 in $DACCON SFR$	V typ
	0 to AV _{DD}	DACRN = 1 in DACCON SFR	V typ
Resistive Load	10	From DAC Output to AGND	k Ω typ
Capacitive Load	100	From DAC Output to AGND	pF typ
Output Impedance	0.5		Ωtyp
I _{SINK}	50		μA typ
TEMPERATURE SENSOR			
Accuracy	±2		°C typ
I nermal Impedance (θ_{JA})	90	MQFP Package CSD Dackage (Paca Election) ¹²	°C/W typ
	54	Cor rackage (Dase Floating)	U/w typ

MEMORY ORGANIZATION

The ADuC836 contains four different memory blocks:

- 62 Kbytes of On-Chip Flash/EE Program Memory
- 4 Kbytes of On-Chip Flash/EE Data Memory
- 256 bytes of General-Purpose RAM
- 2 Kbytes of Internal XRAM

(1) Flash/EE Program Memory

The ADuC836 provides 62 Kbytes of Flash/EE program memory to run user code. The user can choose to run code from this internal memory or run code from an external program memory.

If the user applies power or resets the device while the $\overline{\text{EA}}$ pin is pulled low externally, the part will execute code from the external program space; otherwise, if $\overline{\text{EA}}$ is pulled high externally, the part defaults to code execution from its internal 62 Kbytes of Flash/EE program memory.

Unlike the ADuC816, where code execution can overflow from the internal code space to external code space once the PC becomes greater than 1FFFH, the ADuC836 does not support the rollover from F7FFH in internal code space to F800H in external code space. Instead, the 2048 bytes between F800H and FFFFH will appear as NOP instructions to user code.

Permanently embedded firmware allows code to be serially downloaded to the 62 Kbytes of internal code space via the UART serial port while the device is in-circuit. No external hardware is required.

56 Kbytes of the program memory can be reprogrammed during runtime; thus the code space can be upgraded in the field using a user defined protocol or it can be used as a data memory. This is discussed in more detail in the Flash/EE Memory section.

(2) Flash/EE Data Memory

4 Kbytes of Flash/EE Data Memory are available to the user and can be accessed indirectly via a group of registers mapped into the Special Function Register (SFR) area. Access to the Flash/EE Data memory is discussed in detail in the Flash/EE Memory section.

(3) General-Purpose RAM

The general-purpose RAM is divided into two separate memories: the upper and lower 128 bytes of RAM. The lower 128 bytes of RAM can be accessed through direct or indirect addressing; the upper 128 bytes of RAM can only be accessed through indirect addressing as it shares the same address space as the SFR space, which can only be accessed through direct addressing.

The lower 128 bytes of internal data memory are mapped as shown in Figure 2. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits), locations 20H through 2FH above the register banks, form a block of directly addressable bit locations at bit addresses 00H through 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 2048 bytes.

GENERAL NOTES PERTAINING TO THIS DATA SHEET

- 1. SET implies a Logic 1 state and CLEARED implies a Logic 0 state, unless otherwise stated.
- SET and CLEARED also imply that the bit is set or automatically cleared by the ADuC836 hardware, unless otherwise stated.
- 3. User software should not write 1s to reserved or unimplemented bits as they may be used in future products.
- Any pin numbers used throughout this data sheet refer to the 52-lead MQFP package, unless otherwise stated.

Reset initializes the stack pointer to location 07H. Any call or push pre-increments the SP before loading the stack. Therefore, loading the stack starts from location 08H, which is also the first register (R0) of register bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.



Figure 2. Lower 128 Bytes of Internal Data Memory

(4) Internal XRAM

The ADuC836 contains 2 Kbytes of on-chip extended data memory. This memory, although on-chip, is accessed via the MOVX instruction. The 2 Kbytes of internal XRAM are mapped into the bottom 2 Kbytes of the external address space if the CFG836.0 bit is set. Otherwise, access to the external data memory will occur just like a standard 8051.

Even with the CFG836.0 bit set, access to the external XRAM will occur once the 24-bit DPTR is greater than 0007FFH.



Figure 3. Internal and External XRAM

COMPLETE SFR MAP

Figure 6 shows a full SFR memory map and the SFR contents after RESET. NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented, i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations that are reserved for future use are shaded (RESERVED) and should not be accessed by user software.

ISPI WCOL SPM SPM </th
EFH 0 F9H 00H F9H
B B
F7H 0 F6H 0 F6H 0 F7H 0<
MDC MDC MDI IZCM IZCRS IZCTX IZCI BITS EFH 0 EOH 0 EOH 0 EAH 0 EBH 0 BITS EAH SSH EAH SSH ECH 9AH EOH SSH ECH 9AH EOH SSH EAH SSH ECH SSH EAH
EFH 0 EEH 0 EBH 0 EBH 0 EBT EBH 0H RESERVED EBH S3H ECH 9AH EDH 99H RESERVED RESERVED E7H 0 E6H 0 E3H
ACC RESERVED OFOM OFOH OF1L OF1H RESERVED E7H 0 E6H 0 E3H 0 E2H 0 E1H 0 E0H 0 BITS RDY0 RDY1 CAL NOXREF ERR0 ERR1 D
E7H 0 E6H 0 E3H 0 E3H 0 E3H 0 E1H 0 E0H 0 BITS RDY0 RDY1 CAL NOXREF ERR0 ERR1 DBH 0 DBH DBH 0 DBH
Exh O D<
RDY0 RDY1 CAL NOXREF ERR1 DBH 0 DBH DBH DBH DBH DBH DBH
DFH 0 DEH D
CY D7H AC F0 RSI RS0 OV F1 P D7H 0 D6H 0 D5H 0 D4H 0 D3H 0 D2H 0 D1H 0 D0H 0 BITS D0H 00H D2H 0 D1H 0 D0H 0 D1H 0 D0H 0 D1H 0 D0H 0 D2H 0 D1H 0 D0H 0 D2H 0 D1H 0 D0H 0 D2H 0 D4H 45H D5H 00H D2H D3H D0H D4H 45H D5H D0H D7H D3H D0H D4H D5H D2H D7H D3H D7H D2H D2H
DTH D
TF2 EXF2 RCLK TCLK EXEND TR2 CNT2 CAP2 BITS TF2 CFH 0 CH 0 CH 0 H 0H
TF2 EXF2 RCLK TCLK EXEN2 TR2 CNT2 CAP2 BITS IZCON RESERVED RCAP2L IRCAP2L IRC
CFH 0 CEH CEH 0 CEH CEH 0 CEH
PRE3 PRE2 PRE1 PRE0 WDR WDS WDR BITS WDCON RESERVED CHIPID RESERVED REserved<
C7H 0 C6H 0 C4H 1 C3H 0 C2H 0 C1H 0 C0H 0 HESERVED RESERVED R
IP ECON RESERVED RESERVED RESERVED EDATA1 EDATA2 EDATA3 EDATA4 BFH 0 BEH 0 BCH 0 BCH 0 BAH B9H 0 BITS BBH 00H BSFRVED RESERVED RESERVED BCATA1 EDATA2 EDATA3 EDATA4 BFH 0 BCH 0 BCH 0 BAH B9H 0 BBH 0 BITS BBH 00H BSFRVED RESERVED RESERVED BCATA1 EDATA2 EDATA3 EDATA4 BFH 0 BCH 00H BCH 0H BDH 0H BCH 00H BDH 0H BCH 0
PADC P12 PS P11 PX1 P10 PX0 BITS BFH 0 BEH 0 BCH 0 BCH 0 BEH 0 BBH 0 BBH 0 BITS BBH 00H BPWMOL PWMOH PWM1L PWM1H RESERVED BCH 00H BEH 00H BFH 00H AFH 0 AFH 0 ABH 0 ABH 0 BFF
Image: Normal and the state of both of
RD WR T1 T0 INTT INTO TXD RXD BITS P3 PWM0L PWM0H PWM1L PWM1H RESERVED RESERVE
B7H 1 B6H 1 B5H 1 B4H 1 B1H 1 B0H 1 ETC B0H FFH B1H 00H B2H 00H B3H 00H B4H 0H
EAD EAD ET2 ES ET1 EX1 ET0 EX0 BITS ABH 00H ABH
AFH 0 AEH 0 ADH 0 ACH 0 ABH 0 AAH 0 A9H 0 A8H 0 BITS ABH 00H A9H A0H RESERVED RESERVED RESERVED RESERVED RESERVED AEH 00H AFH 00H P2 TIMECON HTHSEC ² SEC ² MIN ² HOUR ² INTVAL DPCON
P2 TIMECON HTHSEC ² SEC ² MIN ² HOUR ² INTVAL DPCON
BITS P2 INVECTIVE SEC WINV NOON INTOLE DPCON
A/H I A6H I A5H I A4H I A3H I A2H I ATH I A0H I A7H 00H A1H 00H A2H 00H A3H 00H A4H 00H A5H 00H A6H 00H A7H 00H
SM0 SM1 SM2 REN TB8 RB8 T1 R1 DTC SCON SBUF DECEDUED DECEDUED T3FD T3CON RESERVED
9FH 0 9EH 0 9DH 0 9CH 0 9BH 0 9AH 0 99H 0 98H 0 BITS 98H 00H 99H 00H RESERVED RESERV
ATH 1 96H 1 96H 1 96H 1 96H 1 96H 1 97H 1
90H FFH 90H FFH 90H 90H 90H 90H 90H 90H 90H 90H 90H 90
TF1 TR1 TF0 TR0 IE1 IT1 IE0 IT0 BITS TCON TMOD TL0 TL1 TH0 TH1 RESERVED RESERVED
P0 SP DPL DPH DPP PCON
87H 1 86H 1 85H 1 84H 1 83H 1 82H 1 81H 1 80H 1 BITS 80H EEH 81H 07H 82H 00H 83H 00H 84H 00H RESERVED RESERVED 87H 00H

NOTES

¹CALIBRATION COEFFICIENTS ARE PRECONFIGURED AT POWER-UP TO FACTORY CALIBRATED VALUES. ²THESE SFRs MAINTAIN THEIR PRERESET VALUES AFTER A RESET IF TIMECON.0 = 1.





SFR NOTE: SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT ADDRESSABLE.

Figure 6. Special Function Register Locations and Their Reset Default Values

ADC0CON (Primary ADC Control Register) and ADC1CON (Auxiliary ADC Control Register)

The ADC0CON and ADC1CON SFRs are used to configure the primary and auxiliary ADC for reference and channel selection, unipolar or bipolar coding and, in the case of the primary ADC, range (the auxiliary ADC operates on a fixed input range of $\pm V_{REF}$).

ADC0CON	Primary ADC Control SFR	ADC1CON	Auxiliary ADC Control SFR
SFR Address	D2H	SFR Address	D3H
Power-On Default Value	07H	Power-On Default Value	00H
Bit Addressable	No	Bit Addressable	No

Table VI. ADC0CON SFR Bit Designations

Bit	Name	Descr	iption			
7		Reserved for Future Use				
6	XREF0	Primary ADC External Reference S Set by user to enable the primary A Cleared by user to enable the prima			leference Se primary AD the primar	ect Bit. C to use the external reference via REFIN(+)/REFIN(–). ADC to use the internal band gap reference (V _{REF} = 1.25 V).
5	CH1	Primar	y ADC C	hannel S	election Bit	
4	CH0	Writter CH1 0 1 1	n by the u CH0 0 1 0 1	ser to selv Positiv AIN1 AIN3 AIN2 AIN3	ect the diffe e Input	rential input pairs used by the primary ADC as follows: Negative Input AIN2 AIN4 AIN2 (Internal Short) AIN2
3	UNI0	Primar Set by Cleared	y ADC U user to er d by user	Inipolar H able unij to enable	Bit. polar coding bipolar cod	, i.e., zero differential input will result in 000000H output. ing, i.e., zero differential input will result in 800000H output.
2	RN2	Primary ADC Range Bits.				
1	RN1	Written by the user to select the primary ADC input range as follows:				
0	RN0	RN2 0 0 0 1 1 1 1	RN1 0 0 1 1 0 0 1 1	RN0 0 1 0 1 0 1 0 1	Selected ±20 mV ±40 mV ±80 mV ±160 m' ±320 m' ±640 m' ±1.28 V +2.56 V	Primary ADC Input Range ($V_{REF} = 2.5 V$) (0 mV-20 mV in Unipolar Mode) (0 mV-40 mV in Unipolar Mode) (0 mV-80 mV in Unipolar Mode) V (0 mV-160 mV in Unipolar Mode) V (0 mV-320 mV in Unipolar Mode) V (0 mV-640 mV in Unipolar Mode) (0 V-1.28 V in Unipolar Mode) (0 V-2.56 V in Unipolar Mode)

Table VII. ADC1CON SFR Bit Designations

Bit	Name	Description				
7		Reserved for Future Use				
6	XREF1	Auxiliary ADC External Reference Bit. Set by user to enable the auxiliary ADC to use the external reference via REFIN(+)/REFIN(-). Cleared by user to enable the auxiliary ADC to use the internal band gap reference.				
5	ACH1	Auxiliary ADC Channel Selection Bits.				
4	ACH0	Written by the user to select the single-ended input pins used to drive the auxiliary ADC as follows:ACH1ACH0Positive InputNegative Input00AIN3AGND01AIN4AGND10Temp SensorAGND (Temp Sensor routed to the ADC input)11AIN5AGND				
3	UNI1	Auxiliary ADC Unipolar Bit. Set by user to enable unipolar coding, i.e., zero input will result in 0000H output. Cleared by user to enable bipolar coding, i.e., zero input will result in 8000H output.				
2		Reserved for Future Use				
1		Reserved for Future Use				
0		Reserved for Future Use				

NOTES

1. When the temperature sensor is selected, user code must select internal reference via XREF1 bit above and clear the UNI1 bit (ADC1CON.3) to select bipolar coding. 2. The temperature sensor is factory calibrated to yield conversion results 8000H at 0°C.

3. A +1°C change in temperature will result in a +1 LSB change in the ADC1H Register ADC conversion result.

PRIMARY AND AUXILIARY ADC CIRCUIT DESCRIPTION Overview

The ADuC836 incorporates two independent Σ - Δ ADCs (primary and auxiliary) with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain gage, pressure transducer, or temperature measurement applications.

Primary ADC

This ADC is intended to convert the primary sensor input. The input is buffered and can be programmed for one of eight input ranges from ± 20 mV to ± 2.56 V being driven from one of three differential input channel options AIN1/2, AIN3/4, or AIN3/2. The input channel is internally buffered, allowing the part to handle significant source impedances on the analog input and

allowing R/C filtering (for noise rejection or RFI reduction) to be placed on the analog inputs if required. On-chip burnout currents can also be turned on. These currents can be used to check that a transducer on the selected channel is still operational before attempting to take measurements.

The ADC employs a Σ - Δ conversion technique to realize up to 16 bits of no missing codes performance. The Σ - Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc³ programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A chopping scheme is also employed to minimize ADC offset errors. A block diagram of the primary ADC is shown in Figure 7.



Figure 7. Primary ADC Block Diagram

ADC Chopping

Both ADCs on the ADuC836 implement a chopping scheme whereby the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc³ filters therefore have a positive offset and negative offset term included.

As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data SFRs. In this way, while the ADC throughput or update rate is as discussed earlier and illustrated in Table VIII, the full settling time through the ADC (or the time to a first conversion result) will actually be given by $2 \times t_{ADC}$.

The chopping scheme incorporated in the ADuC836 ADC results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors.

Calibration

The ADuC836 provides four calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table V. In fact, every ADuC836 has already been factory calibrated. The resultant Offset and Gain calibration coefficients for both the primary and auxiliary ADCs are stored on-chip in manufacturing-specific Flash/EE memory locations. At power-on or after reset, these factory calibration coefficients are automatically downloaded to the calibration registers in the ADuC836 SFR space. Each ADC (primary and auxiliary) has dedicated calibration SFRs, which have been described earlier as part of the general ADC SFR description. However, the factory calibration values in the ADC calibration SFRs will be overwritten if any one of the four calibration options are initiated and that ADC is enabled via the ADC enable bits in ADCMODE.

Even though an internal offset calibration mode is described below, it should be recognized that both ADCs are chopped. This chopping scheme inherently minimizes offset and means that an internal offset calibration should never be required. Also, because factory $5 \text{ V}/25^{\circ}\text{C}$ gain calibration coefficients are automatically present at power-on an internal full-scale calibration will only be required if the part is being operated at 3 V or at temperatures significantly different from 25°C.

The ADuC836 offers internal or system calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two different input conditions: zero-scale and full-scale points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. The result of the zero-scale calibration conversion is stored in the Offset Calibration Registers for the appropriate ADC. The result of the full-scale calibration conversion is stored in the Gain Calibration Registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an internal zero-scale or full-scale calibration, the respective zero-scale input and full-scale inputs are automatically connected to the ADC input pins internally to the device. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the external ADC pins before the calibration mode is initiated. In this way, external ADC errors are taken into account and minimized as a result of system calibration. It should also be noted that to optimize calibration accuracy, all ADuC836 ADC calibrations are carried out automatically at the slowest update rate.

Internally in the ADuC836, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the ADCSTAT SFR to determine end of calibration via a polling sequence or interrupt driven routine.

NONVOLATILE FLASH/EE MEMORY Flash/EE Memory Overview

The ADuC836 incorporates Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit, reprogrammable code and data memory space. Flash/EE memory is a relatively recent type of nonvolatile memory technology and is based on a single transistor cell architecture. This technology is basically an outgrowth of EPROM technology and was developed through the late 1980s. Flash/EE memory takes the flexible in-circuit reprogrammable features of EEPROM and combines them with the space efficient/density features of EPROM (see Figure 15).

Because Flash/EE technology is based on a single transistor cell architecture, a Flash memory array, like EPROM, can be implemented to achieve the space efficiencies or memory densities required by a given design.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased; the erase being performed in page blocks. Thus, flash memory is often and more correctly referred to as Flash/EE memory.



Figure 15. Flash/EE Memory Development

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated into the ADuC836, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace one-time programmable (OTP) devices at remote operating nodes.

Flash/EE Memory and the ADuC836

The ADuC836 provides two arrays of Flash/EE memory for user applications. 62 Kbytes of Flash/EE program space are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed in-circuit, using the serial download mode provided, using conventional third party memory programmers, or via any user defined protocol in User Download (ULOAD) mode.

A 4 Kbyte Flash/EE data memory space is also provided on-chip. This may be used as a general-purpose, nonvolatile scratch pad area. User access to this area is via a group of seven SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

ADuC836 Flash/EE Memory Reliability

The Flash/EE program and data memory arrays on the ADuC836 are fully qualified for two key Flash/EE memory characteristics: Flash/EE Memory Cycling Endurance and Flash/EE Memory Data Retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events, which are defined as:

- a. Initial page erase sequence
- b. Read/verify sequence
- c. Byte program sequenced. Second read/verify sequence
- Memory Endurance
 Cycle

A Single Flash/EE

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specification tables, the ADuC836 Flash/EE Memory Endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of -40°C, +25°C, +85°C, and +125°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the ADuC836 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature ($T_J = 55^{\circ}$ C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, will derate with T_J , as shown in Figure 16.



Figure 16. Flash/EE Memory Data Retention

PULSEWIDTH MODULATOR (PWM)

The PWM on the ADuC836 is a highly flexible PWM offering programmable resolution and input clock, and can be configured for any one of six different modes of operation. Two of these modes allow the PWM to be configured as a Σ - Δ DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 26.



Figure 26. PWM Block Diagram

The PWM uses five SFRs: the control SFR, PWMCON, and four data SFRs: PWM0H, PWM0L, PWM1H, and PWM1L.

PWMCON (as described in Table XVI) controls the different modes of operation of the PWM as well as the PWM clock frequency. PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs at P1.0 and P1.1.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

PWMCON	PWM Control SFR
SFR Address	AEH
Power-On Default Value	00H
Bit Addressable	No

Bit	Name	Description			
7		Reserved for Future	e Use		
6	MD2	PWM Mode Bits			
5	MD1	The MD2/1/0 bits c	choose the PWM mode as follows:		
4	MD0	MD2 MD1 0 0 0 1 0 1 1 0 1 0	 MD0 Mode 0 Mode 0: PWM Disabled 1 Mode 1: Single Variable Resolution PWM 0 Mode 2: Twin 8-bit PWM 1 Mode 3: Twin 16-bit PWM 0 Mode 4: Dual NRZ 16-bit Σ-Δ DAC 1 Mode 5: Dual 8-bit PWM 		
		1 1	0 Mode 6: Dual RZ 16-bit Σ - Δ DAC		
3	CDIV1	PWM Clock Divide	WM Clock Divider. Scale the clock course for the DWM courter as follows:		
2	CLIV	CDIV1 CDIV0 0 0 0 1 1 0 1 1	Description PWM Counter = Selected Clock/1 PWM Counter = Selected Clock 4 PWM Counter = Selected Clock/16 PWM Counter = Selected Clock/64		
1	CSEL1	PWM Clock Divider.			
0	CSEL0	Select the clock source for the PWM as follows:			
		CSEL1 CSEL0 0 0 0 1 1 0 1 1	Description PWM Clock = $f_{XTAL}/15$ PWM Clock = f_{XTAL} PWM Clock = External Input at P3.4/T0/PWMCLK PWM Clock = f_{VCO} (12.58 MHz)		

Table XVI. PWMCON SFR Bit Designations

PWM MODES OF OPERATION

Mode 0: PWM Disabled

The PWM is disabled, allowing P1.0 and P1.1 to be used as normal.

Mode 1: Single Variable Resolution PWM

In Mode 1, both the pulse length and the cycle time (period) are programmable in user code, allowing the resolution of the PWM to be variable.

PWM1H/L sets the period of the output waveform. Reducing PWM1H/L reduces the resolution of the PWM output but increases the maximum output rate of the PWM (e.g., setting PWM1H/L to 65536 gives a 16-bit PWM with a maximum output rate of 192 Hz (12.583 MHz/65536). Setting PWM1H/L to 4096 gives a 12-bit PWM with a maximum output rate of 3072 Hz (12.583 MHz/4096)).

PWM0H/L sets the duty cycle of the PWM output waveform, as shown in Figure 27.





Mode 2: Twin 8-Bit PWM

In Mode 2, the duty cycle of the PWM outputs and the resolution of the PWM outputs are both programmable. The maximum resolution of the PWM output is eight bits.

PWM1L sets the period for both PWM outputs. Typically this will be set to 255 (FFH) to give an 8-bit PWM, although it is possible to reduce this as necessary. A value of 100 could be loaded here to give a percentage PWM (i.e., the PWM is accurate to 1%).

The outputs of the PWM at P1.0 and P1.1 are shown in Figure 28. As can be seen, the output of PWM0 (P1.0) goes low when the PWM counter equals PWM0L. The output of PWM1 (P1.1) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.



Figure 28. PWM Mode 2

Mode 3: Twin 16-Bit PWM

In Mode 3, the PWM counter is fixed to count from 0 to 65536, giving a fixed 16-bit PWM. Operating from the 12.58 MHz core clock results in a PWM output rate of 192 Hz. The duty cycle of the PWM outputs at P1.0 and P1.1 is independently programmable.

As in Figure 29, while the PWM counter is less than PWM0H/L, the output of PWM0 (P1.0) is high. Once the PWM counter equals PWM0H/L, PWM0 (P1.0) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P1.1) is high. Once the PWM counter equals PWM1H/L, PWM1 (P1.1) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized (i.e., once the PWM counter rolls over to 0, both PWM0 (P1.0) and PWM1 (P1.1) will go high).



Figure 29. PWM Mode 3

Mode 4: Dual NRZ 16-Bit Σ - Δ DAC

Mode 4 provides a high speed PWM output similar to that of a Σ - Δ DAC. Typically, this mode will be used with the PWM clock equal to 12.58 MHz.

In this mode, P1.0 and P1.1 are updated every PWM clock (80 ns in the case of 12.58 MHz). Over any 65536 cycles (16-bit PWM), PWM0 (P1.0) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P1.1) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

If PWM1H is set to 4010H (slightly above one quarter of FS), then typically P1.1 will be low for three clocks and high for one clock (each clock is approximately 80 ns). Over every 65536 clocks, the PWM will compromise for the fact that the output should be slightly above one quarter of full scale by having a high cycle followed by only two low cycles.



Figure 30. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ - Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ - Δ DAC output at 49 kHz.

Mode 5: Dual 8-Bit PWM

In Mode 5, the duty cycle of the PWM outputs and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

The output resolution is set by the PWM1L and PWM1H SFRs for the P1.0 and P1.1 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P1.0 and P1.1, respectively. Both PWMs have the same clock source and clock divider.



Figure 31. PWM Mode 5

Mode 6: Dual RZ 16-Bit Σ - Δ DAC

Mode 6 provides a high speed PWM output similar to that of a Σ - Δ DAC. Mode 6 operates very similarly to Mode 4. However, the key difference is that Mode 6 provides return to zero (RZ) Σ - Δ DAC output. Mode 4 provides non-return-to-zero Σ - Δ DAC outputs. The RZ mode ensures that any difference in the rise and fall times will not affect the Σ - Δ DAC INL. However, the RZ Mode halves the dynamic range of the Σ - Δ DAC outputs from 0 \rightarrow AV_{DD} to 0 \rightarrow AV_{DD}/2. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one quarter of FS) then P1.1 will typically be low for three full clocks (3×80 ns), high for half a clock (40 ns) and then low again for half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM will compromise for the fact that the output should be slightly above one quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ - Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ - Δ DAC output at 49 kHz.



Figure 32. PWM Mode 6

ON-CHIP PLL

The ADuC836 is intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency, or at binary submultiples of it, to allow power saving in cases where maximum core performance is not

PLLCON	PLL Control Register
SFR Address	D7H
Power-On Default Value	03H
Bit Addressable	No

required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. This choice of frequencies ensures that the modulators and the core will be synchronous, regardless of the core clock rate. The PLL control register is PLLCON.

Table XVII. PLLCON SFR Bit Designations

Bit	Name	Descri	ption		
7	OSC_PD	Oscillat Set by u Cleared This fea	or Power-l user to halt by user to ature allow	Down Bit. the 32 kH enable th s the TIC	Hz oscillator in Power-Down mode. ne 32 kHz oscillator in Power-Down mode. to continue counting even in Power-Down mode.
6	LOCK	 PLL Lock Bit. This is a read-only bit. Set automatically at power-on to indicate the PLL loop is correctly tracking the crystal clock. After power-down, this bit can be polled to wait for the PLL to lock. Cleared automatically at power-on to indicate the PLL is not correctly tracking the crystal clock. This may be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 12.58 MHz ± 20%. After the ADuC836 wakes up from power-down, user code may poll this bit to wait for the PLL to lock. If LOCK = 0, then the PLL is not locked. 			
5		Reserve	d for Futu	re Use. Sl	nould be written with 0.
4	LTEA	Reading this bit returns the state of the external $\overline{\text{EA}}$ pin latched at reset or power-on.			
3	FINT	Fast Int Set by u regardle the core the fast	terrupt Res user enablings of the co e resumes of interrupt	sponse Bit ng the resp onfiguratio code exect response f	ponse to any interrupt to be executed at the fastest core clock frequency, on of the CD2–0 bits (see below). After user code has returned from an interrupt, ation at the core clock selected by the CD2–0 bits. Cleared by user to disable eature.
2	CD2	CPU (C	Core Clock	x) Divider	Bits.
1	CD1	This number determines the frequency at which the microcontroller core will operate.			
0	CD0	CD2 0 0 0 1 1 1 1 1	CD1 0 1 1 0 0 1 1	CD0 0 1 0 1 0 1 0 1	Core Clock Frequency (MHz) 12.582912 6.291456 3.145728 1.572864 (Default Core Clock Frequency) 0.786432 0.393216 0.196608 0.098304

TIME INTERVAL COUNTER (WAKE-UP/RTC TIMER)

A time interval counter (TIC) is provided on-chip for:

- Periodically waking up the part from power-down
- Implementing a real-time clock
- Counting longer intervals than the standard 8051 compatible timers are capable of

The TIC is capable of timeout intervals ranging from 1/128th second to 255 hours. Furthermore, this counter is clocked by the crystal oscillator rather than the by PLL, and thus has the ability to remain active in Power-Down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely, spaced readings are required.

The TIC counter can easily be used to generate a real-time clock. The hardware will count in seconds, minutes, and hours; however, user software will have to count in days, months, and years. The current time can be written to the timebase SFRs (HTHSEC, SEC, MIN, and HOUR) while TCEN is low. When the RTC timer is enabled (TCEN is set), the TCEN bit itself and the HTHSEC, SEC, MIN, and HOUR Registers are not reset to 00H after a hardware or watchdog timer reset. This is to prevent the need to recalibrate the real-time clock after a reset. However, these registers will be reset to 00H after a power cycle (independent of TCEN) or after any reset if TCEN is clear.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow will clock the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See IEIP2 SFR description under the Interrupt System section.) If the ADuC836 is in Power-Down mode, again with TIC interrupt enabled, the TII bit will wake up the device and resume code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table XVIII with a block diagram of the TIC shown in Figure 33.



TCEN 32.768kHz EXTERNAL CRYSTAL

Figure 33. TIC, Simplified Block Diagram

Bit	Name	Description				
7		Reserved for Future Use				
6		Reserved for Future Use. For future product code compatibility, this bit should be written as a 1.				
5	ITS1	Interval Timebase Selection Bits.				
4	ITS0	Written by user to determine the interval counter update rate.				
		ITS1 ITS0 Interval Timebase				
		0 0 1/128 Second				
		0 1 Seconds				
		1 0 Minutes				
		1 1 Hours				
3	STI	Single Time Interval Bit. Set by user to generate a single interval timeout. If set, a timeout will clear the TIEN bit. Cleared by user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.				
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.				
1	TIEN	Time Interval Enable Bit. Set by user to enable the 8-bit time interval counter. Cleared by user to disable and clear the contents of the 8-bit interval counter. To ensure that the 8-bit interval counter is cleared, TIEN must be held low for at least 30.5 µs (32 kHz).				
0	TCEN	Time Clock Enable Bit. Set by user to enable the time clock to the time interval counters. Cleared by user to disable the 32 kHz clock to the TIC and clear the 8-bit prescaler and the HTHSEC, SEC, MIN, and HOURS SFRs. To ensure that these registers are cleared, TCEN must be held low for at least 30.5 µs (32 kHz). The time registers (HTHSEC, SEC, MIN, and HOUR) can be written only while TCEN is low.				

Table XVIII. TIMECON SFR Bit Designations

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC836 enters an erroneous state, possibly due to a programming error, electrical noise, or RFI. The watchdog function can be disabled by clearing the WDE (Watchdog Enable) bit in the Watchdog Control (WDCON) SFR. When enabled, the watchdog circuit will generate a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3–0 bits in WDCON). The watchdog timer itself is a 16-bit counter that is clocked at 32.768 kHz. The watchdog timeout interval can be adjusted via the PRE3–0 bits in WDCON. Full control and status of the watchdog timer function can be controlled via the Watchdog Timer Control SFR (WDCON). The WDCON SFR can only be written by user software if the double write sequence described in WDWR below is initiated on every write access to the WDCON SFR.

Watchdog Timer Control Register
С0Н
10H
Yes

Table XIX. WDCON SFR Bit Designations

Bit	Name	Description				
7	PRE3	Watchdog Timer Prescale Bits.				
6	PRE2	The Watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/f_{PLL}))$				
5	PRE1	$(0 \le PRE \le 7; f_{PLL} = 32.768 \text{ kHz})$				
4	PRE0	PRE3PRE2PRE1PRE0Period (ms)Action00015.6Reset or Interrupt00131.2Reset or Interrupt001062.5Reset or Interrupt001125Reset or Interrupt010250Reset or Interrupt0101500Reset or Interrupt0112000Reset or Interrupt0111000Reset or Interrupt0118000Reset or Interrupt0118000Reset or Interrupt1000.0Immediate ResetPRE3-0 > 10011001Festored				
3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog will generate an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR EA instruction, and it is also a fixed, high priority interrupt. If the watchdog is not being used to monitor the system, it can alternatively be used as a timer. The prescaler is used to set the timeout period in which an interrupt will be generated. (See also Note 1, Table XXXIX in the Interrupt System section.)				
2	WDS	Watchdog Status Bit. Set by the watchdog controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.				
1	WDE	Watchdog Enable Bit. Set by user to enable the watchdog and clear its counters. If a 1 is not written to this bit within the watchdog timeout period, the watchdog will generate a reset or interrupt, depending on WDIR. Cleared under the following conditions: User writes 0, watchdog reset (WDIR = 0); hardware reset; PSM interrupt.				
0	WDWR	Watchdog Write Enable Bit. To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the very next instruction must be a write instruction to the WDCON SFR. For example:				
		CLR EA ; disable interrupts while writing ; to WDT SETB WDWR ; allow write to WDCON MOV WDCON, #72h ; enable WDT for 2.0s timeout SETB EA ; enable interrupts again (if rqd)				

8052 COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits, which are also available to the user on-chip. These remaining functions are mostly 8052 compatible (with a few additional features) and are controlled via standard 8052 SFR bit definitions.

Parallel I/O

The ADuC836 uses four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some ports are capable of external memory operations while others are multiplexed with alternate functions for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general-purpose I/O pin.

Port 0

Port 0 is an 8-bit open-drain bidirectional I/O port that is directly controlled via the Port 0 SFR. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory.

Figure 36 shows a typical bit latch and I/O buffer for a Port 0 port pin. The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which will clock in a value from the internal bus in response to a "write to latch" signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a "read latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read pin" signal from the CPU. Some instructions that read a port activate the "read latch" signal, and others activate the "read pin" signal. See the Read-Modify-Write Instructions section for more details.



Figure 36. Port 0 Bit Latch and I/O Buffer

As shown in Figure 36, the output drivers of Port 0 pins are switchable to an internal ADDR and ADDR/DATA bus by an internal CONTROL signal for use in external memory accesses. During external memory accesses, the P0 SFR is written with 1s (i.e., all of its bit latches become 1s). When accessing external memory, the CONTROL signal in Figure 36 goes high, enabling push-pull operation of the output pin from the internal address or data bus (ADDR/DATA line). Therefore, no external pull-ups are required on Port 0 for it to access external memory.

In general-purpose I/O port mode, Port 0 pins that have 1s written to them via the Port 0 SFR will be configured as open-drain and therefore will float. In this state, Port 0 pins can be used as high impedance inputs. This is represented in Figure 36 by the NAND gate whose output remains high as long as the CONTROL signal is low, thereby disabling the top FET. External pull-up resistors are therefore required when Port 0 pins are used as general-purpose outputs. Port 0 pins with 0s written to them will drive a logic low output voltage (V_{OL}) and will be capable of sinking 1.6 mA.

Port 1

Port 1 is also an 8-bit port directly controlled via the P1 SFR. The Port 1 pins are divided into two distinct pin groupings: P1.0 to P1.1 and P1.2 to P1.7.

P1.0 and P1.1

P1.0 and P1.1 are bidirectional digital I/O pins with internal pull-ups.

If P1.0 and P1.1 have 1s written to them via the P1 SFR, they are pulled high by the internal pull-up resistors. In this state, they can also be used as inputs. As input pins being externally pulled low, they will source current because of the internal pull-ups. With 0s written to them, both of these pins will drive a logic low output voltage (V_{OL}) and will be capable of sinking 10 mA compared to the standard 1.6 mA sink capability on the other port pins.

These pins also have various secondary functions described in Table XXIV. The Timer 2 alternate functions of P1.0 and P1.1 can only be activated if the corresponding bit latch in the P1 SFR contains a 1. Otherwise, the port pin is stuck at 0. In the case of the PWM outputs at P1.0 and P1.1, the PWM outputs will overwrite anything written to P1.0 or P1.1.

Table XXIV.	P1.0 and P1.1 Alternate Pin Functions
-------------	---------------------------------------

Pin	Alternate Function
P1.0	T2 (Timer/Counter 2 External Input)
	PWM0 (PWM0 output at this pin)
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger) PWM1 (PWM1 output at this pin)

Figure 37 shows a typical bit latch and I/O buffer for a P1.0 or P1.1 port pin. No external memory access is required from either of these pins, although internal pull-ups are present.



Figure 37. P1.0 and P1.1 Bit Latch and I/O Buffer

The internal pull-up consists of active circuitry, as shown in Figure 38. Whenever a P1.0 or P1.1 bit latch transitions from low to high, Q1 in Figure 38 turns on for two oscillator periods to quickly pull the pin to a logic high state. Once there, the weaker Q3 turns on, thereby latching the pin to a logic high. If the pin is momentarily pulled low externally, Q3 will turn off, but the very weak Q2 will continue to source some current into the pin, attempting to restore it to a logic high.



Figure 38. Internal Pull-Up Configuration

Power Supplies

The ADuC836's operational power supply voltage range is 2.7 V to 5.25 V. Although the guaranteed data sheet specifications are given only for power supplies within 2.7 V to 3.6 V or +5% of the nominal 5 V level, the chip will function equally well at any power supply level between 2.7 V and 5.25 V.

Separate analog and digital power supply pins (AV_{DD} and DV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals that are often present on the system DV_{DD} line. In this mode, the part can also operate with split supplies, that is, using different voltage supply levels for each supply. For example, this means that the system can be designed to operate with a DV_{DD} voltage level of 3 V while the AV_{DD} level can be at 5 V, or vice-versa if required. A typical split-supply configuration is shown in Figure 61.



Figure 61. External Dual-Supply Connections

As an alternative to providing two separate power supplies, AV_{DD} can be kept quiet by placing a small series resistor and/or ferrite bead between it and DV_{DD} , and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 62. In this configuration, other analog circuitry (such as op amps, voltage reference, and so on) can be powered from the AV_{DD} supply line as well.



Figure 62. External Single-Supply Connections

Notice that in Figures 61 and 62, a large value (10 μ F) reservoir capacitor sits on DV_{DD} and a separate 10 μ F capacitor sits on AV_{DD}. Also, local decoupling capacitors (0.1 μ F) are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure the smaller capacitors are closest to each V_{DD} pin with lead lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, it should also be noticed that, at all times, the analog and digital ground pins on the ADuC836 should be referenced to the same system ground reference point.

Power-On Reset (POR) Operation

An internal POR (Power-On Reset) is implemented on the ADuC836. For DV_{DD} below 2.45 V, the internal POR will hold the ADuC836 in reset. As DV_{DD} rises above 2.45 V, an internal timer will time out for typically 128 ms before the part is released from reset. The user must ensure that the power supply has reached a stable 2.7 V minimum level by this time. Likewise on power-down, the internal POR will hold the ADuC836 in reset until the power supply has dropped below 1 V. Figure 63 illustrates the operation of the internal POR in detail.



Figure 63. Internal Power-on-Reset Operation

Power Consumption

The DV_{DD} power supply current consumption is specified in normal, idle, and power-down modes. The AV_{DD} power supply current is specified with the analog peripherals disabled. The normal mode power consumption represents the current drawn from DV_{DD} by the digital core. The other on-chip peripherals (watchdog timer, power supply monitor, and so on) consume negligible current and are therefore lumped in with the normal operating current here. Of course, the user must add any currents sourced by the parallel and serial I/O pins, and those sourced by the DAC in order to determine the total current needed at the ADuC836's DV_{DD} and AV_{DD} supply pins. Also, current drawn from the DV_{DD} supply will increase by approximately 5 mA during Flash/EE erase and program cycles.

OTHER HARDWARE CONSIDERATIONS In-Circuit Serial Download Access

Nearly all ADuC836 designs will want to take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the ADuC836's UART, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is illustrated in Figure 66 with a simple ADM3202 based circuit. If users would rather not include an RS-232 chip onto the target board, refer to the application note, *uC006–A 4-Wire UART-to-PC Interface* available at www.analog.com/microconverter, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the ADuC836.

In addition to the basic UART connections, users will also need a way to trigger the chip into Download mode. This is accomplished via a 1 k Ω pull-down resistor that can be jumpered onto the \overrightarrow{PSEN} pin, as shown in Figure 66. To get the ADuC836 into Download mode, simply connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it will be ready to receive a new program serially. With the jumper removed, the device will power on in Normal mode (and run the program) whenever power is cycled or RESET is toggled.

Note that <u>PSEN</u> is normally an output (as described in the External Memory Interface section) and that it is sampled as an input only on the falling edge of RESET (i.e., at power-up or upon an external manual reset). Note also that if any external circuitry unintentionally pulls <u>PSEN</u> low during power-up or reset events, it could cause the chip to enter Download mode and therefore fail to begin user code execution as it should. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself.

Embedded Serial Port Debugger

From a hardware perspective, entry to Serial Port Debug mode is identical to the serial download entry sequence described above. In fact, both Serial Download and Serial Port Debug modes can be thought of as essentially one mode of operation used in two different ways.

Note that the serial port debugger is fully contained on the ADuC836 device, (unlike ROM monitor type debuggers) and therefore no external memory is needed to enable in-system debug sessions.

Single-Pin Emulation Mode

Also built into the ADuC836 is a dedicated controller for single-pin in-circuit emulation (ICE) using standard production ADuC836 devices. In this mode, emulation access is gained by connection to a single pin, the \overline{EA} pin. Normally, this pin is hard-wired either high or low to select execution from internal or external program memory space, as described earlier. To enable single-pin emulation mode, however, users will need to pull the \overline{EA} pin high through a 1 k Ω resistor, as shown in Figure 66. The emulator will then connect to the 2-pin header also shown in Figure 66. To be compatible with the standard connector that comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch Friction Lock header from Molex (www.molex.com) such as their part number 22-27-2021. Be sure to observe the polarity of this header. As represented in Figure 66, when the Friction Lock tab is at the right, the ground pin should be the lower of the two pins (when viewed from the top).

Parameter SPI MASTER MODE TIMING (CPHA = 0)		Min	Тур	Max	Unit
t _{SL}	SCLOCK Low Pulsewidth*		630		ns
t _{SH}	SCLOCK High Pulsewidth*		630		ns
t _{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t _{DOSU}	Data Output Setup before SCLOCK Edge			150	ns
t _{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t _{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t _{DF}	Data Output Fall Time		10	25	ns
t _{DR}	Data Output Rise Time		10	25	ns
t _{SR}	SCLOCK Rise Time		10	25	ns
t _{SF}	SCLOCK Fall Time		10	25	ns

*Characterized under the following conditions:

1. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1 respectively, i.e., core clock frequency = 1.57 MHz. 2. SPI bit rate selection bits SPR1 and SPR0 in SPICON SFR are both set to 0.



Figure 76. SPI Master Mode Timing (CPHA = 0)

Parameter			Тур	Max	Unit
SPI SLAVE MODE TIMING (CPHA = 1)					
t _{SS}	SS to SCLOCK Edge	0			ns
t _{SL}	SCLOCK Low Pulsewidth		330		ns
t _{SH}	SCLOCK High Pulsewidth		330		ns
t _{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t _{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t _{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t _{DF}	Data Output Fall Time		10	25	ns
t _{DR}	Data Output Rise Time		10	25	ns
t _{SR}	SCLOCK Rise Time		10	25	ns
t _{SF}	SCLOCK Fall Time		10	25	ns
t _{SFS}	SS High after SCLOCK Edge	0			ns



Figure 77. SPI Slave Mode Timing (CPHA = 1)

Parameter		Min	Max	Unit
I ² C-SERIAI	INTERFACE TIMING			
t _L	SCLOCK Low Pulsewidth	4.7		μs
t _H	SCLOCK High Pulsewidth	4.0		μs
t _{SHD}	Start Condition Hold Time	0.6		μs
t _{DSU}	Data Setup Time	100		ns
t _{DHD}	Data Hold Time		0.9	μs
t _{RSU}	Setup Time for Repeated Start	0.6		μs
t _{PSU}	Stop Condition Setup Time	0.6		μs
t _{BUF}	Bus Free Time between a STOP	1.3		μs
	Condition and a START Condition			
t _R	Rise Time of Both SCLOCK and SDATA		300	ns
t _F	Fall Time of Both SCLOCK and SDATA		300	ns
t _{SUP} *	Pulsewidth of Spike Suppressed		50	ns

*Input filtering on both the SCLOCK and SDATA inputs surpresses noise spikes less than 50 ns.



Figure 79. I²C Compatible Interface Timing