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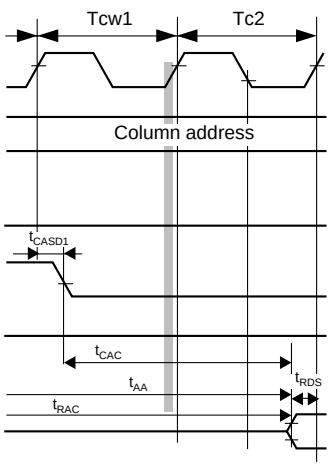
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28.7MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	74
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417040acf28v

Section	Page	Description
25.4 A/D Converter Characteristics Table 25.16 A/D Converter Timing (A mask)	779	Table amended Non-linearity error* Offset error* Full scale error* Quantize error*
26.2 DC Characteristics Table 26.2 DC Characteristics	782	Table amended Schmitt trigger input voltage — PA2, PA5, PA6–PA9, PE0–PE15 — $V_T^+ - V_T^-$ — $V_{CC}\times 0.07$ — — V — $VT^+ \geq V_{CC}\times 0.9V$ (min); $VT^- \leq V_{CC}\times 0.2V$ (max)
	783	Table amended Analog supply current — AI_{CC} — — 4 8 mA f = 16.7MHz AI_{ref} — — 0.5 1*3 mA QFP144 version only *3 2 mA in the A mask version of MASK products.
26.3.2 Control Signal Timing Table 26.5 Control Signal Timing	786	Note amended Notes: *1 SH7042/43 ZTAT (excluding A mask) are 3.2V. *2 The $\overline{RES}$, $\overline{MRES}$, NMI, $\overline{BREQ}$, and $\overline{IRQ7}$–$\overline{IRQ0}$ signals are asynchronous inputs, but when the setup times shown here are provided, the signals are considered to have produced changes at clock rise (for $\overline{RES}$, $\overline{MRES}$, $\overline{BREQ}$) or clock fall (for NMI and $\overline{IRQ7}$–$\overline{IRQ0}$). If the setup times are not provided, recognition is delayed until the next clock rise or fall.
26.3.3 Bus Timing Figure 26.12 DRAM Cycle (Normal Mode, 1 Wait, TPC = 0, RCD = 0)	795	Figure amended 

- Bits 11–10—DTC Mode 1, 0 (MD1, MD0): These bits designate the DTC transfer mode.

Bit 11 (MD1)	Bit 10 (MD0)	Description
0	0	Normal mode
0	1	Repeat mode
1	0	Block transfer mode
1	1	Reserved (setting prohibited)

- Bits 9–8—DTC Data Transfer Size 1, 0 (SZ1, SZ0): These bits designate the data size for data transfers.

Bit 9 (SZ1)	Bit 8 (SZ0)	Description
0	0	Byte (8 bits)
0	1	Word (16 bits)
1	0	Longword (32 bits)
1	1	Reserved (setting prohibited)

- Bit 7—DTC Transfer Mode Select (DTS): When in repeat mode or block transfer mode, this bit designates whether the source side or destination side will be the repeat area or block area.

Bit 7 (DTS)	Description
0	Destination side is the repeat area or block area
1	Source side is the repeat area or block area

- Bit 6—DTC Chain Enable (CHNE): This bit designates whether to perform continuous DTC data transfers with the same activating source. Continued transfer information is read after the 16th byte from the start address of the previous transfer information.

Bit 6 (CHNE)	Description
0	DTC data transfer end (activation wait state ensues)
1	DTC data transfer continue (read continue register information, execute transfer)

Table 11.10 DMAC Internal Status

Item	Address Reload On	Address Reload Off
SAR	H'FFFF83F0	H'FFFF83F4
DAR	H'FFFFF004	H'FFFFF004
DMATCR	H'0000007C	H'0000007C
Bus rights	Released	Maintained
DMAC operation	Halted	Processing continues
Interrupts	Not issued	Not issued
Transfer request source flag clear	Executed	Not executed

Notes: 1. Interrupts are executed until the DMATCR value becomes 0, and if the IE bit of the CHCR is set to 1, are issued regardless of whether the address reload is on or off.
2. If transfer request source flag clears are executed until the DMATCR value becomes 0, they are executed regardless of whether the address reload is on or off.
3. Designate burst mode when using the address reload function. There are cases where abnormal operation will result if it is executed in cycle steal mode.
4. Designate a multiple of four for the TCR value when using the address reload function. There are cases where abnormal operation will result if anything else is designated.

To execute transfers after the fifth one when the address reload is on, make the transfer request source issue another transfer request signal.

11.4.4 Example of DMA Transfer between A/D Converter and Internal Memory (Address Reload On) (A Mask)

In this example the on-chip A/D converter (A/D1) is the transfer source and the internal memory is the transfer destination, and the address reload on.

Table 11.11 indicates the transfer conditions and the setting values of each of the registers.

- Bits 3–0—I/O Control A3–A0 (IOA3–IOA0): These bits set the TGR1A register function.

Bit 3: IOA3	Bit 2: IOA2	Bit 1: IOA1	Bit 0: IOA0	Description		
0	0	0	0	TGR1A	Output disabled (initial value)	
			1	is an	Initial	Output 0 on compare-match
		1	0	output	output	Output 1 on compare-match
			1	compare	is 0	Toggle output on compare-match
	1	0	0	register	Output disabled	
			1		Initial	Output 0 on compare-match
		1	0		output	Output 1 on compare-match
			1		is 1	Toggle output on compare-match
1	0	0	0	TGR1A	Capture	Input capture on rising edge
			1	is an	input source	Input capture on falling edge
		1	0	input	is the	Input capture on both edges
			1	capture	TIOC1A pin	
	1	0	0	register	Capture input	Input capture
			1		source is TGR0A	on channel 0/TGR0A
		1	0		compare-match/input	compare-match/input capture generation
			1		capture	

12.5 Interrupts

12.5.1 Interrupt Sources and Priority Ranking

The MTU has three interrupt sources: TGR register compare-match/input captures, TCNT counter overflows and TCNT counter underflows. Because each of these three types of interrupts are allocated its own dedicated status flag and enable/disable bit, the issuing of interrupt request signals to the interrupt controller can be independently enabled or disabled.

When an interrupt source is generated, the corresponding status flag in the timer status register (TSR) is set to 1. If the corresponding enable/disable bit in the timer input enable register (TIER) is set to 1 at this time, the MTU makes an interrupt request of the interrupt controller. The interrupt request is canceled by clearing the status flag to 0.

The channel priority order can be changed with the interrupt controller. The priority ranking within a channel is fixed. For more information, see section 6, Interrupt Controller (INTC).

Table 12.17 lists the MTU interrupt sources.

Input Capture/Compare Match Interrupts: If the TGIE bit of the timer input enable register (TIER) is already set to 1 when the TGF flag in the timer status register (TSR) is set to 1 by a TGR register input capture/compare-match of any channel, an interrupt request is sent to the interrupt controller. The interrupt request is canceled by clearing the TGF flag to 0. The MTU has 16 input capture/compare-match interrupts; four each for channels 0, 3, and 4, and two each for channels 1 and 2.

Overflow Interrupts: If the TCIEV bit of the TIER is already set to 1 when the TCFV flag in the TSR is set to 1 by a TCNT counter overflow of any channel, an interrupt request is sent to the interrupt controller. The interrupt request is canceled by clearing the TCFV flag to 0. The MTU has five overflow interrupts, one for each channel.

Underflow Interrupts: If the TCIEU bit of the TIER is already set to 1 when the TCFU flag in the TSR is set to 1 by a TCNT counter underflow of any channel, an interrupt request is sent to the interrupt controller. The interrupt request is canceled by clearing the TCFU flag to 0. The MTU has two underflow interrupts, one each for channels 1 and 2.

12.7.4 Contention between TCNT Write and Increment

If a count-up signal is issued in the T_2 state during the TCNT write cycle, TCNT write has priority, and the counter is not incremented (figure 12.78).

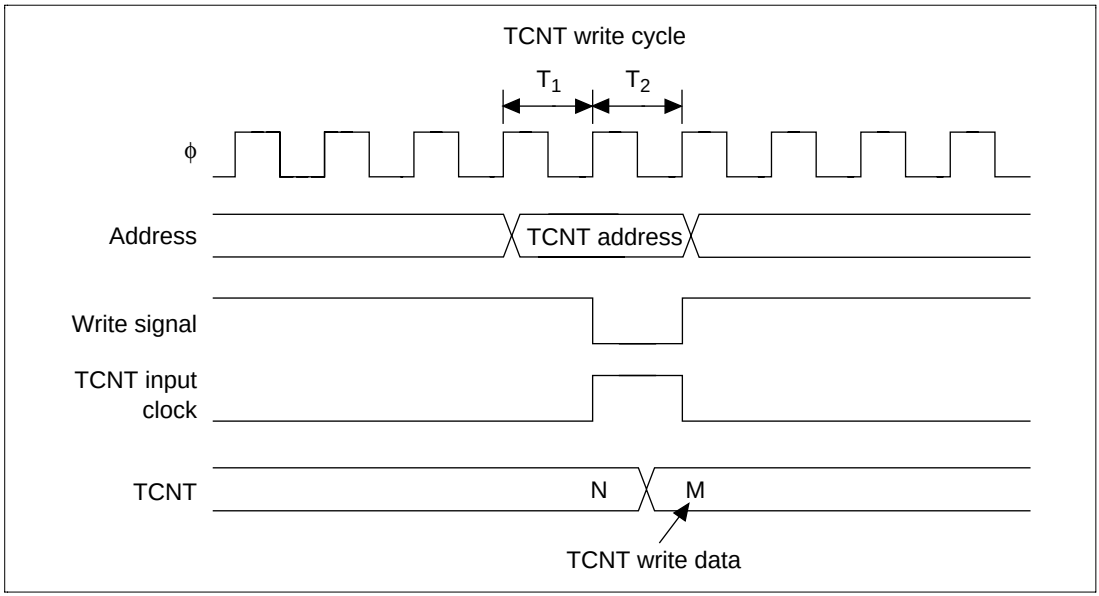


Figure 12.78 TCNT Write and Increment Contention

When setting the buffer operation in the reset synchronous PWM mode, it is not necessary to set the timer interrupt enable register's (TIER4) TGIEC and TGIED bits to 0, to prohibit interrupt output.

Figure 12.88 shows an example of operations for TGR3, TGR4, TIOC3, and TIOC4, with TMDR3's BFA and BFB bits set to 1, and TMDR4's BFA and BFB bits set to 0.

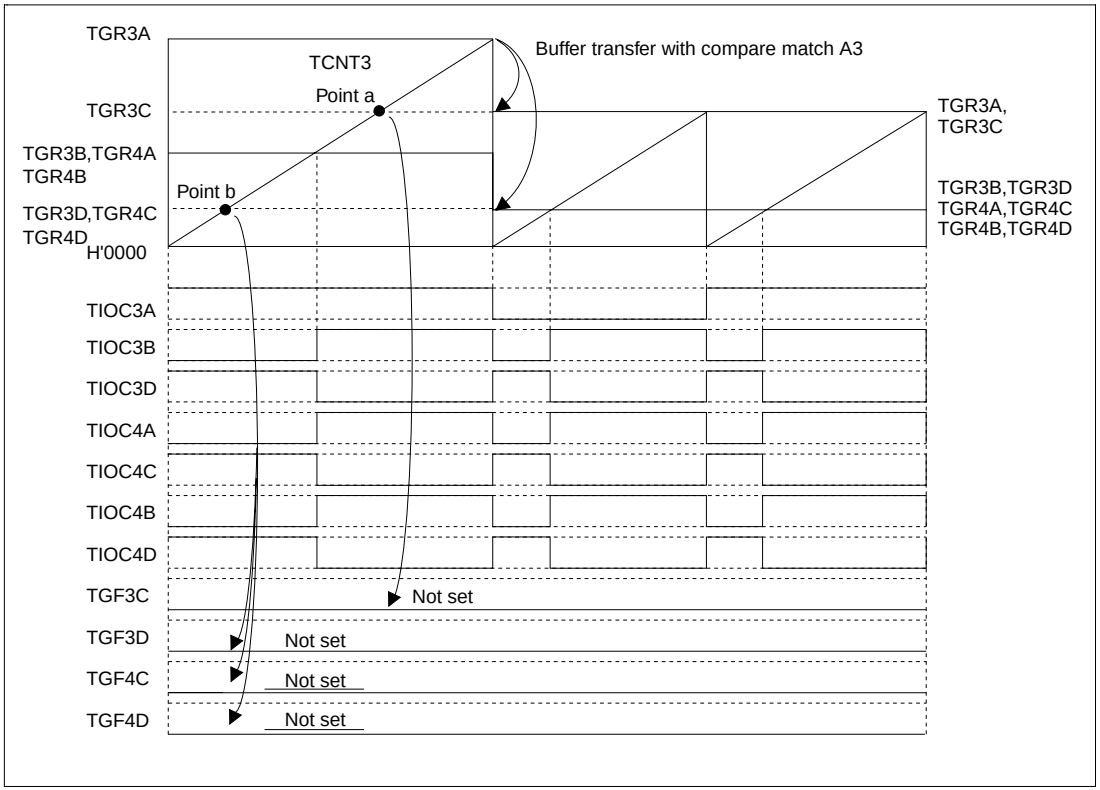


Figure 12.88 Buffer Operation and Compare-Match Flags in Reset Sync PWM Mode (for A Mask)

12.7.14 Overflow Flags in Reset Sync PWM Mode

When set to reset sync PWM mode, TCNT3 and TCNT4 start counting when the CST3 bit of TSTR is set to 1. At this point, TCNT4's count clock source and count edge obey the TCR3 setting.

In reset sync PWM mode, with cycle register TGR3A's set value at H'FFFF, take care when specifying TGR3A compare-match for the counter clear source, since the operation of the overflow flag (TCFV bit) differs with TSR3 and TSR4.

(12) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Reset-Synchronous PWM Mode: Figure 12.107 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in reset-synchronous PWM mode after re-setting.

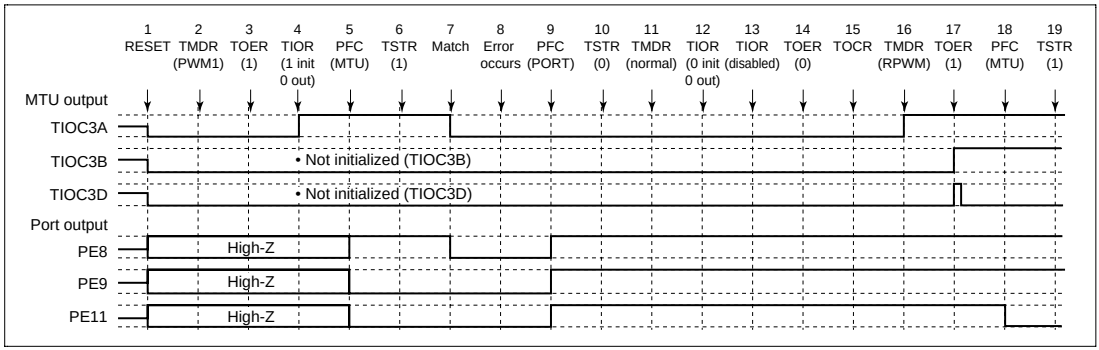


Figure 12.107 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronous PWM Mode

1 to 14 are the same as in figure 12.106.

15. Select the reset-synchronous PWM output level and cyclic output enabling/disabling with TOCR.
16. Set reset-synchronous PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU output with the PFC.
19. Operation is restarted by TSTR.

12.11.2 Output-Level Compare Operation

Figure 12.127 shows an example of the output-level compare operation for the combination of PE09/TIOC3B and PE11/TIOC3D. The operation is the same for the other pin combinations.

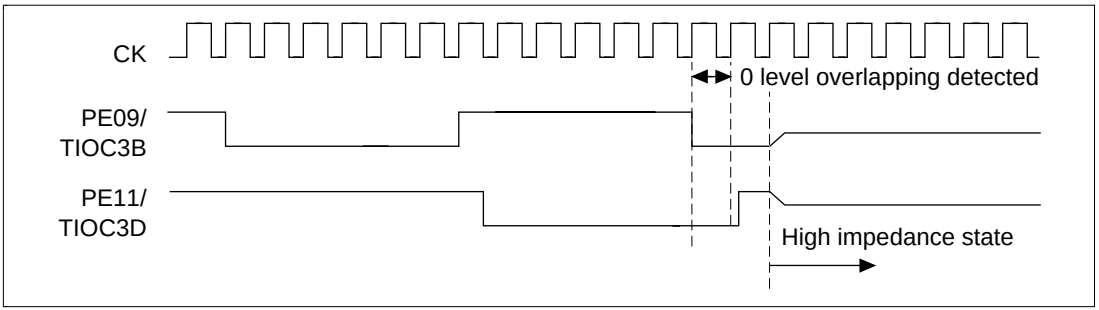


Figure 12.127 Output-Level Detection Operation

12.11.3 Release from High-Impedance State

High-current pins that have entered high-impedance state due to input-level detection can be released either by returning them to their initial state with a power-on reset, or by clearing all of the bit 12–15 (POE0F–POE3F) flags of the ICSR. High-current pins that have become high-impedance due to output-level detection can be released either by returning them to their initial state with a power-on reset, or by first clearing bit 9 (OCE) of the OCSR to disable output-level compares, then clearing the bit 15 (OSF) flag. However, when returning from high-impedance state by clearing the OSF flag, always do so only after outputting a high level from the high-current pins (TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D). High-level outputs can be achieved by setting the MTU internal registers. See section 12.2, MTU Register Descriptions, for details.

13.3.4 Timing of Setting the Overflow Flag (OVF)

In the interval timer mode, when the TCNT overflows, the OVF flag of the TCSR is set to 1 and an interval timer interrupt is simultaneously requested (figure 13.6).

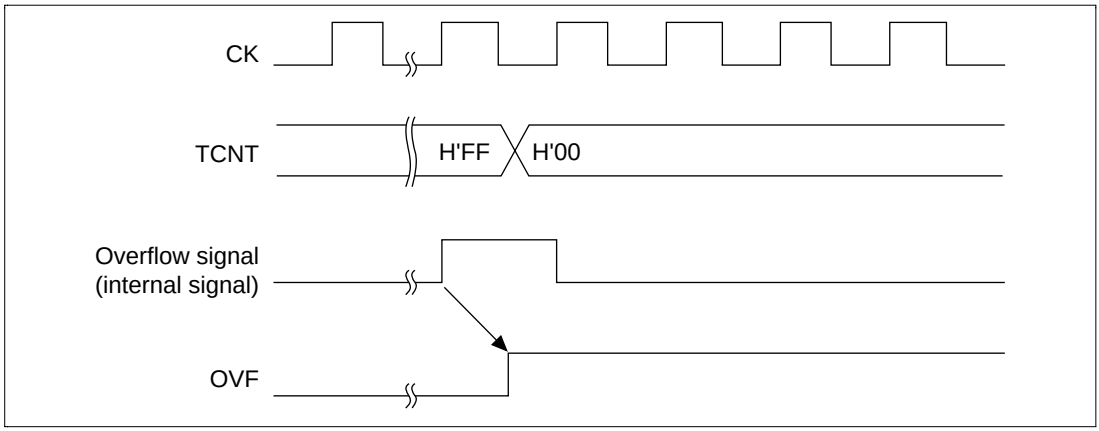


Figure 13.6 Timing of Setting the OVF

13.3.5 Timing of Setting the Watchdog Timer Overflow Flag (WOVF)

When the TCNT overflows in the watchdog timer mode, the WOVF bit of the RSTCSR is set to 1 and a $\overline{\text{WDTOVF}}$ signal is output. When the RSTE bit is set to 1, TCNT overflow enables an internal reset signal to be generated for the entire chip (figure 13.7).

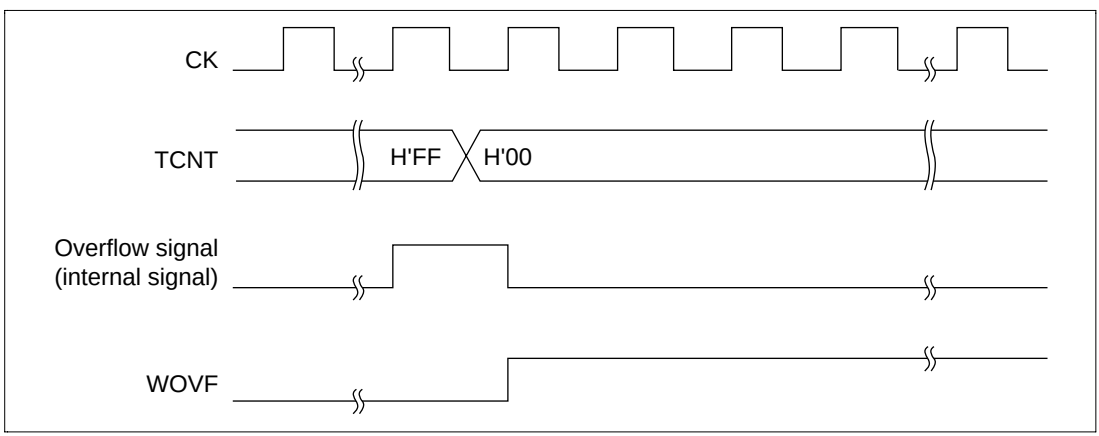


Figure 13.7 Timing of Setting the WOVF Bit

Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)

Bit Rate (Bits/s)	φ (MHz)								
	22			22.1184			24		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	97	–0.35	3	97	0.19	3	106	–0.44
150	3	71	–0.54	3	71	0.00	3	77	0.16
300	2	142	0.16	2	143	0.00	2	155	0.16
600	2	71	–0.54	2	71	0.00	2	77	0.16
1200	1	142	0.16	1	143	0.00	1	155	0.16
2400	1	71	–0.54	1	71	0.00	1	77	0.16
4800	0	142	0.16	0	143	0.00	0	155	0.16
9600	0	71	–0.54	0	71	0.00	0	77	0.16
14400	0	47	–0.54	0	47	0.00	0	51	0.16
19200	0	35	–0.54	0	35	0.00	0	38	0.16
28800	0	23	–0.54	0	23	0.00	0	25	0.16
31250	0	21	0.00	0	21	0.54	0	23	0.00
38400	0	17	–0.54	0	17	0.00	0	19	–2.34

Section 15 High Speed A/D Converter (Excluding A Mask)

15.1 Overview

The high speed A/D converter has 10-bit resolution, and can select from a maximum of eight channels of analog inputs.

15.1.1 Features

The high speed A/D converter has the following features:

- 10-bit resolution
- Eight input channels
- Analog conversion voltage range setting is selectable
  - Using the reference voltage pin (AVref) as an analog standard voltage (Vref), conversion of analog input from 0 to Vref (only with SH7043).
- High-speed conversion
  - Minimum conversion time: 2.9 µs per channel (for 28-MHz operation)
  - 1.4 µs per channel during continuous conversion
- Multiple conversion modes
  - Select mode/group mode
  - Single mode/scan mode
  - Buffered operation possible
  - 2 channel simultaneous sampling possible
- Three types of conversion start
  - Software, timer conversion start trigger (MTU), or $\overline{\text{ADTRG}}$ pin can be selected.
- Eight data registers
  - Conversion results stored in 16-bit data registers corresponding to each channel.
- Sample and hold function
- A/D conversion end interrupt generation
  - An A/D conversion end interrupt (ADI) request can be generated on completion of A/D conversions

Port A Control Register L2 (PACRL2):

Bit:	15	14	13	12	11	10	9	8
	PA7 MD1	PA7 MD0	PA6 MD1	PA6 MD0	PA5 MD1	PA5 MD0	—	PA4MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit:	7	6	5	4	3	2	1	0
	—	PA3MD	PA2 MD1	PA2 MD0	—	PA1MD	—	PA0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R	R/W

- Bits 15 and 14—PA7 Mode 1, 0 (PA7MD1 and PA7MD0): These bits select the function of the PA7/TCLKB/$\overline{CS3}$ pin.

Bit 15: PA7MD1	Bit 14: PA7MD0	Description
0	0	General input/output (PA7) (initial value)
	1	MTU timer clock input (TCLKB)
1	0	Chip select output ($\overline{CS3}$) (PA7 in single chip mode)
	1	Reserved

- Bits 13 and 12—PA6 Mode 1, 0 (PA6MD1 and PA6MD0): These bits select the function of the PA6/TCLKA/$\overline{CS2}$ pin.

Bit 13: PA6MD1	Bit 12: PA6MD0	Description
0	0	General input/output (PA6) (initial value)
	1	MTU timer clock input (TCLKA)
1	0	Chip select output ($\overline{CS2}$) (PA6 in single chip mode)
	1	Reserved

FLMCRn. The time during which the Pn bit is set is the flash memory programming time. Set 200 µs as the time for one programming operation.

22.7.2 Program-Verify Mode (n = 1 for Addresses H'0000–H'1FFFF, n = 2 for Addresses H'20000–H'3FFFF)

In program-verify mode, the data written in program mode is read to check whether it has been correctly written in the flash memory.

After the elapse of a given programming time, the programming mode is exited (the Pn bit in FLMCRn is released, then the PSUn bit is released at least 10 µs later). The watchdog timer is released after the elapse of 10 µs or more, and the operating mode is switched to program-verify mode by setting the PVn bit in FLMCRn. Before reading in program-verify mode, a dummy write of H'FF data should be made to the addresses to be read. The dummy write should be executed after the elapse of 4 µs or more. When the flash memory is read in this state (verify data is read in 32-bit units), the data at the latched address is read. Wait at least 2 µs after the dummy write before performing this read operation. Next, the written data is compared with the verify data, and reprogram data is computed (see figure 22.13) and transferred to the reprogram data area. After 32 bytes of data have been verified, exit program-verify mode, wait for at least 4 µs, then release the SWE bit in FLMCR1. If reprogramming is necessary, set program mode again, and repeat the program/program-verify sequence as before. However, ensure that the program/program-verify sequence is not repeated more than 1,000 times on the same bits.

```
;
        MOV.L     #Wait10u,R3
        MOV.L     #FLMCR1,R0
        OR.B      #SWESET,@(R0,GBR)       ; Set SWE
EWait_1 SUBC      R2,R3                   ; Wait 10 µs
        BF        EWait_1
;
        MOV.L     #0,R9                   ; Initialize n (R9) to 0
;
        MOV.B     @(6,R5),R0
        MOV.B     R0,@(EBR1,GBR)          ; Erase memory block (EBR1) setting
        MOV.B     @(7,R5),R0
        MOV.B     R0,@(EBR2,GBR)          ; Erase memory block (EBR2) setting
;
        MOV.L     #FLMCR1,R0
        MOV.L     @R5,R6                  ; Erase memory block start address -> R6
        MOV.L     #H'020000,R7
        CMP/GT    R6,R7
        BT        EraseLoop
        MOV.L     #FLMCR2,R0
;
EraseLoop         .EQU     $
        MOV.L     #WDT_TCSR,R1            ; Enable WDT
        MOV.W     #WDT_9m,R3              ; 9.2 ms cycle
        MOV.W     R3,@R1
;
        MOV.L     #Wait200u,R3
        OR.B      #ESUSET,@(R0,GBR)       ; Set ESU
EWait_2 SUBC      R2,R3                   ; Wait 200 µs
        BF        EWait_2
;
        MOV.L     #Wait5m,R3
        OR.B      #ESET,@(R0,GBR)         ; Set E
EWait_3 SUBC      R2,R3                   ; Wait 5 ms
        BF        EWait_3
;
        MOV.L     #Wait10u,R3
```

26.3.5 Multifunction Timer Pulse Unit Timing

Table 26.9 Multifunction Timer Pulse Unit Timing (Conditions: V_{CC} = 3.0* to 3.6V, AV_{CC} = 3.0* to 3.6V, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 3.0* to AV_{CC}, V_{SS} = AV_{SS} = 0V, T_a = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
Output compare output delay time	t_{TOCD}	—	100	ns	26.23
Input capture input setup time	t_{TICS}	100	—	ns	
Timer input setup time	t_{TCKS}	100	—	ns	26.24
Timer clock pulse width (single edge specification)	$t_{TCKWH/L}$	1.5	—	t_{cyc}	
Timer clock pulse width (both edges specified)	$t_{TCKWH/L}$	2.5	—	t_{cyc}	
Timer clock pulse width (phase measurement mode)	$t_{TCKWH/L}$	2.5	—	t_{cyc}	

Note: * SH7042/43 ZTAT (excluding A mask) are 3.2V.

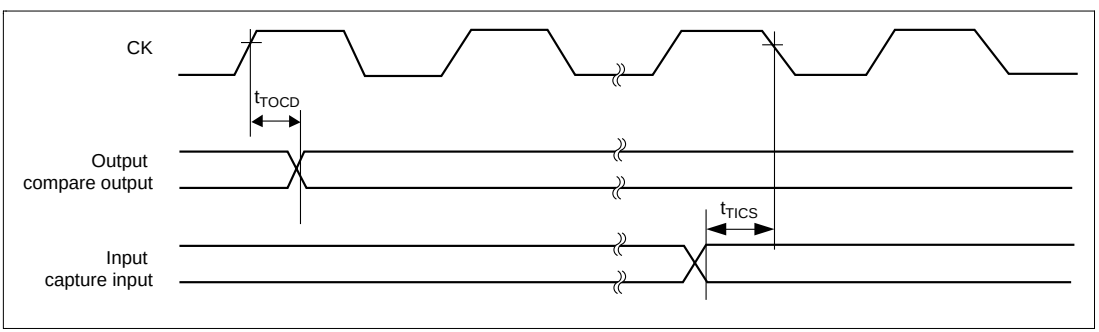


Figure 26.23 MTU I/O Timing

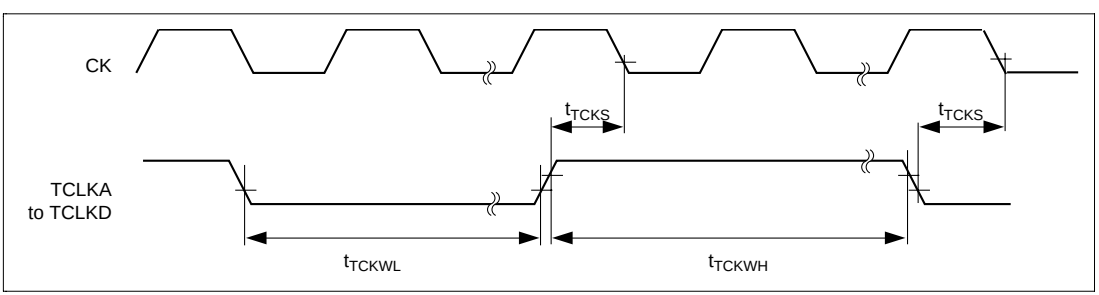


Figure 26.24 MTU Clock Input Timing

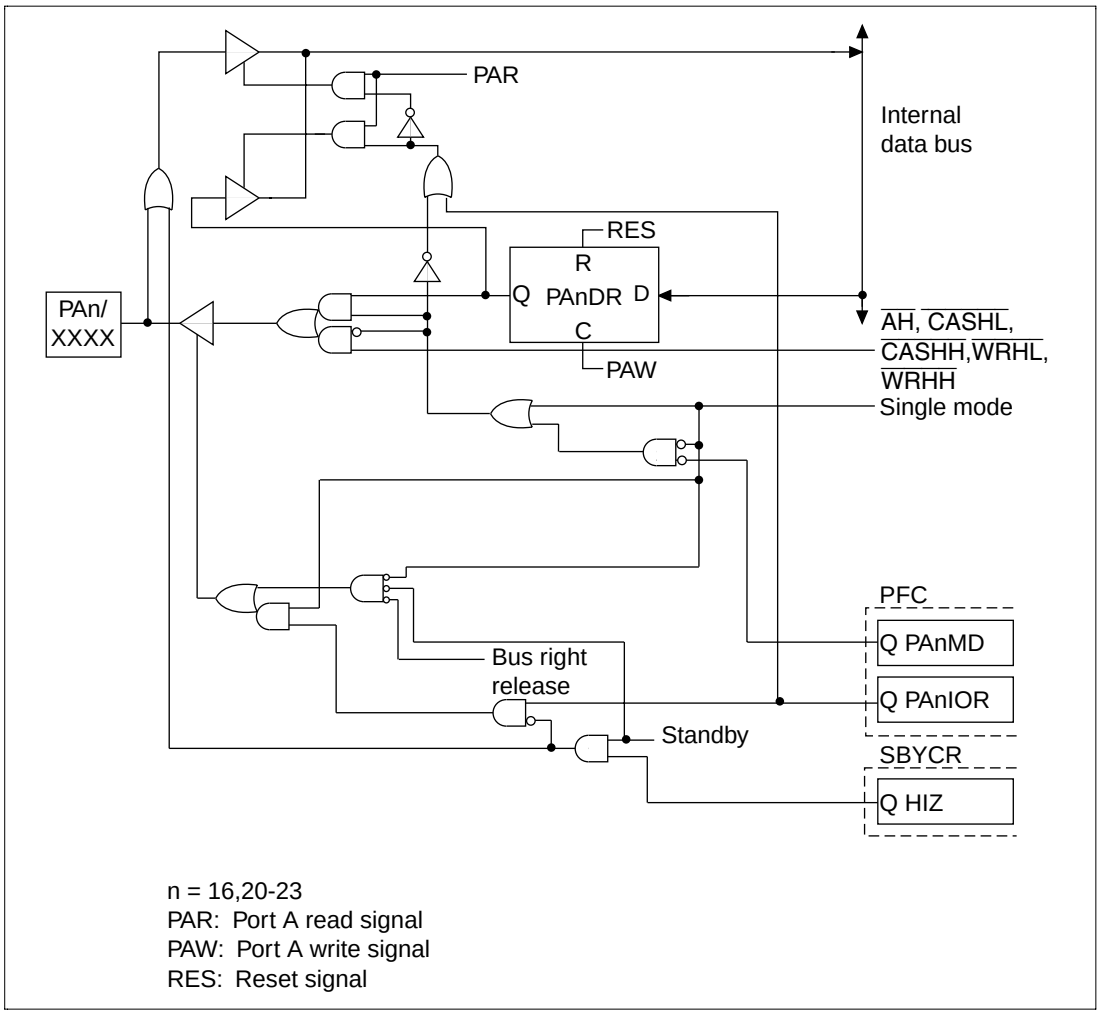


Figure B.12 PAn/XXXX Block Diagram

Appendix E Product Code Lineup

Table E.1 SH7040, SH7041, SH7042, SH7043, SH7044, and SH7045 Product Lineup

Product Type		Mask Version	Product Code	Mark Code	Package	Order Model No.*2
SH7040A	Mask ROM verion	A MASK	HD6437040AF28	HD6437040A (***)F28	QFP2020-112	HD6437040A***F
			HD6437040AVF16	HD6437040A(***)VF16	QFP2020-112	HD6437040A***F
			HD6437040AVX16	HD6437040A(***)VX16	TQFP1414-120	HD6437040A***X
			HD6437040ACF28	HD6437040A(***)CF28	QFP2020-112Cu*1	HD6437040A***CF
			HD6437040AVCF16	HD6437040A(***)VCF16	QFP2020-112Cu*1	HD6437040A***CF
	ROM less version	A MASK	HD6417040AF28	HD6417040AF28	QFP2020-112	HD6417040AF28
			HD6417040AVF16	HD6417040AVF16	QFP2020-112	HD6417040AVF16
			HD6417040AVX16	HD6417040AVX16	TQFP1414-120	HD6417040AVX16
			HD6417040ACF28	HD6417040ACF28	QFP2020-112Cu*1	HD6417040ACF28
			HD6417040AVCF16	HD6417040AVCF16	QFP2020-112Cu*1	HD6417040AVCF16
SH7041A	Mask ROM version	A MASK	HD6437041AF28	HD6437041A(***)F28	QFP2020-144	HD6437041A***F
			HD6437041AVF16	HD6437041A(***)VF16	QFP2020-144	HD6437041A***F
			HD6437041ACF28	HD6437041A(***)CF28	QFP2020-144Cu*1	HD6437041A***CF
			HD6437041AVCF16	HD6437041A(***)VCF16	QFP2020-144Cu*1	HD6437041A***CF
	ROM less verion	A MASK	HD6417041AF28	HD6417041AF28	QFP2020-144	HD6417041AF28
			HD6417041AVF16	HD6417041AVF16	QFP2020-144	HD6417041AVF16
			HD6417041ACF28	HD6417041ACF28	QFP2020-144Cu*1	HD6417041ACF28
			HD6417041AVCF16	HD6417041AVCF16	QFP2020-144Cu*1	HD6417041AVCF16
SH7042	Mask ROM version	–	HD6437042F28	HD6437042 (***)F28	QFP2020-112	HD6437042***F
			HD6437042VF16	HD6437042 (***)VF16	QFP2020-112	HD6437042***F
	Z-TAT version	–	HD6477042F28	HD6477042F28	QFP2020-112	HD6477042F28
			HD6477042VF16	HD6477042VF16	QFP2020-112	HD6477042VF16
SH7042A	Mask ROM version	A MASK	HD6437042AF28	HD6437042A(***)F28	QFP2020-112	HD6437042A***F
			HD6437042AVF16	HD6437042A(***)VF16	QFP2020-112	HD6437042A***F
			HD6437042AVX16	HD6437042A(***)VX16	TQFP1414-120	HD6437042A***X
			HD6437042ACF28	HD6437042A(***)CF28	QFP2020-112Cu*1	HD6437042A***CF
			HD6437042AVCF16	HD6437042A(***)VCF16	QFP2020-112Cu*1	HD6437042A***CF