Renesas - HD6417040ACFI28V Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit
Speed	28MHz
Connectivity	EBI/EMI, SCI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	74
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417040acfi28v

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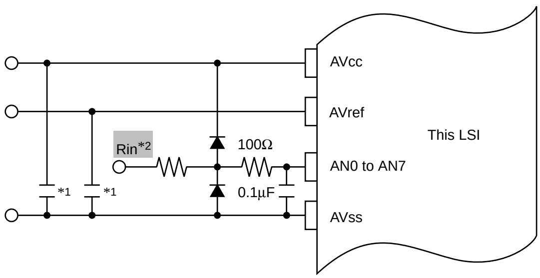
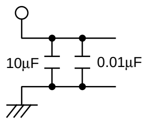


Notes: Numbers are only to be noted as reference value
*1


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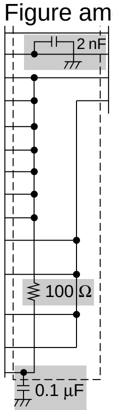
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Table 1.3 Pin Arrangement by Mode for SH7040, SH7042 (TQFP-120 Pin) (cont)

TQFP120 Pin No.	MCU Mode	PROM Mode
63	PD10/D10	NC
64	PD9/D9	NC
65	PD8/D8	NC
66	V_{SS}	V_{SS}
67	PD7/D7	D7
68	PD6/D6	D6
69	PD5/D5	D5
70	V_{CC}	V_{CC}
71	PD4/D4	D4
72	PD3/D3	D3
73	PD2/D2	D2
74	PD1/D1	D1
75	PD0/D0	D0
76	V_{SS}	V_{SS}
77	XTAL	NC
78	MD3	V_{CC}
79	EXTAL	V_{SS}
80	MD2	V_{CC}
81	NMI	A9
82	V_{CC}	V_{CC}
83	MD1	V_{CC}
84	MD0	V_{CC}
85	$PLLV_{CC}$	V_{CC}
86	PLLCAP	V_{SS}
87	$PLLV_{SS}$	V_{SS}
88	PA15/CK	NC
89	$\overline{RES}$	V_{PP}
90	NC	NC
91	NC	NC
92	PE0/TIOC0A/$\overline{DREQ0}$	NC
93	PE1/TIOC0B/$\overline{DRAK0}$	NC

CPU returns to ordinary program execution state through the exception processing state after the oscillator stabilization time has elapsed. In this mode, power consumption drops markedly, since the oscillator stops (table 2.18).

Table 2.18 Power-Down State

		State						
Mode	**Transition Conditions**	**Clock**	**CPU**	**On-Chip Peripheral Modules**	**CPU Registers**	**On-Chip Cache or On-Chip RAM**	**I/O Port Pins**	**Canceling**
Sleep	Execute SLEEP instruction with SBY bit cleared to 0 in SBYCR	Run	Halt	Run	Held	Held	Held	• Interrupt • DMA address error • Power-on reset • Manual reset
Stand-by	Execute SLEEP instruction with SBY bit set to 1 in SBYCR	Halt	Halt	Halt and initialize*	Held	Held	Held or Hi-Z (select-able)	• NMI interrupt • Power-on reset • Manual reset

Note: * Differs depending on the peripheral module and pin.

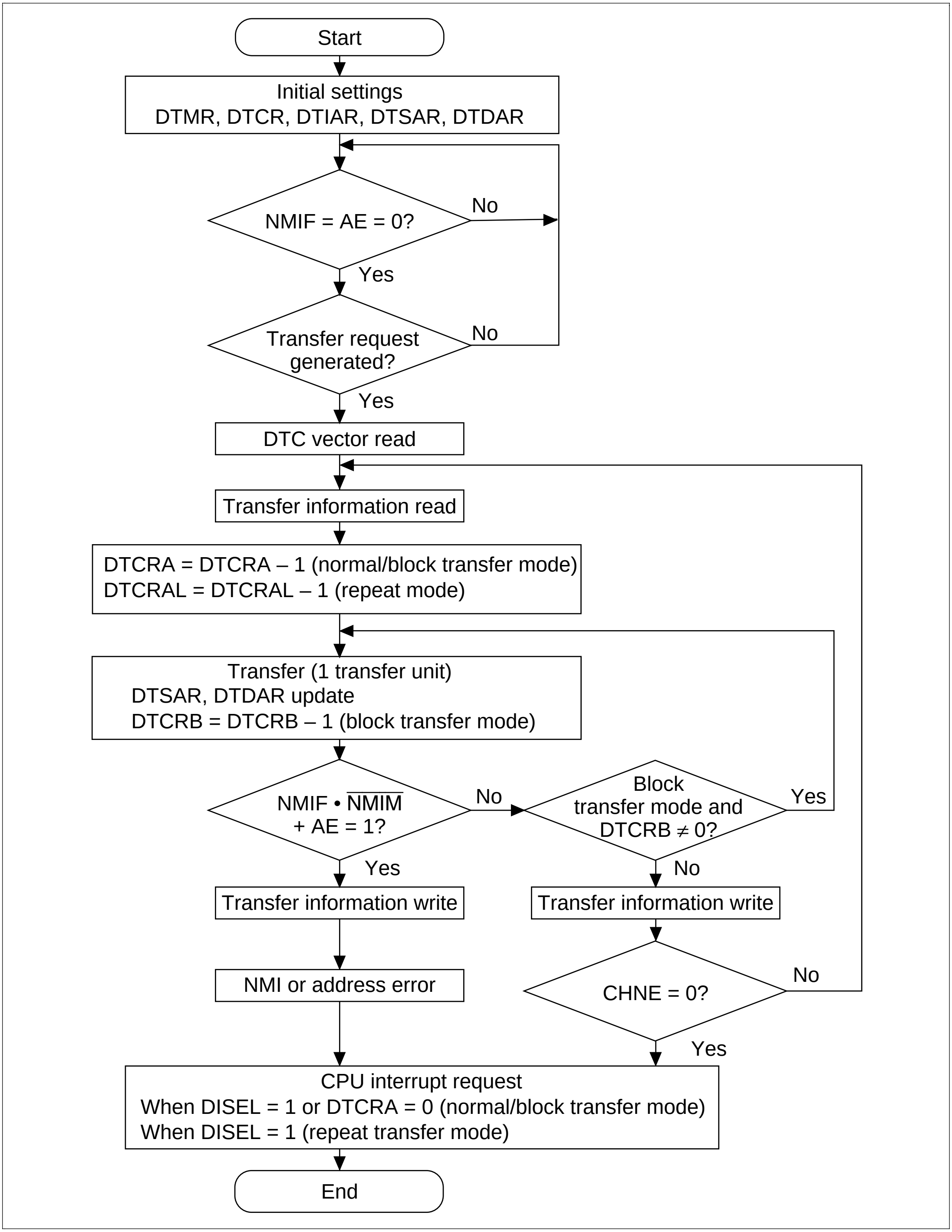


Figure 8.2 DTC Operation Flowchart

12.2.3 Timer I/O Control Register (TIOR)

The TIOR is a register that controls the TGR. The MTU has eight TIOR registers, two each for channels 0, 3, and 4, and one each for channels 1 and 2. TIOR is initialized to H'00 by a power-on reset or the standby mode. Manual reset does not initialize TIOR.

Channels 0, 3, 4: TIOR0H, TIOR3H, TIOR4H

Channels 1, 2: TIOR1, TIOR2:

Bit:	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7–4—I/O Control B3–B0 (IOB3–IOB0): These bits set the TGRB register function.
- Bits 3–0—I/O Control A3–B0 (IOA3–IOA0): These bits set the TGRA register function.

Channels 0, 3, 4: TIOR0L, TIOR3L, TIOR4L:

Bit:	7	6	5	4	3	2	1	0
	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: When the TGRC or TGRD registers are set for buffer operation, these settings become ineffective and the operation is as a buffer register.

- Bits 7–4—I/O Control D3–D0 (IOD3–IOD0): These bits set the TGRD register function.
- Bits 3–0—I/O Control C3–C0 (IOC3–IOC0): These bits set the TGRC register function.

• Bits 3–0—I/O Control C3–C0 (IOC3–IOC0): These bits set the TGR0C register function.

Bit 3: IOC3	Bit 2: IOC2	Bit 1: IOC1	Bit 0: IOC0	Description		
0	0	0	0	TGR0C	Output disabled (initial value)	
			1	is an	Initial	Output 0 on compare-match
		1	0	output	output	Output 1 on compare-match
			1	compare	is 0	Toggle output on compare-match
	1	0	0	register	Output disabled	
			1		Initial	Output 0 on compare-match
		1	0		output	Output 1 on compare-match
			1		is 1	Toggle output on compare-match
1	0	0	0	TGR0C	Capture	Input capture on rising edge
			1	is an	input source	Input capture on falling edge
		1	0	input	is the	Input capture on both edges
			1	capture	TIOC0C pin	
	1	0	0	register	Capture	Input capture
			1		input source	on TCNT1
		1	0		is channel 1/	count up/count down
			1		count clock	

Note: When the BFA bit of TMDR0 is set to 1 and TGR0C is being used as a buffer register, these settings become ineffective and input capture/output compares do not occur.

12.4.9 Complementary PWM Mode

In the complementary PWM mode, three-phase output of non-overlapping positive and negative PWM waveforms can be obtained using channels 3 and 4.

In complementary PWM mode, TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D pins become PWM output pins, the TIOC3A pin can be set for toggle output synchronized with the PWM period. TCNT3 and TCNT4 function as increment/decrement counters.

Table 12.15 shows the PWM output pins used. Table 12.16 shows the settings of the registers.

A function to directly cut off the PWM output by using an external signal is supported as a port function.

Table 12.15 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
3	TIOC3A	Toggle output synchronized with PWM period (or I/O port)
	TIOC3B	PWM output 1
	TIOC3C	I/O port (Avoid setting this pin as a timer I/O pin in the complementary PWM mode.)
	TIOC3D	$\overline{\text{PWM output 1}}$ (non-overlapping negative-phase waveform of PWM output 1)
4	TIOC4A	PWM output 2
	TIOC4B	PWM output 3
	TIOC4C	$\overline{\text{PWM output 2}}$ (non-overlapping negative-phase waveform of PWM output 2)
	TIOC4D	$\overline{\text{PWM output 3}}$ (non-overlapping negative-phase waveform of PWM output 3)

12.7 Notes and Precautions

This section describes contention and other matters requiring special attention during MTU operations.

12.7.1 Input Clock Limitations

The input clock pulse width, in the case of single edge, must be 1.5 states or greater, and 2.5 states or greater for both edges. Normal operation cannot be guaranteed with lesser pulse widths.

In phase counting mode, the phase difference between the two input clocks and the overlap must be 1.5 states or greater for each, and the pulse width must be 2.5 states or greater. Input clock conditions for phase counting mode are shown in figure 12.76.

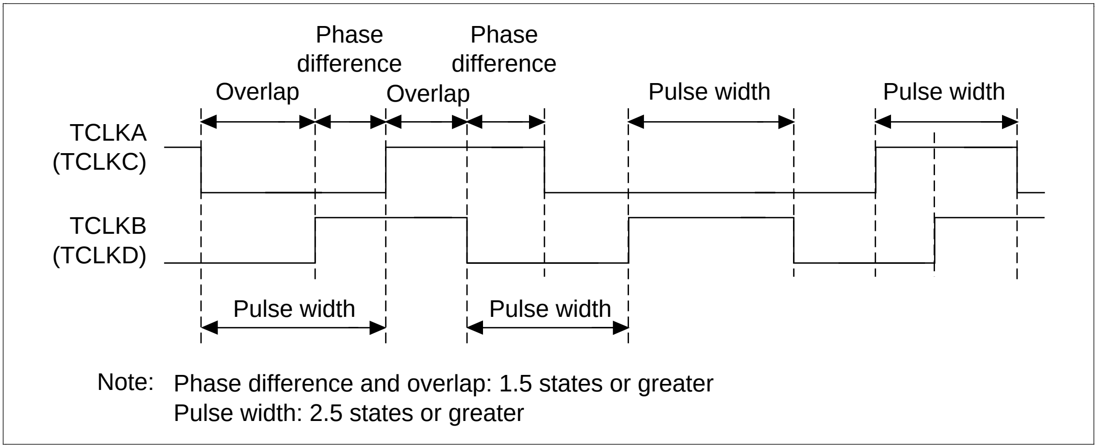


Figure 12.76 Phase Difference, Overlap, and Pulse Width in Phase Count Mode

12.7.2 Note on Cycle Setting

When setting a counter clearing by compare-match, clearing is done in the final state when TCNT matches the TGR value (update timing for count value on TCNT match). The actual number of states set in the counter is given by the following equation:

$$f = \frac{\phi}{(N+1)}$$

(f: counter frequency, ϕ: operating frequency, N: value set in the TGR)

Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)

Bit Rate (Bits/s)	φ (MHz) 12.288			14			14.7456		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	217	0.08	2	248	–0.17	3	64	0.70
150	2	159	0.00	2	181	0.16	2	191	0.00
300	2	79	0.00	2	90	0.16	2	95	0.00
600	1	159	0.00	1	181	0.16	1	191	0.00
1200	1	79	0.00	1	90	0.16	1	95	0.00
2400	0	159	0.00	0	181	0.16	0	191	0.00
4800	0	79	0.00	0	90	0.16	0	95	0.00
9600	0	39	0.00	0	45	–0.93	0	47	0.00
14400	0	26	–1.23	0	29	1.27	0	31	0.00
19200	0	19	0.00	0	22	–0.93	0	23	0.00
28800	0	12	2.56	0	14	1.27	0	15	0.00
31250	0	11	2.40	0	13	0.00	0	14	–1.70
38400	0	9	0.00	0	10	3.57	0	11	0.00

Table 15.1 Pin Configuration

Pin	Abbreviation	I/O	Function
Analog supply	AV_{CC}	I	Analog section power supply
Analog ground	AV_{SS}	I	Analog section ground and A/D conversion reference voltage
Reference voltage	AV_{ref}	I	A/D conversion standard voltage (SH7043 only)
Analog input 0	AN0	I	Analog input channel 0
Analog input 1	AN1	I	Analog input channel 1
Analog input 2	AN2	I	Analog input channel 2
Analog input 3	AN3	I	Analog input channel 3
Analog input 4	AN4	I	Analog input channel 4
Analog input 5	AN5	I	Analog input channel 5
Analog input 6	AN6	I	Analog input channel 6
Analog input 7	AN7	I	Analog input channel 7
A/D external trigger input	$\overline{\text{ADTRG}}$	I	External trigger for A/D conversion start

15.1.4 Register Configuration

Table 15.2 shows the configuration of the high speed A/D converter registers.

Table 15.2 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address	Access Size
A/D data register A	ADDRA	R	H'0000	H'FFFF83F0	8,16
A/D data register B	ADDRB	R	H'0000	H'FFFF83F2	
A/D data register C	ADDRC	R	H'0000	H'FFFF83F4	
A/D data register D	ADDRD	R	H'0000	H'FFFF83F6	
A/D data register E	ADDRE	R	H'0000	H'FFFF83F8	
A/D data register F	ADDRF	R	H'0000	H'FFFF83FA	
A/D data register G	ADDRG	R	H'0000	H'FFFF83FC	
A/D data register H	ADDRH	R	H'0000	H'FFFF83FE	
A/D control/status register	ADCSR	R/(W)*	H'00	H'FFFF83E0	
A/D control register	ADCR	R/W	H'00	H'FFFF83E1	

Note: * Only 0 can be written to bit 7 to clear the flag.

When the DTC or DMAC are activated by an ADI interrupt, the ADF flag is cleared to 0 when the final specified data register is read.

Table 15.9 High Speed A/D Converter Interrupt Sources

Interrupt Source	Description	DTC, DMAC Activation
ADI	Interrupt caused by conversion end	Possible

15.6 Notes on Use

Take note of the following for the A/D converter.

1. Analog input voltage range

   During A/D conversions, see that the voltage applied to the analog input pins AN0–AN7 is within the range Avss ≤ AN0–AN7 ≤ AVcc.

2. AVcc and AVss input voltages

   The AVcc and AVss input voltage must be AVcc = Vcc ± 10%, AVss = Vss. When not using the A/D converter, use AVcc = Vcc, AVss = Vss. During the standby mode, use V_{RAM} ≤ Avcc ≤ 5.5V, AVss = Vss. V_{RAM} is the RAM standby voltage.

3. AVref input voltage

   The analog standard voltage AVref (AV_{ref}) must be Avref ≤ AVcc. When not using the A/D converter, use AV_{ref} = Vcc. During the standby mode, use V_{RAM} ≤ AVref ≤ AVcc. V_{RAM} is the RAM standby voltage.

4. Input ports

   The time constant for the circuit connecting to the input port must be shorter than the sampling time of the A/D converter. Input voltage may not be sampled sufficiently when the time constant of the circuit is long.

5. Conversion start modes

   Depending on the PWR bit setting, the demand for A/D conversion will differ for the high-speed start mode and low-demand conversion mode.

6. Analog input pins handling

   Connect a protection circuit as shown in figure 15.14 to prevent analog input pins (AN0–AN7) from being destroyed due to abnormal voltage from surge, etc. This circuit is also equipped with a CR filter to control errors due to noise. The circuit shown in the diagram is only an example and the number of circuits is to be determined by considering the actual condition of use.

   Figure 15.15 shows an equivalent circuit of analog input pins and table 15.10 shows the specification of the analog input pins.

Table 15.10 Analog Input Pin Specification

Item	Min	Max	Unit
Analog input capacity	—	20	pF
Permitted source impedance	—	1	kΩ

Section 16 Mid-Speed A/D Converter (A Mask)

16.1 Overview

The mid-speed A/D converter has 10 bit resolution, and can select from a maximum of eight channels of analog input.

The mid-speed A/D converter is structured by two independent modules (A/D0 and A/D1)

16.1.1 Features

The mid-speed A/D converter has the following features:

- 10-bit resolution
- Eight input channels (four channels times two)
- Analog conversion voltage range setting is selectable
  — Using the standard voltage pin (AVref) as an analog standard voltage (Vref), conversion of analog input from 0V to Vref (only with SH7041A, SH7043A, and SH7045).
  (Connected to AV_{CC} internally in the SH7040A, SH7042A, and SH7044.)
- High speed conversion
  — Minimum conversion time: per channel
  — Operation frequency: f≤20MHz, CKS=0, 1
  6.7μs (20MHz, CKS=1)
  — Operation frequency: f>20MHz, CKS=0
  9.3μs (28.7MHz, CKS=0)
- Multiple conversion modes
  — Single mode/scan mode
  — 2 channel simultaneous conversion
- Three types of conversion start
  — Software, timer conversion start trigger (MTU), or ADTRG pin can be selected.
- Eight data registers
  — Conversion results stored in 16-bit data registers corresponding to each channel.
- Sample and hold function
- A/D conversion end interrupt generation
  — An A/D conversion end interrupt (ADI) can be generated on completion of A/D conversion.
- Furthermore, ADI0 (A/D0 interrupt request) can activate DTC and ADI1 (A/D1 interrupt request) can activate DMAC.

Table 16.4 A/D Conversion Time (Single Mode)

		CKS=0			CKS=1		
	Notation	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A/D conversion start delay time	t_D	10	—	17	6	—	9
Input sampling time	t_{SPL}	—	64	—	—	32	—
A/D conversion time	t_{CCNV}	259	—	266	131	—	134

Note: Numbers in the table are in states (t_{cyc}).

16.4.4 External Trigger Input Timing

It is possible to start A/D conversion from an external trigger input. External trigger input is input from the $\overline{\text{ADTRG}}$ pin or MTU when the TRGE bit of the A/D control register (ADCR) is set to 1.

A/D conversion is started when the ADST bit of the A/D control/status register (ADCSR) is set to 1 by the $\overline{\text{ADTRG}}$ input pin last transition edge or MTU trigger. Other operations, regardless of whether in the single or scan mode, are the same as when setting the ADST bit to 1 with the software.

Figure 16.6 shows an example of external trigger input timing.

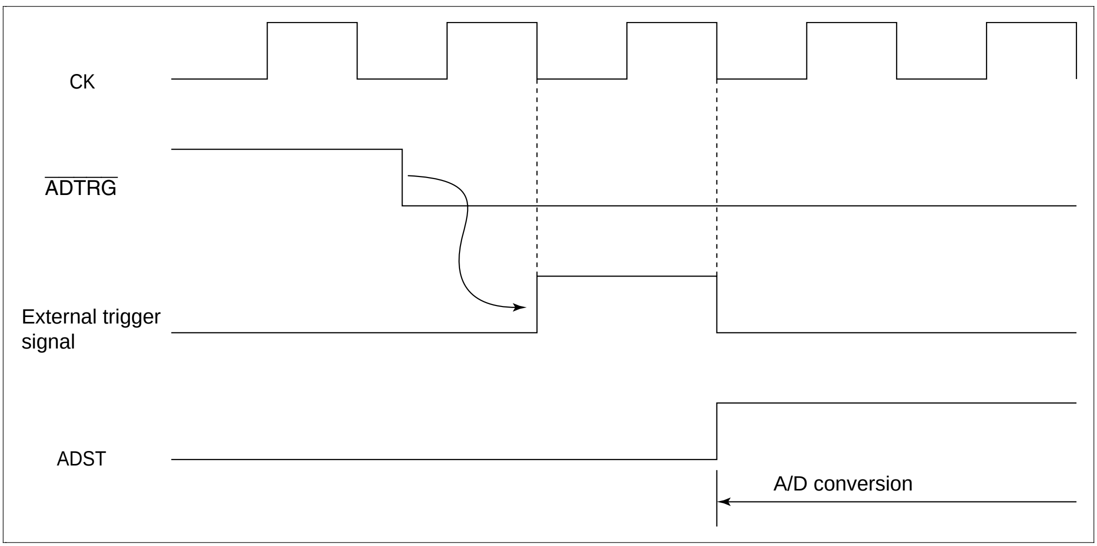


Figure 16.6 External Trigger Input Timing

Table 18.2 Pin Arrangement by Mode (cont)

Pin NO.			Pin Name								
			On-Chip ROM Disabled				On-Chip ROM Enabled				
			MPU Mode0		MPU Mode 1		MPU Mode2		Single Chip Mode		
TFP120	FP144	FP112	Initial Function	PFC Selected Function Possiblilities	Initial Function	PFC Selected Function Possiblilities	Initial Function	PFC Selected Function Possiblilities	Initial Function	PFC Selected Function Possiblilities	PROM Mode
—	127	—	AVREF	AVREF	AVREF	AVREF	AVREF	AVREF	AVREF	AVREF	
98	118	91	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0	VSS
99	119	92	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1	VSS
100	120	93	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2	VSS
101	121	94	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3	VSS
102	122	95	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4	VSS
103	123	96	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5	VSS
105	125	98	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6	VSS
106	126	99	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7	VSS
92	109	85	PE0	PE0/TIOC0A/$\overline{DREQ0}$	PE0	PE0/TIOC0A/$\overline{DREQ0}$	PE0	PE0/TIOC0A/$\overline{DREQ0}$	PE0	PE0/TIOC0A	NC
93	110	86	PE1	PE1/TIOC0B/DRAK0	PE1	PE1/TIOC0B/DRAK0	PE1	PE1/TIOC0B/DRAK0	PE1	PE1/TIOC0B	NC
94	111	87	PE2	PE2/TIOC0C/$\overline{DREQ1}$	PE2	PE2/TIOC0C/$\overline{DREQ1}$	PE2	PE2/TIOC0C/$\overline{DREQ1}$	PE2	PE2/TIOC0C	NC
95	113	88	PE3	PE3/TIOC0D/DRAK1	PE3	PE3/TIOC0D/DRAK1	PE3	PE3/TIOC0D/DRAK1	PE3	PE3/TIOC0D	NC
96	114	89	PE4	PE4/TIOC1A	PE4	PE4/TIOC1A	PE4	PE4/TIOC1A	PE4	PE4/TIOC1A	NC
109	115	102	PE5	PE5/TIOC1B	PE5	PE5/TIOC1B	PE5	PE5/TIOC1B	PE5	PE5/TIOC1B	NC
112	116	104	PE6	PE6/TIOC2A	PE6	PE6/TIOC2A	PE6	PE6/TIOC2A	PE6	PE6/TIOC2A	NC
113	137	105	PE7	PE7/TIOC2B	PE7	PE7/TIOC2B	PE7	PE7/TIOC2B	PE7	PE7/TIOC2B	NC
114	138	106	PE8	PE8/TIOC3A	PE8	PE8/TIOC3A	PE8	PE8/TIOC3A	PE8	PE8/TIOC3A	NC
115	139	107	PE9	PE9/TIOC3B	PE9	PE9/TIOC3B	PE9	PE9/TIOC3B	PE9	PE9/TIOC3B	NC
116	140	108	PE10	PE10/TIOC3C	PE10	PE10/TIOC3C	PE10	PE10/TIOC3C	PE10	PE10/TIOC3C	NC
118	142	110	PE11	PE11/TIOC3D	PE11	PE11/TIOC3D	PE11	PE11/TIOC3D	PE11	PE11/TIOC3D	NC
119	143	111	PE12	PE12/TIOC4A	PE12	PE12/TIOC4A	PE12	PE12/TIOC4A	PE12	PE12/TIOC4A	NC
120	144	112	PE13	PE13/TIOC4B/$\overline{MRES}$	PE13	PE13/TIOC4B/$\overline{MRES}$	PE13	PE13/TIOC4B/$\overline{MRES}$	PE13	PE13/TIOC4B/$\overline{MRES}$	NC
2	2	1	PE14	PE14/TIOC4C/DACK0/$\overline{AH}$	PE14	PE14/TIOC4C/DACK0/$\overline{AH}$	PE14	PE14/TIOC4C/DACK0/$\overline{AH}$	PE14	PE14/TIOC4C	NC
3	5	2	PE15	PE15/TIOC4D/DACK1/$\overline{IRQOUT}$	PE15	PE15/TIOC4D/DACK1/$\overline{IRQOUT}$	PE15	PE15/TIOC4D/DACK1/$\overline{IRQOUT}$	PE15	PE15/TIOC4D	$\overline{CE}$

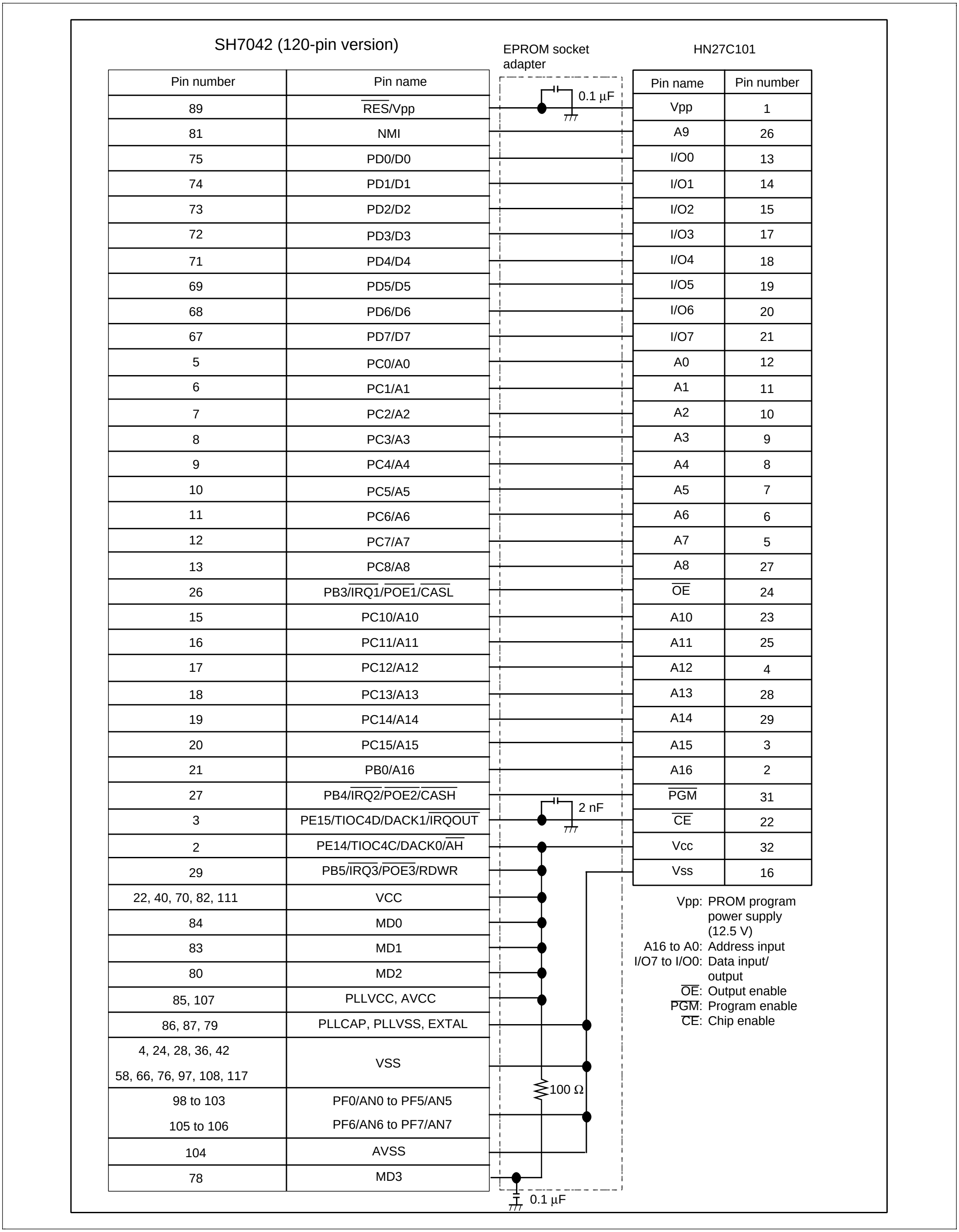


Figure 21.3 SH7042 Pin and HN27C101 Pin Correspondence (120-Pin Version)

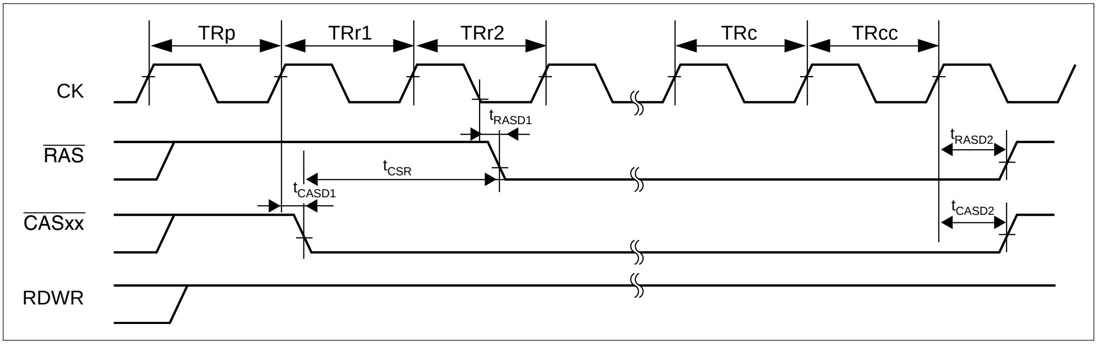


Figure 25.18 Self Refresh

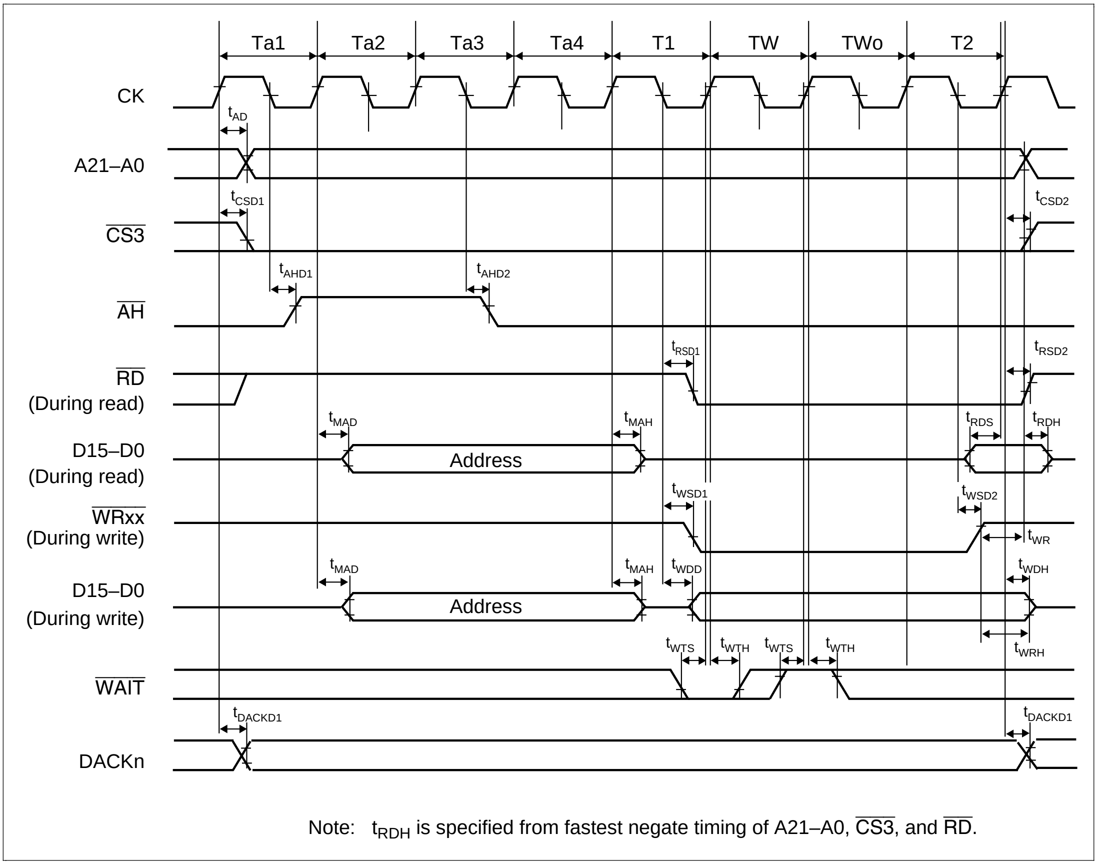


Figure 25.19 Address Data Multiplex I/O Space Cycle (1 Software Wait + External Wait)

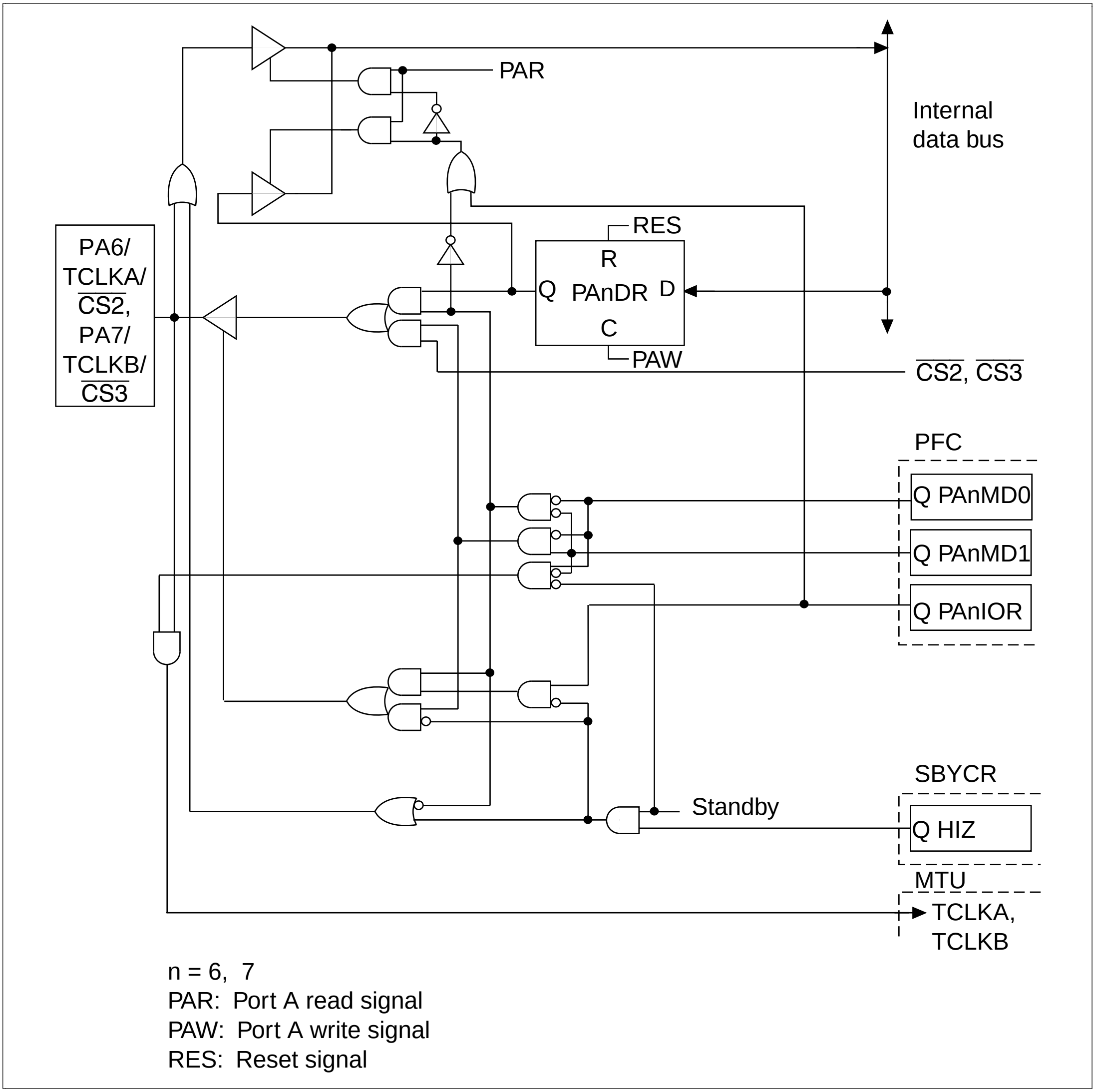
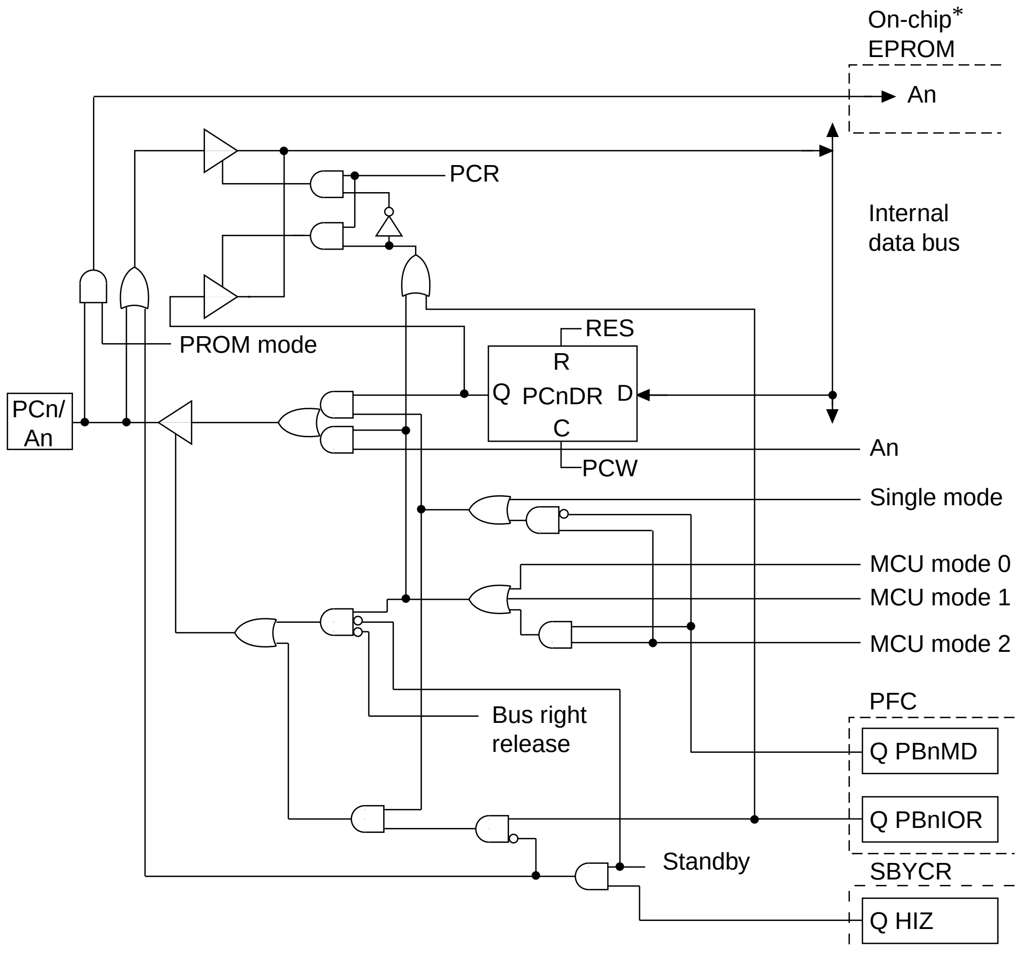


Figure B.3 PA6/TCLKA/$\overline{CS2}$, PA7/TCLKB/$\overline{CS3}$ (ZTAT, Mask) Block Diagram



n = 0–15
PCR: Port C read signal
PCW: Port C write signal
RES: Reset signal

Note: * Not available with the mask versions.

Figure B.22 PCn/An Block Diagram