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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417041acf28v

List of Items Revised or Added for This Version

1.1.1 SH7040 Series Features

Notes on the SH7040 Series Specifications — 7, 9

Type	Abbreviation	Mask Version	On-chip ROM	External Bus Width	A/D Accuracy (5Vversion)	Package	Operating Temp	Frequency	Voltage	Type Name	Notes on the SH7040 Series Specifications: ROM	Notes on the SH7040 Series Specifications: Electrical Characteristics
ZTAT	SH7042		128 kB	16 bits	±15LSB (High-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6477042F28	See "128 kB PROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6477042VF16		
	SH7042A	A mask	128 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6477042AF28	See "128 kB PROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6477042AVF16		
						TQFP1414-120		16 MHz	3.3 V	HD6477042AVX16		
						QFP2020-112Cu*						
								28 MHz	5 V	HD6477042ACF28		
								16 MHz	3.3 V	HD6477042AVCF16		
	SH7043		128 kB	32 bits	±15LSB (High-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6477043F28	See "128 kB PROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6477043VF16		
	SH7043A	A mask	128 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6477043AF28	See "128 kB PROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6477043AVF16		
						QFP2020-144Cu*						
								28 MHz	5 V	HD6477043ACF28		
								16 MHz	3.3 V	HD6477043AVCF16		
FLASH	SH7044F	A mask	256 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD64F7044F28	See "256 kB Flash Memory"	See "Electrical Characteristics"
	SH7045F	A mask	256 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD64F7045F28	See "256 kB Flash Memory"	See "Electrical Characteristics"
MASK	SH7040A	A mask	64 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6437040AF28	See "64 kB Mask ROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6437040AVF16		
						TQFP1414-120		16 MHz	3.3 V	HD6437040AVX16		
						QFP2020-112Cu*						
								28 MHz	5 V	HD6437040ACF28		
								16 MHz	3.3 V	HD6437040AVCF16		
	SH7041A	A mask	64 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6437041AF28	See "64 kB Mask ROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6437041AVF16		
						QFP2020-144Cu*						
								28 MHz	5 V	HD6437041ACF28		
								16 MHz	3.3 V	HD6437041AVCF16		
	SH7042		128 kB	16 bits	±15LSB (High-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6437042F28	See "128 kB Mask ROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6437042VF16		
	SH7042A	A mask	128 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6437042AF28	See "128 kB Mask ROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6437042AVF16		
						TQFP1414-120		16 MHz	3.3 V	HD6437042AVX16		
						QFP2020-112Cu*						
								28 MHz	5 V	HD6437042ACF28		
								16 MHz	3.3 V	HD6437042AVCF16		
	SH7043		128 kB	32 bits	±15LSB (High-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6437043F28	See "128 kB Mask ROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6437043VF16		
	SH7043A	A mask	128 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6437043AF28	See "128 kB Mask ROM"	See "Electrical Characteristics"
								16 MHz	3.3 V	HD6437043AVF16		
						QFP2020-144Cu*						
								28 MHz	5 V	HD6437043ACF28		
								16 MHz	3.3 V	HD6437043AVCF16		
	SH7044	A mask	256 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6437044F28	See "256 kB Mask ROM"	See "Electrical Characteristics"
	SH7045	A mask	256 kB	32bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6437045F28	See "256 kB Mask ROM"	See "Electrical Characteristics"
ROM less	SH7040A	A mask		16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD6417040AF28		See "Electrical Characteristics"
								16 MHz	3.3 V	HD6417040AVF16		
						TQFP1414-120		16 MHz	3.3 V	HD6417040AVX16		
						QFP2020-112Cu*		28 MHz	5 V	HD6417040ACF28		
								16 MHz	3.3 V	HD6417040AVCF16		
	SH7041A	A mask		32 bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD6417041AF28		See "Electrical Characteristics"
								16 MHz	3.3 V	HD6417041AVF16		
						QFP2020-144Cu*						
								28 MHz	5 V	HD6417041ACF28		
								16 MHz	3.3 V	HD6417041AVCF16		

Note: Package with Copper used as the lead material.

1.4 The F-ZTAT Version Onboard Programming

Figure 1.6 Condition Transfer for Flash Memory — 42

Note amended

Notes: For transferring between user mode and user program mode, proceed while CPU is not programming or erasing the flash memory.
* RAM emulation permitted

2.4 Instruction Set by Classification

Table 2.16 Branch Instructions — 70

Table amended

BF/S	label	10001111dddddddd	Delayed branch, if T = 0, disp × 2 + PC → PC; if T = 1, nop	2/1*	—

4.2.3 Notes on Board Design

—

Deleted

4.5 Usage Notes

83 to 85

Newly added

11.1.4 Register Configuration

Table 11.2 DMAC Registers — 218

Note *5 deleted

Type	Abbreviation	Mask Version	On-chip ROM	External Bus Width	A/D Accuracy (5V Version)	Package	Operating Temp	Frequency	Voltage	Type Name	Notes on the SH7040 Series Specifications (For details, see each section in this manual)						
											INTC	DTC	DMAC	MTU	A/D Converter	ROM	Electrical Characteristics
ZTAT	SH7042		128 kB	16 bits	±15LSB (High-Speed)	QFP2020-112	–20°C to 75°C	28 MHz 16 MHz	5 V 3.3 V	HD6477042F28 HD6477042VF16					See “High-Speed A/D Converter”	See “128 kB PROM”	See “Electrical Characteristics”
	SH7042A	A mask	128 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112 TQFP1414-120 QFP2020-112Cu*	–20°C to 75°C	28 MHz 16 MHz 16 MHz 28 MHz 16 MHz	5 V 3.3 V 3.3 V 5 V 3.3 V	HD6477042AF28 HD6477042AVF16 HD6477042AVX16 HD6477042ACF28 HD6477042AVCF16	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “128 kB PROM”	See “Electrical Characteristics”
	SH7043		128 kB	32 bits	±15LSB (High-Speed)	QFP2020-144	–20°C to 75°C	28 MHz 16 MHz	5 V 3.3 V	HD6477043F28 HD6477043VF16					See “High-Speed A/D Converter”	See “128 kB PROM”	See “Electrical Characteristics”
	SH7043A	A mask	128 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144 QFP2020-144Cu*	–20°C to 75°C	28 MHz 16 MHz 28 MHz 16 MHz	5 V 3.3 V 5 V 3.3 V	HD6477043AF28 HD6477043AVF16 HD6477043ACF28 HD6477043AVCF16	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “128 kB PROM”	See “Electrical Characteristics”
FLASH	SH7044F	A mask	256 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112	–20°C to 75°C	28 MHz	5 V	HD64F7044F28	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “256 kB Flash Memory”	See “Electrical Characteristics”
	SH7045F	A mask	256 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144	–20°C to 75°C	28 MHz	5 V	HD64F7045F28	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “256 kB Flash Memory”	See “Electrical Characteristics”
MASK	SH7040A	A mask	64 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112 TQFP1414-120 QFP2020-112Cu*	–20°C to 75°C	28 MHz 16 MHz 16 MHz 28 MHz 16 MHz	5 V 3.3 V 3.3 V 5 V 3.3 V	HD6437040AF28 HD6437040AVF16 HD6437040AVX16 HD6437040ACF28 HD6437040AVCF16	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “64 kB Mask ROM”	See “Electrical Characteristics”
	SH7041A	A mask	64 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144 QFP2020-144Cu*	–20°C to 75°C	28 MHz 16 MHz 28 MHz 16 MHz	5 V 3.3 V 5 V 3.3 V	HD6437041AF28 HD6437041AVF16 HD6437041ACF28 HD6437041AVCF16	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “64 kB Mask ROM”	See “Electrical Characteristics”
	SH7042		128 kB	16 bits	±15LSB (High-Speed)	QFP2020-112	–20°C to 75°C	28 MHz 16 MHz	5 V 3.3 V	HD6437042F28 HD6437042VF16					See “High-Speed A/D Converter”	See “128 kB Mask ROM”	See “Electrical Characteristics”
	SH7042A	A mask	128 kB	16 bits	±4LSB (Mid-Speed)	QFP2020-112 TQFP1414-120 QFP2020-112Cu*	–20°C to 75°C	28 MHz 16 MHz 16 MHz 28 MHz 16 MHz	5 V 3.3 V 3.3 V 5 V 3.3 V	HD6437042AF28 HD6437042AVF16 HD6437042AVX16 HD6437042ACF28 HD6437042AVCF16	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “128 kB Mask ROM”	See “Electrical Characteristics”
	SH7043		128 kB	32 bits	±15LSB (High-Speed)	QFP2020-144	–20°C to 75°C	28 MHz 16 MHz	5 V 3.3 V	HD6437043F28 HD6437043VF16					See “High-Speed A/D Converter”	See “128 kB Mask ROM”	See “Electrical Characteristics”
	SH7043A	A mask	128 kB	32 bits	±4LSB (Mid-Speed)	QFP2020-144 QFP2020-144Cu*	–20°C to 75°C	28 MHz 16 MHz 28 MHz 16 MHz	5 V 3.3 V 5 V 3.3 V	HD6437043AF28 HD6437043AVF16 HD6437043ACF28 HD6437043AVCF16	Change the interrupt vectors related A/D converter	Change the DTER access methods and DTC vectors	Change the setting methods on transfer requests	Change the Usage Notes	See “Mid-Speed A/D Converter”	See “128 kB Mask ROM”	See “Electrical Characteristics”

Word or longword immediate data is not located in the instruction code, but instead is stored in a memory table. An immediate data transfer instruction (MOV) accesses the memory table using the PC relative addressing mode with displacement.

2.3 Instruction Features

2.3.1 RISC-Type Instruction Set

All instructions are RISC type. This section details their functions.

16-Bit Fixed Length: All instructions are 16 bits long, increasing program code efficiency.

One Instruction per Cycle: The microprocessor can execute basic instructions in one cycle using the pipeline system. Instructions are executed in 35 ns at 28.7 MHz.

Data Length: Longword is the standard data length for all operations. Memory can be accessed in bytes, words, or longwords. Byte or word data accessed from memory is sign-extended and handled as longword data. Immediate data is sign-extended for arithmetic operations or zero-extended for logic operations. It also is handled as longword data (table 2.2).

Table 2.2 Sign Extension of Word Data

SH7040 Series CPU		Description	Example of Conventional CPU	
MOV.W	@(disp,PC),R1	Data is sign-extended to 32 bits, and R1 becomes H'00001234. It is next operated upon by an ADD instruction.	ADD.W	#H'1234,R0
ADD	R1,R0			
	.....			
.DATA.W	H'1234			

Note: @(disp, PC) accesses the immediate data.

Load-Store Architecture: Basic operations are executed between registers. For operations that involve memory access, data is loaded to the registers and executed (load-store architecture). Instructions such as AND that manipulate bits, however, are executed directly in memory.

Delayed Branch Instructions: Unconditional branch instructions are delayed. Executing the instruction that follows the branch instruction and then branching reduces pipeline disruption during branching (table 2.3). There are two types of conditional branch instructions: delayed branch instructions and ordinary branch instructions.

Table 2.12 Data Transfer Instructions

Instruction	Instruction Code	Operation	Execution Cycles	T Bit
MOV #imm,Rn	1110nnnniiiiiiii	#imm → Sign extension → Rn	1	—
MOV.W @(disp,PC),Rn	1001nnnndddddddd	(disp × 2 + PC) → Sign extension → Rn	1	—
MOV.L @(disp,PC),Rn	1101nnnndddddddd	(disp × 4 + PC) → Rn	1	—
MOV Rm,Rn	0110nnnnmmmm0011	Rm → Rn	1	—
MOV.B Rm,@Rn	0010nnnnmmmm0000	Rm → (Rn)	1	—
MOV.W Rm,@Rn	0010nnnnmmmm0001	Rm → (Rn)	1	—
MOV.L Rm,@Rn	0010nnnnmmmm0010	Rm → (Rn)	1	—
MOV.B @Rm,Rn	0110nnnnmmmm0000	(Rm) → Sign extension → Rn	1	—
MOV.W @Rm,Rn	0110nnnnmmmm0001	(Rm) → Sign extension → Rn	1	—
MOV.L @Rm,Rn	0110nnnnmmmm0010	(Rm) → Rn	1	—
MOV.B Rm,@–Rn	0010nnnnmmmm0100	Rn–1 → Rn, Rm → (Rn)	1	—
MOV.W Rm,@–Rn	0010nnnnmmmm0101	Rn–2 → Rn, Rm → (Rn)	1	—
MOV.L Rm,@–Rn	0010nnnnmmmm0110	Rn–4 → Rn, Rm → (Rn)	1	—
MOV.B @Rm+,Rn	0110nnnnmmmm0100	(Rm) → Sign extension → Rn,Rm + 1 → Rm	1	—
MOV.W @Rm+,Rn	0110nnnnmmmm0101	(Rm) → Sign extension → Rn,Rm + 2 → Rm	1	—
MOV.L @Rm+,Rn	0110nnnnmmmm0110	(Rm) → Rn,Rm + 4 → Rm	1	—
MOV.B R0,@(disp,Rn)	10000000nnnndddd	R0 → (disp + Rn)	1	—
MOV.W R0,@(disp,Rn)	10000001nnnndddd	R0 → (disp × 2 + Rn)	1	—
MOV.L Rm,@(disp,Rn)	0001nnnnmmmmdddd	Rm → (disp × 4 + Rn)	1	—
MOV.B @(disp,Rm),R0	10000100mmmmdddd	(disp + Rm) → Sign extension → R0	1	—
MOV.W @(disp,Rm),R0	10000101mmmmdddd	(disp × 2 + Rm) → Sign extension → R0	1	—
MOV.L @(disp,Rm),Rn	0101nnnnmmmmdddd	(disp × 4 + Rm) → Rn	1	—
MOV.B Rm,@(R0,Rn)	0000nnnnmmmm0100	Rm → (R0 + Rn)	1	—

Table 2.13 Arithmetic Operation Instructions (cont)

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
SUB	Rm,Rn	0011nnnnmmmm1000	Rn–Rm → Rn	1	—
SUBC	Rm,Rn	0011nnnnmmmm1010	Rn–Rm–T → Rn, Borrow → T	1	Borrow
SUBV	Rm,Rn	0011nnnnmmmm1011	Rn–Rm → Rn, Underflow → T	1	Overflow

Note: * The normal minimum number of execution cycles. (The number in parentheses is the number of cycles when there is contention with following instructions.)

Bit:	31	30	29	28	27	26	25	24
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	23	22	21	…	…	2	1	0
				…	…			
Initial value:	—	—	—	…	…	—	—	—
R/W:	R/W	R/W	R/W	…	…	R/W	R/W	R/W

11.2.2 DMA Destination Address Registers 0–3 (DAR0–DAR3)

DMA destination address registers 0–3 (DAR0–DAR3) are 32-bit read/write registers that specify the destination address of a DMA transfer. These registers have a count function, and during a DMA transfer, they indicate the next destination address. In single-address mode, DAR values are ignored when a device with DACK has been specified as the transfer destination.

Specify a 16-bit or 32-bit boundary address when doing 16-bit or 32-bit data transfers. Operation cannot be guaranteed on any other address. The initial value after power-on resets or in software standby mode, is undefined. These registers are not initialized with manual reset.

Bit:	31	30	29	28	27	26	25	24
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	23	22	21	…	…	2	1	0
				…	…			
Initial value:	—	—	—	…	…	—	—	—
R/W:	R/W	R/W	R/W	…	…	R/W	R/W	R/W

12.2.11 Timer Output Control Register (TOCR)

The timer output control register (TOCR) enables/disables PWM synchronized toggle output in complementary PWM mode and reset sync PWM mode, and controls output level inversion of PWM output. The TOCR is initialized to H'00 by a power-on reset or in the standby mode. Manual reset does not initialize TOCR. These register settings are ineffective for anything other than complementary PWM mode/reset-synchronized PWM mode.

Bit:	7	6	5	4	3	2	1	0
	—	PSYE	—	—	—	—	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R/W	R/W

- Bits 7, 5–2—Reserved: These bits always read as 1. The write value should always be 1.
- Bit 6—PWM Synchronous Output Enable (PSYE): Selects the enable/disable of toggle output synchronized with the PWM period.

Bit 6: PSYE	Description
0	Toggle output synchronous with PWM period disabled (initial value)
1	Toggle output synchronous with PWM period enabled

- Bit 1—Output Level Select N (OLSN): Selects the reverse phase output level of the complementary PWM mode or reset-synchronized PWM mode.

			Compare Match Output	
OLSN	**Initial Output**	**Active Level**	**Increment Count**	**Decrement Count**
0	High level*	Low level	High level	Low level (initial value)
1	Low level*	High level	Low level	High level

Note: * The reverse phase waveform initial output value changes to active level after elapse of the dead time after count start.

- Bit 0—Output Level Select P (OLSP): Selects the positive phase output level of the complementary PWM mode or reset-synchronized PWM mode.

			Compare Match Output	
OLSP	**Initial Output**	**Active Level**	**Increment Count**	**Decrement Count**
0	High level	Low level	Low level	High level (initial value)
1	Low level	High level	High level	Low level

Table 12.16 Register Settings for Complementary PWM Mode

Channel	Counter/Register	Description	Read/Write from CPU
3	TCNT3	Start of up-count from value set in dead time register	Maskable by BSC/BCR1 setting*
	TGR3A	Set TCNT3 upper limit value (1/2 carrier cycle + dead time)	Maskable by BSC/BCR1 setting*
	TGR3B	PWM output 1 compare register	Maskable by BSC/BCR1 setting*
	TGR3C	TGR3A buffer register	Always readable/writable
	TGR3D	PWM output 1/TGR3B buffer register	Always readable/writable
4	TCNT4	Up-count start, initialized to H'0000	Maskable by BSC/BCR1 setting*
	TGR4A	PWM output 2 compare register	Maskable by BSC/BCR1 setting*
	TGR4B	PWM output 3 compare register	Maskable by BSC/BCR1 setting*
	TGR4C	PWM output 2/TGR4A buffer register	Always readable/writable
	TGR4D	PWM output 3/TGR4B buffer register	Always readable/writable
Timer dead time data register (TDDR)		Set TCNT4 and TCNT3 offset value (dead time value)	Maskable by BSC/BCR1 setting*
Timer cycle data register (TCDR)		Set TCNT4 upper limit value (1/2 carrier cycle)	Maskable by BSC/BCR1 setting*
Timer cycle buffer register (TCBR)		TCDR buffer register	Always readable/writable
Subcounter (TCNTS)		Subcounter for dead time generation	Read-only
Temporary register 1 (TEMP1)		PWM output 1/TGR3B temporary register	Not readable/writable
Temporary register 2 (TEMP2)		PWM output 2/TGR4A temporary register	Not readable/writable
Temporary register 3 (TEMP3)		PWM output 3/TGR4B temporary register	Not readable/writable

Note: * Access can be enabled or disabled according to the setting of bit 13 (MTURWE) in BSC/BCR1 (bus controller/bus control register 1).

Section 13 Watchdog Timer (WDT)

13.1 Overview

The watchdog timer (WDT) is a 1-channel timer for monitoring system operations. If a system encounters a problem (crashes, for example) and the timer counter overflows without being rewritten correctly by the CPU, an overflow signal ($\overline{\text{WDTOVF}}$) is output externally. The WDT can simultaneously generate an internal reset signal for the entire chip.

When the watchdog function is not needed, the WDT can be used as an interval timer. In the interval timer operation, an interval timer interrupt is generated at each counter overflow. The WDT is also used in recovering from the standby mode.

13.1.1 Features

- Works in watchdog timer mode or interval timer mode.
- Outputs $\overline{\text{WDTOVF}}$ in the watchdog timer mode. When the counter overflows in the watchdog timer mode, overflow signal $\overline{\text{WDTOVF}}$ is output externally. You can select whether to reset the chip internally when this happens. Either the power-on reset or manual reset signal can be selected as the internal reset signal.
- Generates interrupts in the interval timer mode. When the counter overflows, it generates an interval timer interrupt.
- Clears standby mode.
- Works with eight counter input clocks.

Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)

Bit Rate (Bits/s)	φ (MHz)								
	18.432			19.6608			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	81	–0.22	3	86	0.31	3	88	–0.25
150	2	239	0.00	2	255	0.00	3	64	0.16
300	2	119	0.00	2	127	0.00	2	129	0.16
600	1	239	0.00	1	255	0.00	2	64	0.16
1200	1	119	0.00	1	127	0.00	1	129	0.16
2400	0	239	0.00	0	255	0.00	1	64	0.16
4800	0	119	0.00	0	127	0.00	0	129	0.16
9600	0	59	0.00	0	63	0.00	0	64	0.16
14400	0	39	0.00	0	42	–0.78	0	42	0.94
19200	0	29	0.00	0	31	0.00	0	32	–1.36
28800	0	19	0.00	0	20	1.59	0	21	–1.36
31250	0	17	2.40	0	19	–1.70	0	19	0.00
38400	0	14	0.00	0	15	0.00	0	15	1.73

14.3 Operation

14.3.1 Overview

For serial communication, the SCI has an asynchronous mode in which characters are synchronized individually, and a clock synchronous mode in which communication is synchronized with clock pulses. Asynchronous/clock synchronous mode and the transmission format are selected in the serial mode register (SMR), as shown in table 14.8. The SCI clock source is selected by the C/$\overline{A}$ bit in the serial mode register (SMR) and the CKE1 and CKE0 bits in the serial control register (SCR), as shown in table 14.9.

Asynchronous Mode:

- Data length is selectable: seven or eight bits.
- Parity and multiprocessor bits are selectable, as well as the stop bit length (one or two bits). These selections determine the transmit/receive format and character length.
- In receiving, it is possible to detect framing errors (FER), parity errors (PER), overrun errors (ORER), and the break state.
- An internal or external clock can be selected as the SCI clock source.
  - — When an internal clock is selected, the SCI operates using the on-chip baud rate generator clock, and can output a clock with a frequency matching the bit rate.
  - — When an external clock is selected, the external clock input must have a frequency 16 times the bit rate. (The on-chip baud rate generator is not used.)

Clock Synchronous Mode:

- The communication format has a fixed 8-bit data length.
- In receiving, it is possible to detect overrun errors (ORER).
- An internal or external clock can be selected as the SCI clock source.
  - — When an internal clock is selected, the SCI operates using the on-chip baud rate generator clock, and outputs a synchronous clock signal to external devices.
  - — When an external clock is selected, the SCI operates on the input synchronous clock. The on-chip baud rate generator is not used.

Table 15.3 Analog Input Channel and ADDR Correspondence

Analog Input Channel	A/D Data Register
AN0	ADDRA*
AN1	ADDRB*
AN2	ADDRC*
AN3	ADDRD*
AN4	ADDRE
AN5	ADDRF
AN6	ADDRG
AN7	ADDRH

Note: * Except during buffer operation

15.2.2 A/D Control/Status Register (ADCSR)

The ADCSR is an 8-bit read/write register used for A/D conversion operation control and to indicate status.

The ADCSR is initialized to H'00 by power-on reset or in standby mode. Manual reset does not initialize ADCSR.

Bit:	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	CKS	GRP	CH2	CH1	CH0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * The only value that can be written is a 0 to clear the flag.

The settings for this register are effective only for the 144-pin version. There are no corresponding pins for this register in the 112-pin and 120-pin versions. However, read/writes are possible.

Bit:	15	14	13	12	11	10	9	8
	—	PA23 MD	—	PA22 MD	—	PA21 MD	—	PA20 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

Bit:	7	6	5	4	3	2	1	0
	PA19 MD1	PA19 MD0	PA18 MD1	PA18 MD0	—	PA17 MD	—	PA16 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads as 0. The write value should always be 0.
- Bit 14—PA23 Mode (PA23MD): Selects the function of the PA23/$\overline{\text{WRHH}}$ pin.

Bit 14: PA23MD	Description
0	General input/output (PA23) (initial value) ($\overline{\text{WRHH}}$ in on-chip ROM invalid mode)
1	Most significant byte write output ($\overline{\text{WRHH}}$) (PA23 in single chip mode)

- Bit 13—Reserved: This bit always reads as 0. The write value should always be 0.
- Bit 12—PA22 Mode (PA22MD): Selects the function of the PA22/$\overline{\text{WRHL}}$ pin.

Bit 12: PA22MD	Description
0	General input/output (PA22) (initial value) ($\overline{\text{WRHL}}$ in on-chip ROM invalid mode)
1	Write output ($\overline{\text{WRHL}}$) (PA22 in single chip mode)

- Bit 11—Reserved: This bit always reads as 0. The write value should always be 0.
- Bit 10—PA21 Mode (PA21MD): Selects the function of the PA21/$\overline{\text{CASHH}}$ pin.

Bit 10: PA21MD	Description
0	General input/output (PA21) (initial value)
1	Column address output ($\overline{\text{CASHH}}$) (PA21 in single chip mode)

- Bit 9—Reserved: Always reads as 0. The write values should always be 0.

Table 22.12 Commands of the Programmer Mode

Command Name	Number of Cycles	First Cycle			Second Cycle		
		Mode	Address	Data	Mode	Address	Data
Memory read mode	1+n	write	X	H'00	read	RA	Dout
Auto-program mode	129	write	X	H'40	write	WA	Din
Auto-erase mode	2	write	X	H'20	write	X	H'20
Status read mode	2	write	X	H'71	write	X	H'71

Notes: 1. In auto-program mode, 129 cycles are required for command writing by a simultaneous 128-byte write.
2. In memory read mode, the number of cycles depends on the number of address write cycles (n).

22.11.3 Memory Read Mode

Table 22.13 AC Characteristics in Transition to Memory Read Mode (Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, T_a = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	t_{nxtc}	20		µs	
$\overline{CE}$ hold time	t_{ceh}	0		ns	
$\overline{CE}$ setup time	t_{ces}	0		ns	
Data hold time	t_{dh}	50		ns	
Data setup time	t_{ds}	50		ns	
Write pulse width	t_{wep}	70		ns	
$\overline{WE}$ rise time	t_r		30	ns	
$\overline{WE}$ fall time	t_f		30	ns	

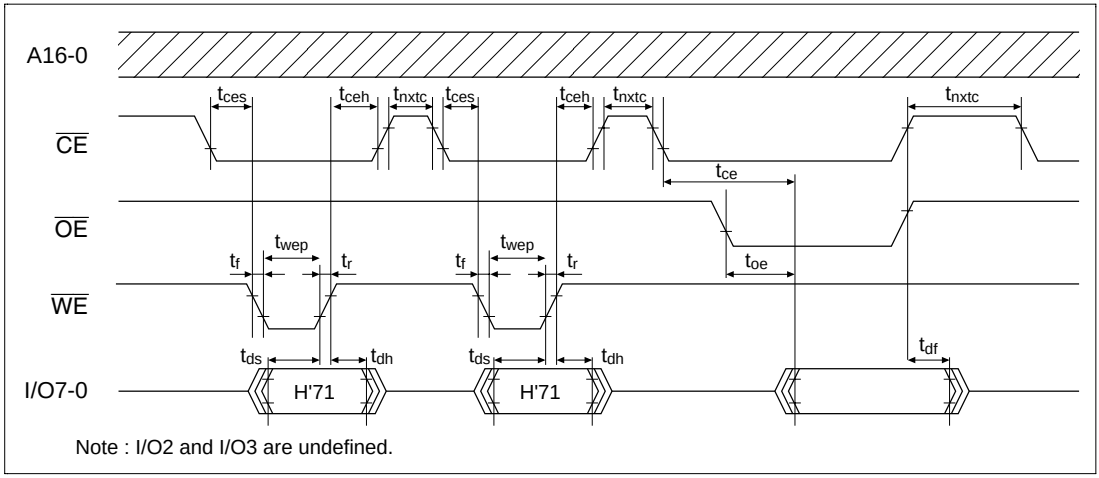

Figure 22.27 Status Read Mode Timing Waveforms

Table 22.19 Return Commands for the Status Read Mode

Pin Name	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Attribute	Normal end identification	Command error	Program-ming error	Erase error	—	—	Program-ming or erase count exceeded	Effective address error
Initial value	0	0	0	0	0	0	0	0
Indications	Normal end: 0 Abnormal end: 1	Command Error: 1 Otherwise: 0	Program-ming Error: 1 Otherwise: 0	Erasing Error: 1 Otherwise: 0	—	—	Count exceeded: 1 Otherwise: 0	Effective address Error: 1 Otherwise: 0

Note: D2 and D3 are undefined at present.

22.11.7 Status Polling

1. I/O7 status polling is a flag that indicates the operating status in auto-program/auto-erase mode.
2. I/O6 status polling is a flag that indicates a normal or abnormal end in auto-program/auto-erase mode.

24.1.2 Related Register

Table 24.2 shows the register used for power-down state control.

Table 24.2 Related Register

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Standby control register	SBYCR	R/W	H'1F	H'FFFF8614	8, 16, 32

24.2 Standby Control Register (SBYCR)

The standby control register (SBYCR) is a read/write 8-bit register that sets the transition to standby mode, and the port status in standby mode. The SBYCR is initialized to H'1F when reset.

Bit:	7	6	5	4	3	2	1	0
	SBY	HIZ	—	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/W	R/W	R	R	R	R	R	R

- Bit 7—Standby (SBY): Specifies transition to the standby mode. The SBY bit cannot be set to 1 while the watchdog timer is running (when the timer enable bit (TME) of the WDT timer control/status register (TCSR) is set to 1). To enter the standby mode, always halt the WDT by 0 clearing the TME bit, then set the SBY bit.

Bit 7: SBY	Description
0	Executing SLEEP instruction puts the LSI into sleep mode (initial value)
1	Executing SLEEP instruction puts the LSI into standby mode

- Bit 6—Port High Impedance (HIZ): In the standby mode, this bit selects whether to set the I/O port pin to high impedance or hold the pin status. The HIZ bit cannot be set to 1 when the TME bit of the WDT timer control/status register (TCSR) is set to 1. When making the I/O port pin status high impedance, always clear the TME bit to 0 before setting the HIZ bit.

Bit 6: HIZ	Description
0	Holds pin status while in standby mode (initial value)
1	Keeps pin at high impedance while in standby mode

- Bits 5–0—Reserved: Bit 5 always reads as 0. Always write 0 to bit 5. Bits 4–0 always read as 1. Always write 1 to these bits.

25.2 DC Characteristics

Table 25.2 DC Characteristics (Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75° C)

Item	Pin	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD3–MD0, PA2, PA5, PA6–PA9, PE0–PE15, FWP	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	—
	EXTAL		V_{CC} × 0.7	—	V_{CC} + 0.3	V	—
	A/D port		2.2	—	AV_{CC} + 0.3	V	—
	Other input pins		2.2	—	V_{CC} + 0.3	V	—
Input low-level voltage	$\overline{RES}$, NMI, MD3–MD0, PA2, PA5, PA6–PA9, PE0–PE15, FWP	V_{IL}	–0.3	—	0.5	V	—
	Other input pins		–0.3	—	0.8	V	—
Schmitt trigger input voltage	PA2, PA5, PA6–PA9, PE0–PE15	$VT^+ – VT^-$	0.4	—	—	V	$VT^+ \geq V_{CC}$ – 0.7 V (min)
							$VT^- \leq$ 0.5 V (max)
Input leak current	$\overline{RES}$, NMI, MD3–MD0, PA2, PA5, PA6–PA9, PE0–PE15,FWP	| Iin |	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	A/D port		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
	Other input pins (except EXTAL pin)		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Three-state leak current (while off)	A21–A0, D31–D0, $\overline{CS3}$–$\overline{CS0}$, RDWR, $\overline{RAS}$, $\overline{CASxx}$, $\overline{WRxx}$, $\overline{RD}$, ports A, B, C, D, E	| I_{TSI} |	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V

Table A.1 On-Chip I/O Register Addresses (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF8610	TCNT*1									WDT
H'FFFF8611	TCNT*2									
H'FFFF8612	RSTCSR*1	WOVF	RSTE	RSTS	—	—	—	—	—	
H'FFFF8613	RSTCSR*2	WOVF	RSTE	RSTS	—	—	—	—	—	
H'FFFF8614	SBYCR	SBY	HIZ	—	—	—	—	—	—	Power-down state
H'FFFF8615 to H'FFFF861F	—	—	—	—	—	—	—	—	—	BSC
H'FFFF8620	BCR1	—	—	MTURWE	—	—	—	—	IOE	
H'FFFF8621		A3LG	A2LG	A1LG	A0LG	A3SZ	A2SZ	A1SZ	A0SZ	
H'FFFF8622	BCR2	IW31	IW30	IW21	IW20	IW11	IW10	IW01	IW00	
H'FFFF8623		CW3	CW2	CW1	CW0	SW3	SW2	SW1	SW0	
H'FFFF8624	WCR1	W33	W32	W31	W30	W23	W22	W21	W20	
H'FFFF8625		W13	W12	W11	W10	W03	W02	W01	W00	
H'FFFF8626	WCR2	—	—	—	—	—	—	—	—	
H'FFFF8627		—	—	DDW1	DDW0	DSW3	DSW2	DSW1	DSW0	
H'FFFF8628	RAMER	—	—	—	—	—	—	—	—	FLASH (F-ZTAT
H'FFFF8629		—	—	—	—	—	RAMS	RAM1	RAM0	version only)
H'FFFF862A	DCR	TPC	RCD	TRAS1	TRAS0	DWW1	DWW0	DWR1	DWR0	BSC
H'FFFF862B		DIW	—	BE	RASD	SZ1	SZ0	AMX1	AMX0	
H'FFFF862C	RTCSR	—	—	—	—	—	—	—	—	
H'FFFF862D		—	CMF	CMIE	CKS2	CKS1	CKS0	RFSH	RMD	
H'FFFF862E	RTCNT	—	—	—	—	—	—	—	—	
H'FFFF862F										
H'FFFF8630	RTCOR	—	—	—	—	—	—	—	—	
H'FFFF8631										

Notes: *1 Write address.
*2 Read address. For details, see section 13.2.4, Register Access, in section 13, Watchdog Timer (WDT).

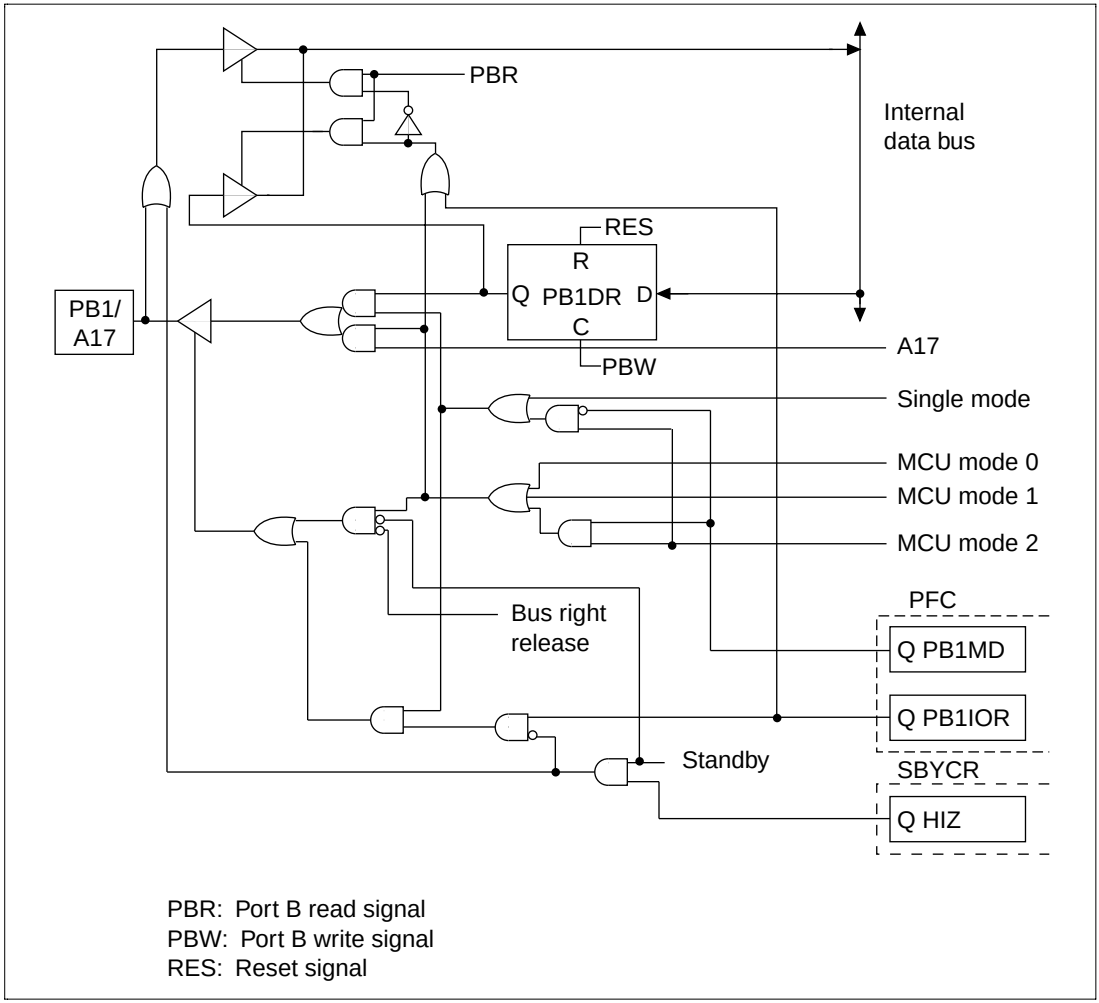

Figure B.16 PB1/A17 Block Diagram

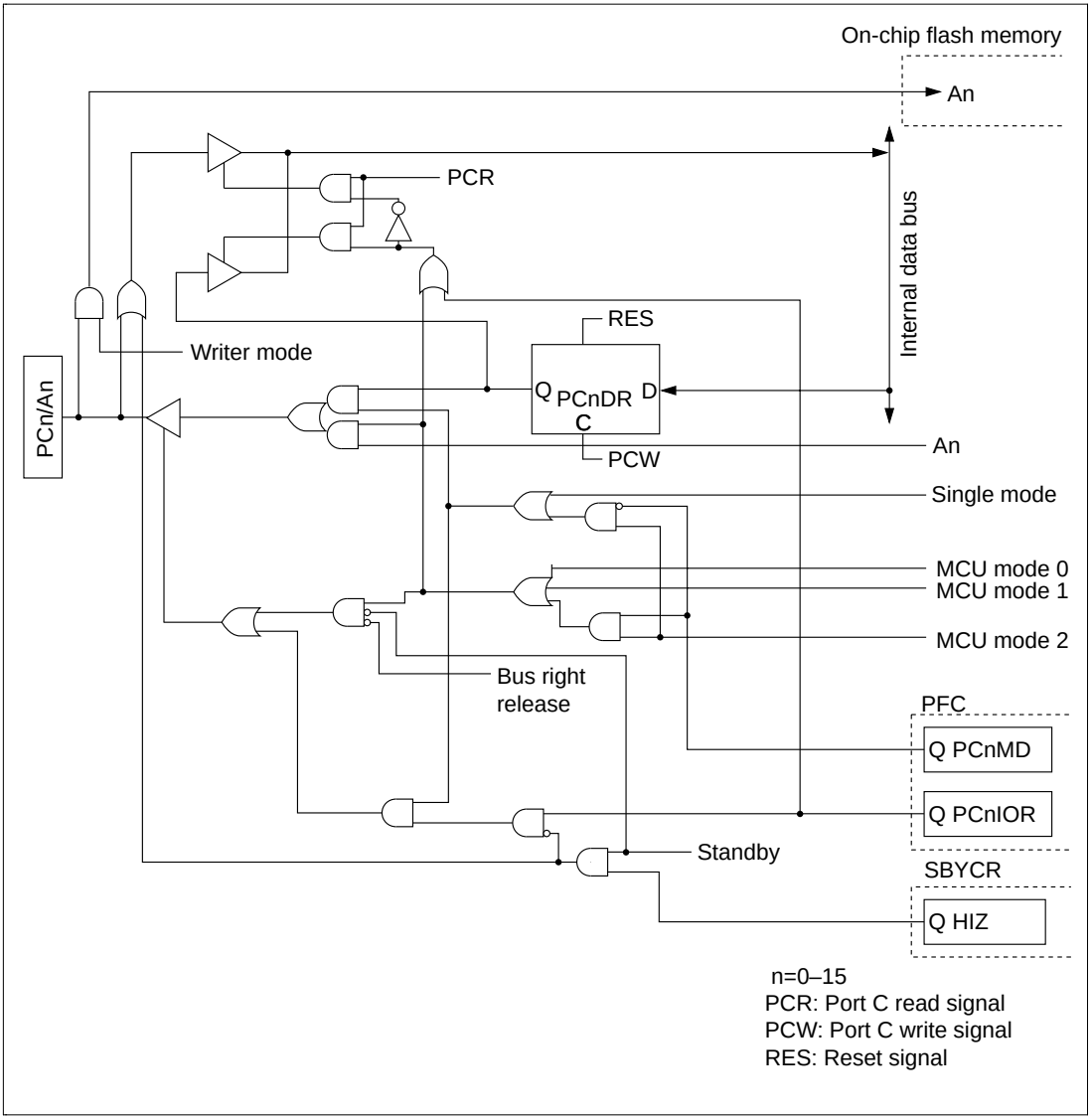

Figure B.23 PCn/An Block Diagram (F-ZTAT Version)