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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28.7MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417041af28v

Section 1 SH7040 Series Overview

1.1 SH7040 Series Overview

The SH7040 Series (SH7040/41/42/43/44/45) CMOS single-chip microprocessors integrate a Renesas-original architecture, high-speed CPU with peripheral functions required for system configuration.

The CPU has a RISC-type instruction set. Most instructions can be executed in one clock cycle, which greatly improves instruction execution speed. In addition, the 32-bit internal-bus architecture enhances data processing power. With this CPU, it has become possible to assemble low cost, high performance/high-functioning systems, even for applications that were previously impossible with microprocessors, such as real-time control, which demands high speeds. In particular, the SH7040 series has a 1-kbyte on-chip cache, which allows an improvement in CPU performance during external memory access.

In addition, the SH7040 Series includes on-chip peripheral functions necessary for system configuration, such as large-capacity ROM and RAM, timers, a serial communication interface (SCI), an A/D converter, an interrupt controller, and I/O ports. Memory or peripheral LSIs can be connected efficiently with an external memory access support function. This greatly reduces system cost.

In addition to the masked-ROM versions of the SH7040 series, the SH7042 and SH7043 have a ZTAT™*1 version with user-programmable on-chip PROM and the SH7044 and SH7045 have an F-ZTAT™*2 version with on-chip flash memory. These versions enable users to respond quickly and flexibly to changing application specifications, growing production volumes, and other conditions.

Notes: *1 ZTAT (Zero Turn-Around Time) is a registered trademark of Renesas Technology Corp.
*2 F-ZTAT (Flexible ZTAT) is a trademark of Renesas Technology Corp.

1.1.1 SH7040 Series Features

CPU:

- Original Renesas architecture
- 32-bit internal data bus
- General-register machine
  - Sixteen 32-bit general registers
  - Three 32-bit control registers
  - Four 32-bit system registers
- RISC-type instruction set

Table 1.3 Pin Arrangement by Mode for SH7040, SH7042 (TQFP-120 Pin) (cont)

TQFP120 Pin No.	MCU Mode	PROM Mode
63	PD10/D10	NC
64	PD9/D9	NC
65	PD8/D8	NC
66	V_{SS}	V_{SS}
67	PD7/D7	D7
68	PD6/D6	D6
69	PD5/D5	D5
70	V_{CC}	V_{CC}
71	PD4/D4	D4
72	PD3/D3	D3
73	PD2/D2	D2
74	PD1/D1	D1
75	PD0/D0	D0
76	V_{SS}	V_{SS}
77	XTAL	NC
78	MD3	V_{CC}
79	EXTAL	V_{SS}
80	MD2	V_{CC}
81	NMI	A9
82	V_{CC}	V_{CC}
83	MD1	V_{CC}
84	MD0	V_{CC}
85	$PLLV_{CC}$	V_{CC}
86	PLLCAP	V_{SS}
87	$PLLV_{SS}$	V_{SS}
88	PA15/CK	NC
89	$\overline{RES}$	V_{PP}
90	NC	NC
91	NC	NC
92	PE0/TIOC0A/$\overline{DREQ0}$	NC
93	PE1/TIOC0B/$\overline{DRAK0}$	NC

Table 2.9 Instruction Formats (cont)

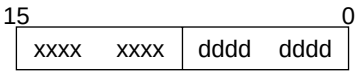
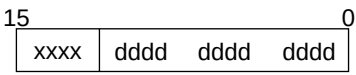
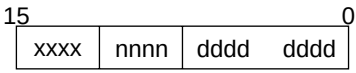
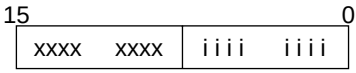
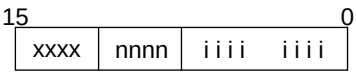
Instruction Formats	Source Operand	Destination Operand	Example
d format 	dddddddd: Indirect GBR with displacement	R0 (Direct register)	`MOV.L @(disp,GBR),R0`
	R0(Direct register)	dddddddd: Indirect GBR with displacement	`MOV.L R0,@(disp,GBR)`
	dddddddd: PC relative with displacement	R0 (Direct register)	`MOVA @(disp,PC),R0`
	dddddddd: PC relative	—	`BF label`
d12 format 	ddddddddddddd: PC relative	—	`BRA label` `(label = disp + PC)`
nd8 format 	dddddddd: PC relative with displacement	nnnn: Direct register	`MOV.L @(disp,PC),Rn`
i format 	iiiiiiii: Immediate	Indirect indexed GBR	`AND.B #imm,@(R0,GBR)`
	iiiiiiii: Immediate	R0 (Direct register)	`AND #imm,R0`
	iiiiiiii: Immediate	—	`TRAPA #imm`
ni format 	iiiiiiii: Immediate	nnnn: Direct register	`ADD #imm,Rn`

Table 2.12 Data Transfer Instructions (cont)

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
MOV.W	Rm,@(R0,Rn)	0000nnnnmmmm0101	Rm → (R0 + Rn)	1	—
MOV.L	Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B	@(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W	@(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L	@(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B	R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W	R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L	R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B	@(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W	@(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L	@(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA	@(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT	Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B	Rm,Rn	0110nnnnmmmm1000	Rm → Swap the bottom two bytes → Rn	1	—
SWAP.W	Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT	Rm,Rn	0010nnnnmmmm1101	Rm: Middle 32 bits of Rn → Rn	1	—

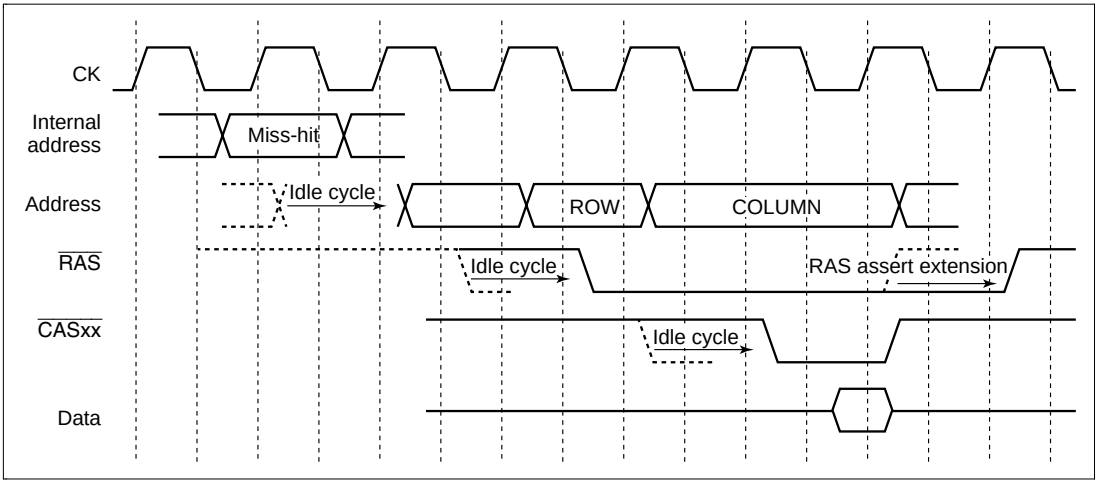


Figure 9.7 Cache Fill Timing in Case of Non-Consecutive Cache Miss from DRAM Space (Normal Mode, TPC = 0, RCD = 0, No Wait)

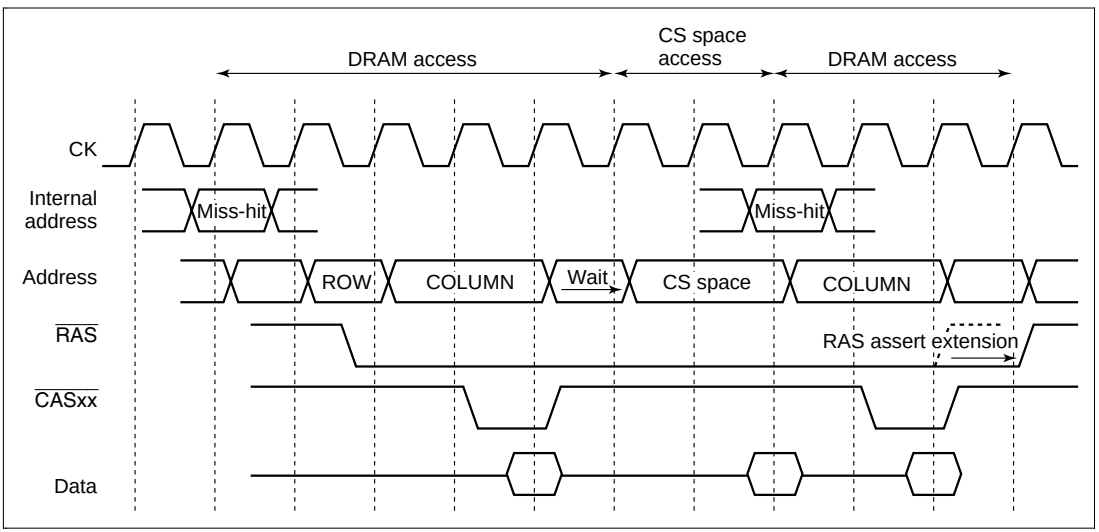


Figure 9.8 Cache Fill Timing in Case of Consecutive Cache Misses from DRAM Space (RAS Down Mode, TPC = 0, RCD = 0, No Wait)

9.4.4 Cache Hit after Cache Miss

The first cache hit after a cache miss is regarded as a cache miss, and a cache fill without idle cycle generation is performed. The next hit operates as a cache hit.

Self-Refresh: When both the RMD and RFSH bits of the RTCSR are set to 1, the $\overline{CAS}$ signal and $\overline{RAS}$ signal are output and the DRAM enters self-refresh mode, as shown in figure 10.16. Do not access DRAM during self-refreshes, in order to preserve DRAM data. When performing DRAM accesses, first cancel the self-refresh, then access only after doing individual refreshes for all row addresses within the time prescribed for the particular DRAM.

For external bus right requests during self-refreshes, to preserve DRAM data at the time of releasing the bus rights, only $\overline{CASx}$, $\overline{RAS}$, and RDWR are output and the bus rights are released to the external device with the self-refresh maintained. Consequently, do not perform DRAM accesses from external devices at such a time.

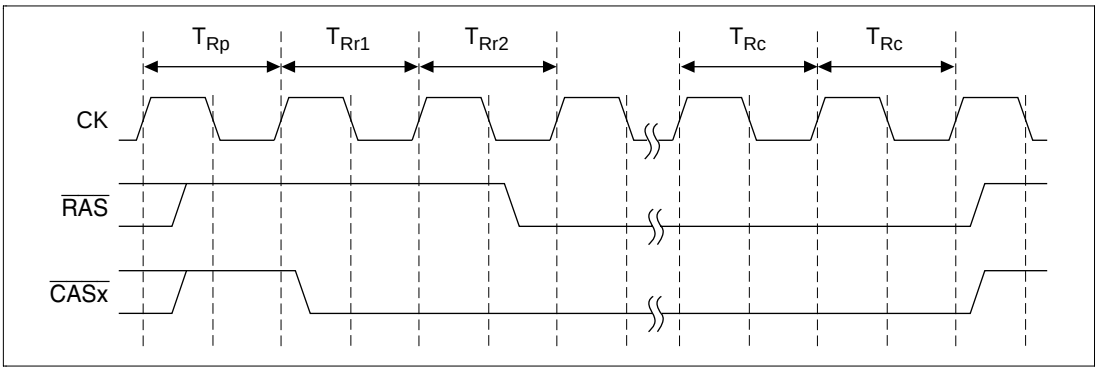


Figure 10.16 Self-Refresh Timing

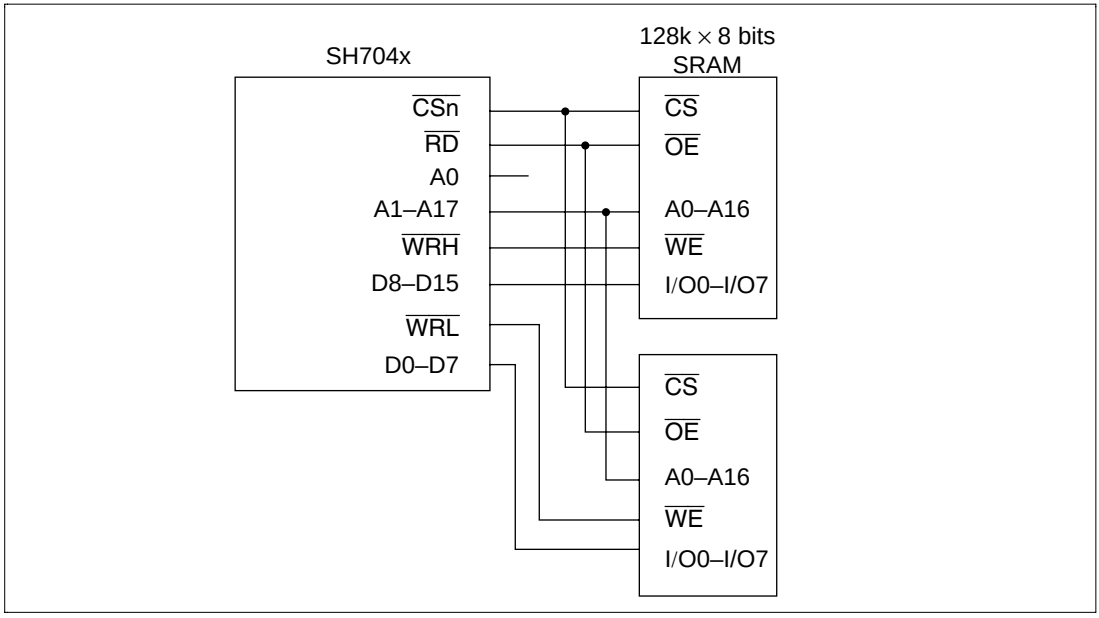


Figure 10.27 16-Bit Data Bus Width SRAM Connection

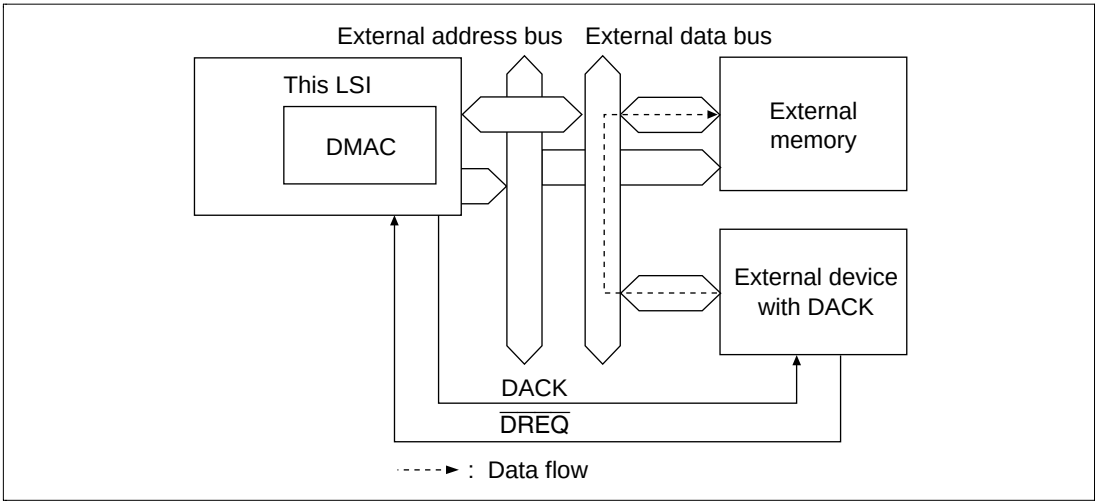
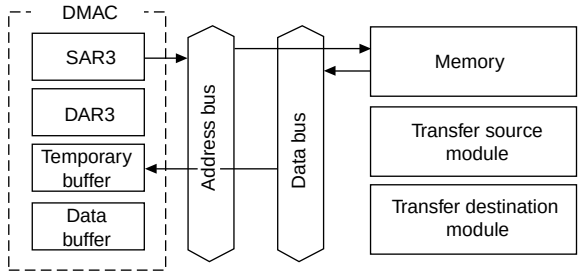


Figure 11.5 Data Flow in Single Address Mode

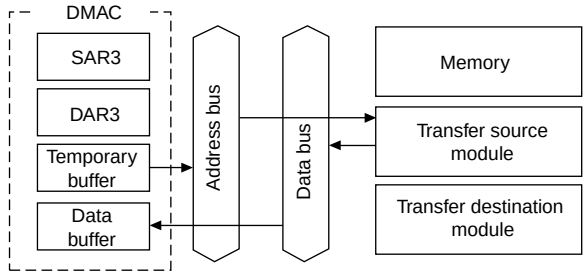
Two types of transfers are possible in the single address mode: (a) transfers between external devices with DACK and memory-mapped external devices, and (b) transfers between external devices with DACK and external memory. The only transfer requests for either of these is the external request ($\overline{\text{DREQ}}$). Figure 11.6 shows the DMA transfer timing for the single address mode.

1st, 2nd bus cycles



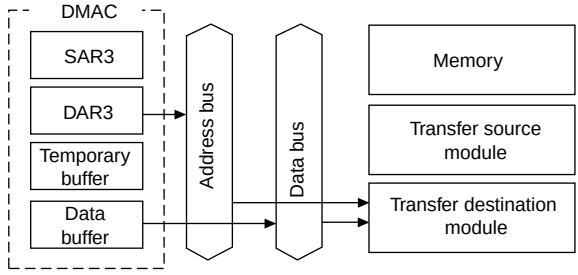
The SAR3 value is taken as the address, memory data is read, and the value is stored in the temporary buffer. Since the value read at this time is used as the address, it must be 32 bits. When external connection data bus is 16 bits, two bus cycles are required.

3rd bus cycle



The value in the temporary buffer is taken as the address, and data is read from the transfer source module to the data buffer.

4th bus cycle



The DAR3 value is taken as the address, and the value in the data buffer is written to the transfer destination module.

Note: Memory, transfer source, and transfer destination modules are shown here. In practice, connection can be made anywhere there is address space.

Figure 11.9 Dual Address Mode and Indirect Address Operation (When External Memory Space is 16 bits)

Burst Mode, Single Address, and Level Detection: $\overline{\text{DREQ}}$ sampling timing in burst mode with single address and level detection is shown in figures 11.21 and 11.22.

In burst mode with single address and level detection, a dummy cycle is inserted as one bus cycle, at the earliest, three cycles after timing of the first sampling. Data during this period is undefined, and the DACK signal is not output. Nor is the number of DMAC transfers counted. The actual DMAC transfer begins after one dummy bus cycle output.

The dummy cycle is not counted either at the start of the second sampling (transfer one bus cycle before the start of the first DMAC transfer). Therefore, the second sampling is not conducted from the bus cycle starting the dummy cycle, but from the start of the CPU(3) bus cycle.

Thereafter, as long the $\overline{\text{DREQ}}$ is continuously sampled, no dummy cycle is inserted. $\overline{\text{DREQ}}$ sampling timing during this period begins from the start of the transfer one bus cycle before the start of DMAC transfer, in the same way as with cycle steal mode.

As with the fourth sampling in figure 11.21, once DMAC transfer is interrupted, a dummy cycle is again inserted at the start as soon as DMAC transfer is resumed.

The DACK output period in burst mode is the same as in cycle steal mode.

- Bit 4—Buffer Operation A (BFA): Designates whether to use the TGRA register for normal operation, or buffer operation in combination with the TGRC register. When using TGRC as a buffer register, no TGRC register input capture/output compares are generated.

  This bit is reserved in channels 1 and 2, which have no TGRC registers. It is always read as 0, and cannot be modified.

Bit 4: BFA	Description
0	TGRA operates normally (initial value)
1	TGRA and TGRC buffer operation

- Bits 3–0—Modes 3–0 (MD3–MD0): These bits set the timer operation mode.

Bit 3: MD3	Bit 2: MD2	Bit 1: MD1	Bit 0: MD0	Description
0	0	0	0	Normal operation (initial value)
			1	Reserved (do not set)
		1	0	PWM mode 1
			1	PWM mode 2*1
	1	0	0	Phase counting mode 1*2
			1	Phase counting mode 2*2
		1	0	Phase counting mode 3*2
			1	Phase counting mode 4*2
1	0	0	0	Reset synchronous PWM mode*3
			1	Reserved (do not set)
		1	0	Reserved (do not set)
			1	Reserved (do not set)
	1	0	0	Reserved (do not set)
			1	Complementary PWM mode 1 (transmit at peak)*3
		1	0	Complementary PWM mode 2 (transmit at valley)*3
			1	Complementary PWM mode 3 (transmit at peak and valley) *3

Notes: *1 PWM mode 2 can not be set for channels 3, 4.

*2 Phase measurement mode can not be set for channels 0, 3, 4.

*3 Reset synchronous PWM mode, complementary PWM mode can only be set for channel 3. When channel 3 is set to reset synchronous PWM mode or complementary PWM mode, the channel 4 settings become ineffective and automatically conform to the channel 3 settings. However, do not set channel 4 to reset synchronous PWM mode or complementary PWM mode. Reset synchronous PWM mode and complementary PWM mode can not be set for channels 0, 1, 2.

12.2.14 Timer Dead Time Data Register (TDDR)

The timer dead time data register (TDDR) is a 16-bit register, used only in complementary PWM mode, that specifies the TCNT3 and TCNT4 counter offset values. In complementary PWM mode, when the TCNT3 and TCNT4 counters are cleared and then restarted, the TDDR register value is loaded into the TCNT3 counter and the count operation starts. The TDDR register is initialized to H'FFFF by a power-on reset or in standby mode. Manual reset does not initialize TDDR. Accessing the TDDR in 8-bit units is prohibited. Always access in 16-bit units.

Bit:	15	14	13	12	11	10	9	8
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2.15 Timer Period Data Register (TCDR)

The timer period data register (TCDR) is a 16-bit register used only in complementary PWM mode. Set the PWM carrier sync value as the TCDR register value. This register is constantly compared with the TCNTS counter in complementary PWM mode, and when a match occurs the TCNTS counter switches direction (decrement to increment).

The TCDR register is initialized to H'FFFF by a reset or in standby mode. Manual reset does not initialize TCDR. Accessing the TCDR in 8-bit units is prohibited. Always access in 16-bit units.

Bit:	15	14	13	12	11	10	9	8
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- A mask operation

  For A mask, the above operation is modified as follows:

  In complementary PWM mode, buffer register compare-match flags can be set only for compare with three counters (TCNT3, TCNT4, and TCNTS).

  Special properties of compare match flag disappear and compare match flags of buffer registers are set to all set values of buffer registers.

  Figure 12.92 shows an example when setting the duty setting register to TGR3B, buffer register to TGR3D and Buffer register to TGR3A-Td.

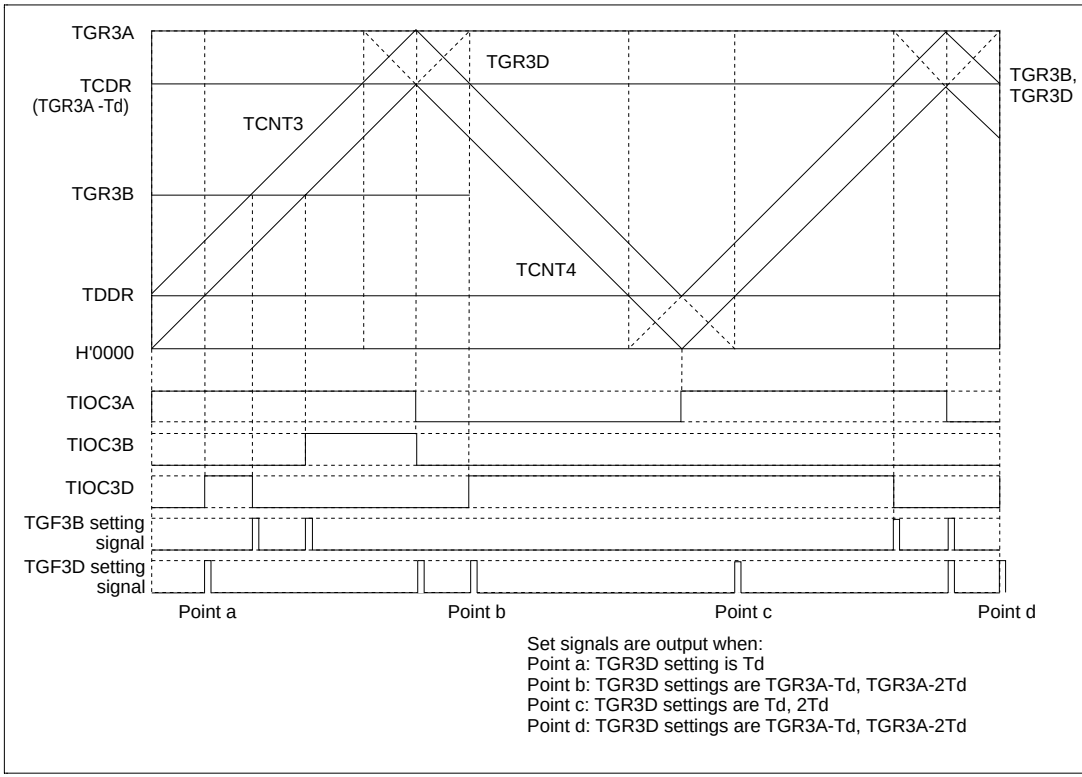


Figure. 12.92 Special Properties of Compare Match Flag in Complementary PWM Mode (for A Mask)

12.9 Port Output Enable (POE)

The port output enable (POE) can be used to establish a high-impedance state for high-current pins, by changing the $\overline{\text{POE0}}$–$\overline{\text{POE3}}$ pin input, depending on the output status of the high-current pins (PE09/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B/$\overline{\text{MRES}}$, PE14/TIOC4C/DACK0/$\overline{\text{AH}}$, PE15/TIOC4D/DACK1/$\overline{\text{IRQOUT}}$). It can also simultaneously generate interrupt requests.

The high-current pins also become high-impedance regardless of whether these pin functions are selected in cases such as when the oscillator stops or in standby mode. Refer to section 4, Clock Pulse Generator (CPG), for details.

12.9.1 Features

- Each of the $\overline{\text{POE0}}$–$\overline{\text{POE3}}$ input pins can be set for falling edge, $\phi/8 \times 16$, $\phi/16 \times 16$, or $\phi/128 \times 16$ low-level sampling.
- High-current pins can be set to high-impedance state by $\overline{\text{POE0}}$–$\overline{\text{POE3}}$ pin falling-edge or low-level sampling.
- High-current pins can be set to high-impedance state when the high-current pin output levels are compared and simultaneous low-level output continues for one cycle or more (except in the 33.3 MHz version).
- Interrupts can be generated by input-level sampling or output-level comparison results.

14.1.2 Block Diagram

Figure 14.1 shows a block diagram of the SCI.

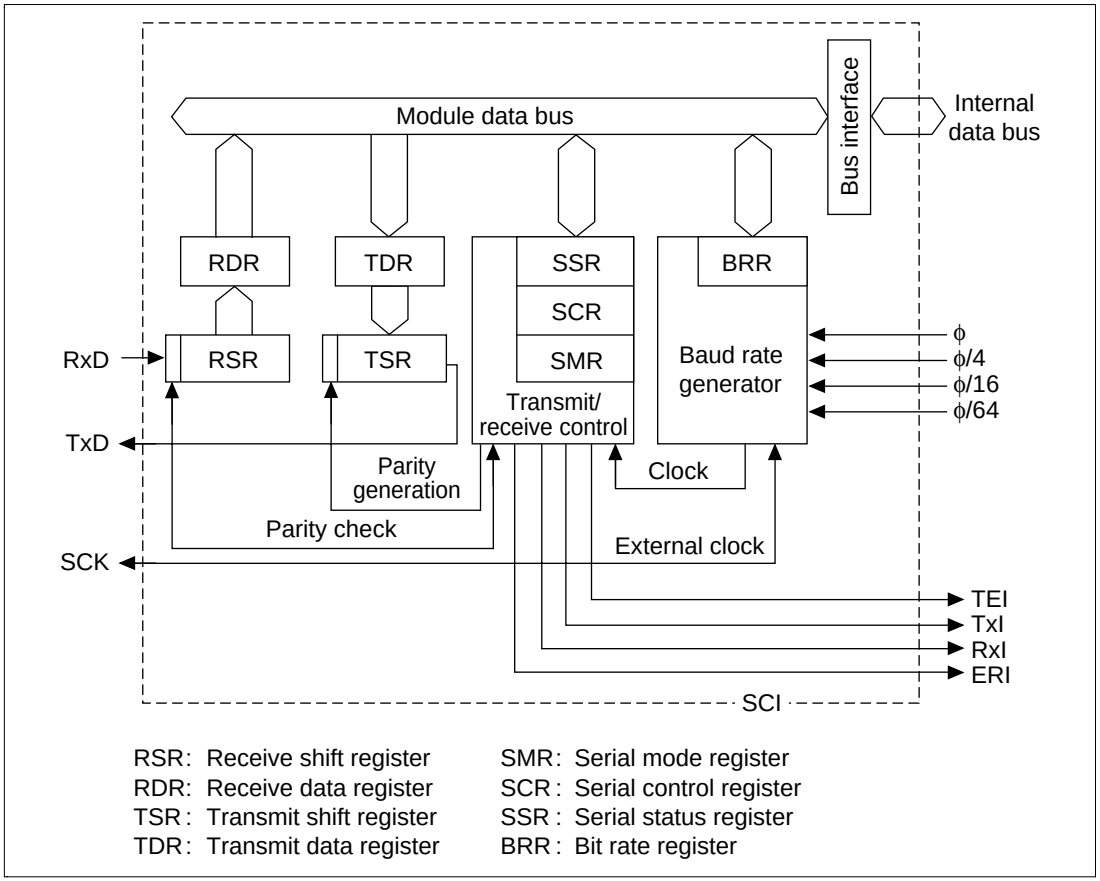


Figure 14.1 SCI Block Diagram

19.3 Port B

Port B is a 10-pin input/output port as listed in table 19.5.

Table 19.5 Port B

ROM Disabled Extended Mode (Modes 0, 1)	ROM Enabled Extended Mode (Mode 2)	Single Chip Mode
PB9 (I/O)/$\overline{\text{IRQ7}}$ (input)/A21 (output)/$\overline{\text{ADTRG}}$ (input)	PB9 (I/O)/$\overline{\text{IRQ7}}$ (input)/A21 (output)/$\overline{\text{ADTRG}}$ (input)	PB9 (I/O)/$\overline{\text{IRQ7}}$ (input)/$\overline{\text{ADTRG}}$ (input)
PB8 (I/O)/$\overline{\text{IRQ6}}$ (input)/A20 (output)/$\overline{\text{WAIT}}$ (input)	PB8 (I/O)/$\overline{\text{IRQ6}}$ (input)/A20 (output)/$\overline{\text{WAIT}}$ (input)	PB8 (I/O)/$\overline{\text{IRQ6}}$ (input)
PB7 (I/O)/$\overline{\text{IRQ5}}$ (input)/A19 (output)/$\overline{\text{BREQ}}$ (input)	PB7 (I/O)/$\overline{\text{IRQ5}}$ (input)/A19 (output)/$\overline{\text{BREQ}}$ (input)	PB7 (I/O)/$\overline{\text{IRQ5}}$ (input)
PB6 (I/O)/$\overline{\text{IRQ4}}$ (input)/A18 (output)/$\overline{\text{BACK}}$ (output)	PB6 (I/O)/$\overline{\text{IRQ4}}$ (input)/A18 (output)/$\overline{\text{BACK}}$ (input)	PB6 (I/O)/$\overline{\text{IRQ4}}$ (input)
PB5 (I/O)/$\overline{\text{IRQ3}}$ (input)/$\overline{\text{POE3}}$ (input)/RDWR (output)	PB5 (I/O)/$\overline{\text{IRQ3}}$ (input)/$\overline{\text{POE3}}$ (input)/RDWR (output)	PB5 (I/O)/$\overline{\text{IRQ3}}$ (input)/$\overline{\text{POE3}}$ (input)
PB4 (I/O)/$\overline{\text{IRQ2}}$ (input)/$\overline{\text{POE2}}$ (input)/$\overline{\text{CASH}}$ (output)	PB4 (I/O)/$\overline{\text{IRQ2}}$ (input)/$\overline{\text{POE2}}$ (input)/$\overline{\text{CASH}}$ (output)	PB4 (I/O)/$\overline{\text{IRQ2}}$ (input)/$\overline{\text{POE2}}$ (input)
PB3 (I/O)/$\overline{\text{IRQ1}}$ (input)/$\overline{\text{POE1}}$ (input)/$\overline{\text{CASL}}$ (output)	PB3 (I/O)/$\overline{\text{IRQ1}}$ (input)/$\overline{\text{POE1}}$ (input)/$\overline{\text{CASL}}$ (output)	PB3 (I/O)/$\overline{\text{IRQ1}}$ (input)/$\overline{\text{POE1}}$ (input)
PB2 (I/O)/$\overline{\text{IRQ0}}$ (input)/$\overline{\text{POE0}}$ (input)/$\overline{\text{RAS}}$ (output)	PB2 (I/O)/$\overline{\text{IRQ0}}$ (input)/$\overline{\text{POE0}}$ (input)/$\overline{\text{RAS}}$ (output)	PB2 (I/O)/$\overline{\text{IRQ0}}$ (input)/$\overline{\text{POE0}}$ (input)
A17 (output)	PB1 (I/O)/A17 (output)	PB1 (I/O)
A16 (output)	PB0 (I/O)/A16 (output)	PB0 (I/O)

19.3.1 Register Configuration

Table 19.6 summarizes the port B register.

Table 19.6 Port B Register

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port B data register	PBDR	R/W	H'0000	H'FFFF8390 H'FFFF8391	8, 16, 32

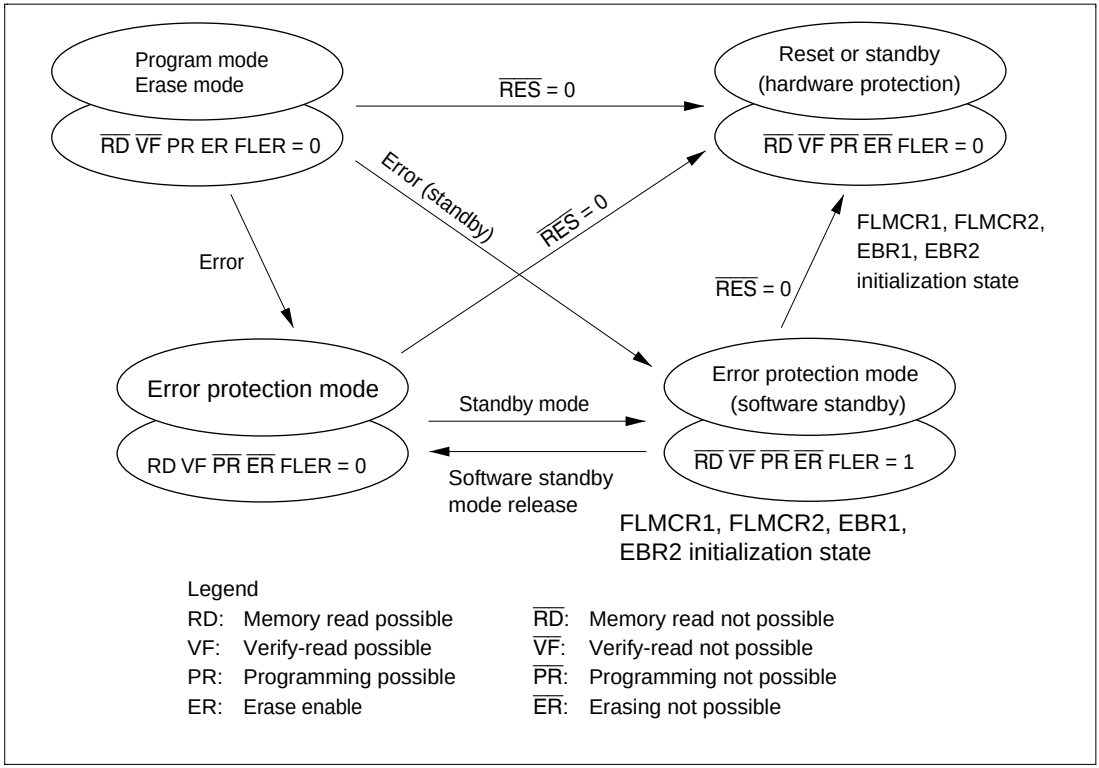


Figure 22.15 Flash Memory State Transitions

Table 25.7 Bus Timing (Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = – 20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
Write address setup time	t_{AS}	0	—	ns	25.8–25.9
Write address hold time	t_{WR}	5	—	ns	25.8, 25.9, 25.19
Write data hold time	t_{WRH}	0	—	ns	
Read/write strobe delay time 1	t_{RWD1}	2*3	18	ns	25.11–25.16
Read/write strobe delay time 2	t_{RWD2}	2*3	18	ns	
High-speed page mode CAS precharge time	t_{CP}	t_{cyc} – 25	—	ns	25.16
RAS precharge time	t_{RP}	$t_{cyc} \times (TPC + 1.5) - 15$	—	ns	25.11–25.16
CAS setup time	t_{CSR}	10	—	ns	25.17, 25.18
AH delay time 1	t_{AHD1}	2*3	18	ns	25.19
AH delay time 2	t_{AHD2}	2*3	18	ns	
Multiplex address delay time	t_{MAD}	2*3	18	ns	
Multiplex address hold time	t_{MAH}	0	—	ns	
DACK delay time	t_{DACKD1}	2*3	21	ns	25.8, 25.9, 25.11–25.16, 25.19

Notes: n is the number of waits. m is 0 when the number of DRAM write cycle waits is 0, and 1 otherwise. RCD is the set value of the RCD bit in DCR. TPC is the set value of the TPC bit in DCR.

*1 If the access time is satisfied, t_{RDS} need not be satisfied.

*2 t_{WDH} (max) is a reference value.

*3 The delay time Min values are reference values (typ).

*4 t_{RDS} is a reference value.

*5 When 28.7MHz, tASR=0ns (min)

Table A.1 On-Chip I/O Register Addresses (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF86DC	CHCR1	—	—	—	—	—	—	—	—	DMAC
H'FFFF86DD		—	—	—	DI	RO	RL	AM	AL	
H'FFFF86DE		DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'FFFF86DF		—	DS	TM	TS1	TS0	IE	TE	DE	
H'FFFF86E0	SAR2									
H'FFFF86E1										
H'FFFF86E2										
H'FFFF86E3										
H'FFFF86E4	DAR2									
H'FFFF86E5										
H'FFFF86E6										
H'FFFF86E7										
H'FFFF86E8	DMATCR2	—	—	—	—	—	—	—	—	
H'FFFF86E9										
H'FFFF86EA										
H'FFFF86EB										
H'FFFF86EC	CHCR2	—	—	—	—	—	—	—	—	
H'FFFF86ED		—	—	—	DI	RO	RL	AM	AL	
H'FFFF86EE		DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'FFFF86EF		—	DS	TM	TS1	TS0	IE	TE	DE	
H'FFFF86F0	SAR3									
H'FFFF86F1										
H'FFFF86F2										
H'FFFF86F3										
H'FFFF86F4	DAR3									
H'FFFF86F5										
H'FFFF86F6										
H'FFFF86F7										
H'FFFF86F8	DMATCR3	—	—	—	—	—	—	—	—	
H'FFFF86F9										
H'FFFF86FA										
H'FFFF86FB										
H'FFFF86FC	CHCR3	—	—	—	—	—	—	—	—	
H'FFFF86FD		—	—	—	DI	RO	RL	AM	AL	
H'FFFF86FE		DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'FFFF86FF		—	DS	TM	TS1	TS0	IE	TE	DE	