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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28.7MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417041avf16v

— Instruction length: 16-bit fixed length for improved code efficiency
— Load-store architecture (basic operations are executed between registers)
— Delayed branch instructions reduce pipeline disruption during branch
— Instruction set based on C language

- Instruction execution time: one instruction/cycle (35 ns/instruction at 28.7-MHz operation)
- Address space: Architecture supports 4 Gbytes
- On-chip multiplier: multiplication operations (32 bits × 32 bits → 64 bits) and multiplication/accumulation operations (32 bits × 32 bits + 64 bits → 64 bits) executed in two to four cycles
- Five-stage pipeline

Cache Memory:

- 1-kbyte instruction cache
- Caching of instruction codes and PC relative read data
- 4-byte line length (1 longword: 2 instruction lengths)
- 256 entry cache tags
- Direct map method
- On-chip ROM/RAM, and on-chip I/O areas not objects of cache
- Used in common with on-chip RAM; 2 kbytes of on-chip RAM used as address array/data array when cache is enabled

Interrupt Controller (INTC):

- Nine external interrupt pins (NMI, $\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$)
- Forty-three internal interrupt sources (forty-four for A mask)
- Sixteen programmable priority levels

User Break Controller (UBC):

- Generates an interrupt when the CPU or DMAC generates a bus cycle with specified conditions
- Simplifies configuration of an on-chip debugger

Bus State Controller (BSC):

- Supports external extended memory access
  — 16-bit (QFP-112, TQFP-120), or 32-bit (QFP-144) external data bus
- Memory address space divided into five areas (four areas of SRAM space, one area of DRAM space) with the following settable features:
  — Bus size (8, 16, or 32 bits)
  — Number of wait cycles

Table 2.13 Arithmetic Operation Instructions (cont)

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
DMULS.L	Rm,Rn	0011nnnnmmmm1101	Signed operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bit	2 to 4*	—
DMULU.L	Rm,Rn	0011nnnnmmmm0101	Unsigned operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bit	2 to 4*	—
DT	Rn	0100nnnn00010000	Rn – 1 → Rn, when Rn is 0, 1 → T. When Rn is nonzero, 0 → T	1	Comparison result
EXTS.B	Rm,Rn	0110nnnnmmmm1110	A byte in Rm is sign-extended → Rn	1	—
EXTS.W	Rm,Rn	0110nnnnmmmm1111	A word in Rm is sign-extended → Rn	1	—
EXTU.B	Rm,Rn	0110nnnnmmmm1100	A byte in Rm is zero-extended → Rn	1	—
EXTU.W	Rm,Rn	0110nnnnmmmm1101	A word in Rm is zero-extended → Rn	1	—
MAC.L	@Rm+,@Rn+	0000nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 32 × 32 → 64 bit	3/(2 to 4)*	—
MAC.W	@Rm+,@Rn+	0100nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 16 × 16 + 64 → 64 bit	3/(2)*	—
MUL.L	Rm,Rn	0000nnnnmmmm0111	Rn × Rm → MACL, 32 × 32 → 32 bit	2 to 4*	—
MULS.W	Rm,Rn	0010nnnnmmmm1111	Signed operation of Rn × Rm → MAC 16 × 16 → 32 bit	1 to 3*	—
MULU.W	Rm,Rn	0010nnnnmmmm1110	Unsigned operation of Rn × Rm → MAC 16 × 16 → 32 bit	1 to 3*	—
NEG	Rm,Rn	0110nnnnmmmm1011	0–Rm → Rn	1	—
NEGC	Rm,Rn	0110nnnnmmmm1010	0–Rm–T → Rn, Borrow → T	1	Borrow

Table 3.2 indicates the setting method for the clock mode.

Table 3.2 Clock Mode Setting

MD3	MD2	Clock Mode
0	0	PLL ON × 1
0	1	PLL ON × 2
1	0	PLL ON × 4
1	1	Reserved (PROM mode only)

3.2 Explanation of Operating Modes

Table 3.3 describes the operating modes.

Table 3.3 Operating Modes

Mode	Description
(MCU) Mode 0	CS0 area becomes an external memory space with 8-bit bus width for the 112-pin version, and 16-bit for the 144-pin version.
(MCU) Mode 1	CS0 area becomes an external memory space with 16-bit bus width for the 112-pin version, and 32-bit for the 144-pin version
(MCU) Mode 2	The on-chip ROM becomes effective. The bus width for the on-chip ROM space is 32 bit.
Mode 3 (single chip mode)	Any port can be used, but external addresses can not be employed.
Mode 4 (PROM mode)	On-chip ROM can be programmed using a general PROM writer.
Clock mode	The input waveform frequency can be used as is, doubled or quadrupled as an internal clock in modes 0 to 3.

5.1.3 Exception Processing Vector Table

Before exception processing begins running, the exception processing vector table must be set in memory. The exception processing vector table stores the start addresses of exception service routines. (The reset exception processing table holds the initial values of PC and SP.)

All exception sources are given different vector numbers and vector table address offsets, from which the vector table addresses are calculated. During exception processing, the start addresses of the exception service routines are fetched from the exception processing vector table, which indicated by this vector table address.

Table 5.3 shows the vector numbers and vector table address offsets. Table 5.4 shows how vector table addresses are calculated.

Table 5.3 Exception Processing Vector Table

Exception Sources		Vector Numbers	Vector Table Address Offset
Power-on reset	PC	0	H'00000000–H'00000003
	SP	1	H'00000004–H'00000007
Manual reset	PC	2	H'00000008–H'0000000B
	SP	3	H'0000000C–H'0000000F
General illegal instruction		4	H'00000010–H'00000013
(Reserved by system)		5	H'00000014–H'00000017
Slot illegal instruction		6	H'00000018–H'0000001B
(Reserved by system)		7	H'0000001C–H'0000001F
(Reserved by system)		8	H'00000020–H'00000023
CPU address error		9	H'00000024–H'00000027
DMAC/DTC address error		10	H'00000028–H'0000002B
Interrupts	NMI	11	H'0000002C–H'0000002F
	User break	12	H'00000030–H'00000033
(Reserved by system)		13	H'00000034–H'00000037
		:	:
		31	H'0000007C–H'0000007F
Trap instruction (user vector)		32	H'00000080–H'00000083
		:	:
		63	H'000000FC–H'000000FF

Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range	Default Priority
		Vector No.	Vector Table Address Offset				
SCI1	ERI1	132	H'00000210–H'00000213	0–15 (0)	IPRF (3–0)	High	High
	RXI1	133	H'00000214–H'00000217	0–15 (0)			
	TXI1	134	H'00000218–H'0000021B	0–15 (0)			
	TEI1	135	H'0000021C–H'0000021F	0–15 (0)		Low	
A/D*	ADI	136	H'00000220–H'00000223	0–15 (0)	IPRG (15–12)	—	
DTC	SWDTCE	140	H'00000230–H'00000233	0–15 (0)	IPRG (11–8)	—	
CMT0	CMI0	144	H'00000240–H'00000243	0–15 (0)	IPRG (7–4)	—	
CMT1	CMI1	148	H'00000250–H'00000253	0–15 (0)	IPRG (3–0)	—	
WDT	ITI	152	H'00000260–H'00000263	0–15 (0)	IPRH (15–12)	High	
BSC	CMI	153	H'00000264–H'00000267	0–15 (0)		Low	
I/O	OEI	156	H'00000270–H'00000273	0–15 (0)	IPRH (11–8)	—	Low

Note: * For A mask products, A/D is as follows

A/D	ADI0	136	H'00000220–H'00000223	0–15 (0)	IPRG (15–12)	High
	ADI1	137	H'00000224–H'00000227	0–15 (0)		Low

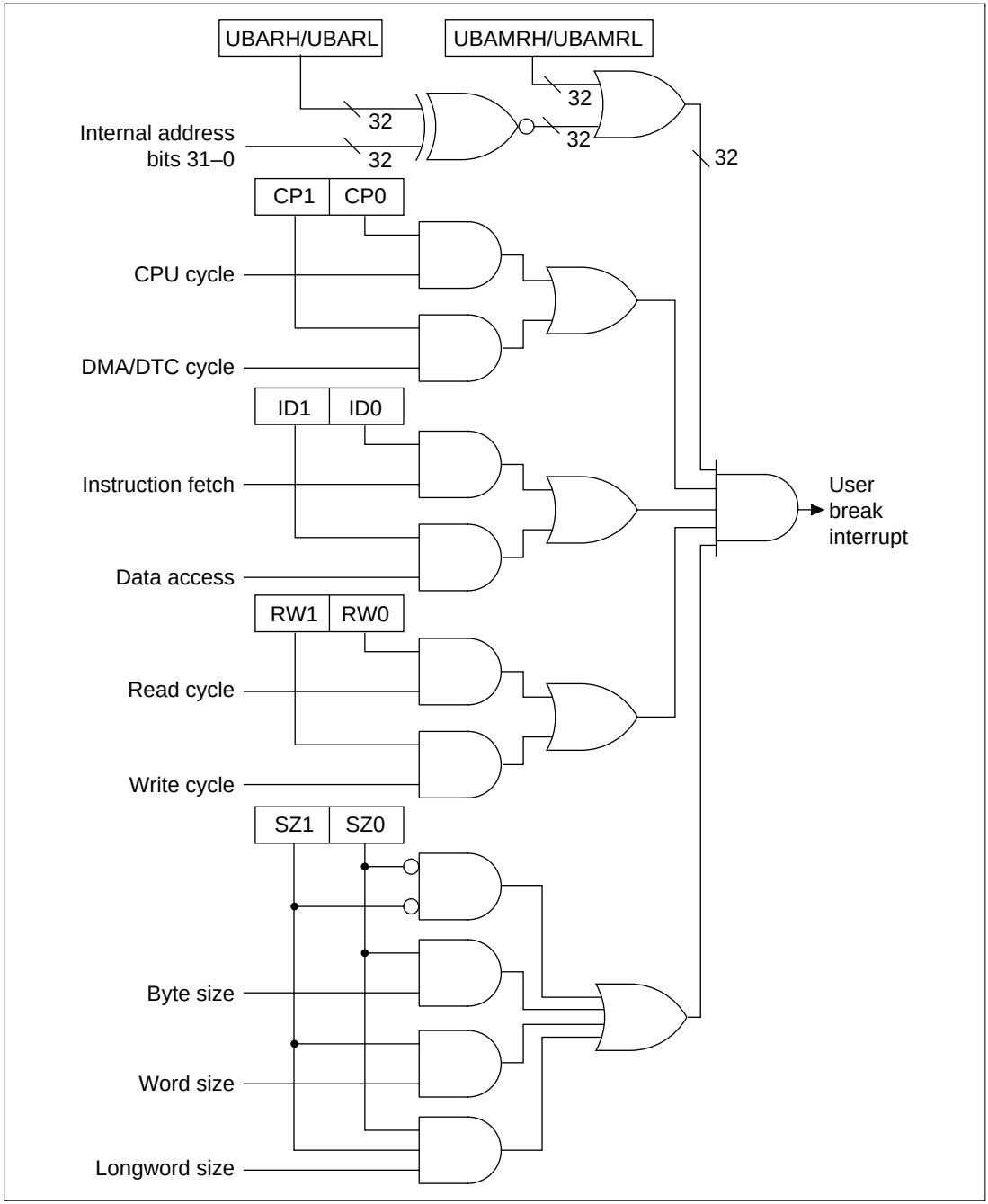


Figure 7.2 Break Condition Judgment Method

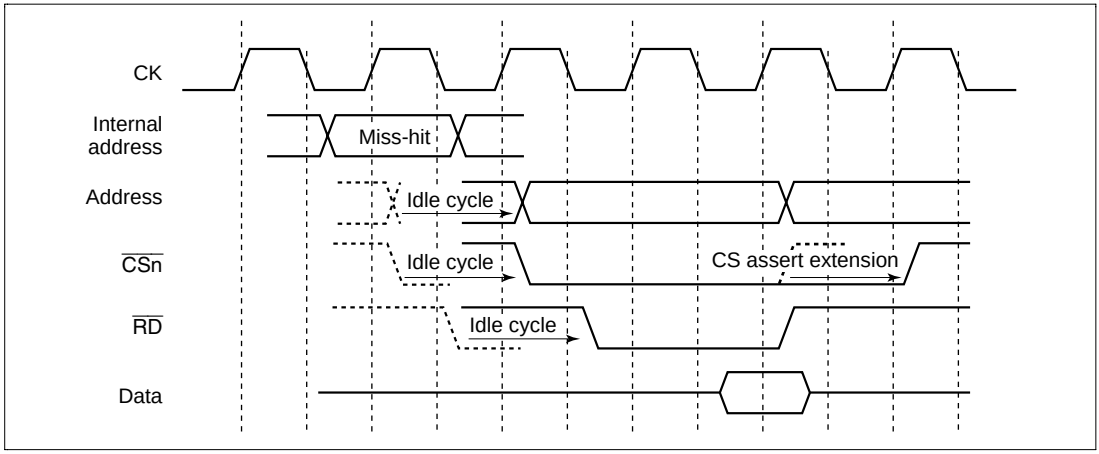


Figure 9.5 Cache Fill Timing in Case of Non-Consecutive Cache Miss from Normal Space (No Wait, No CS Assert Extension)

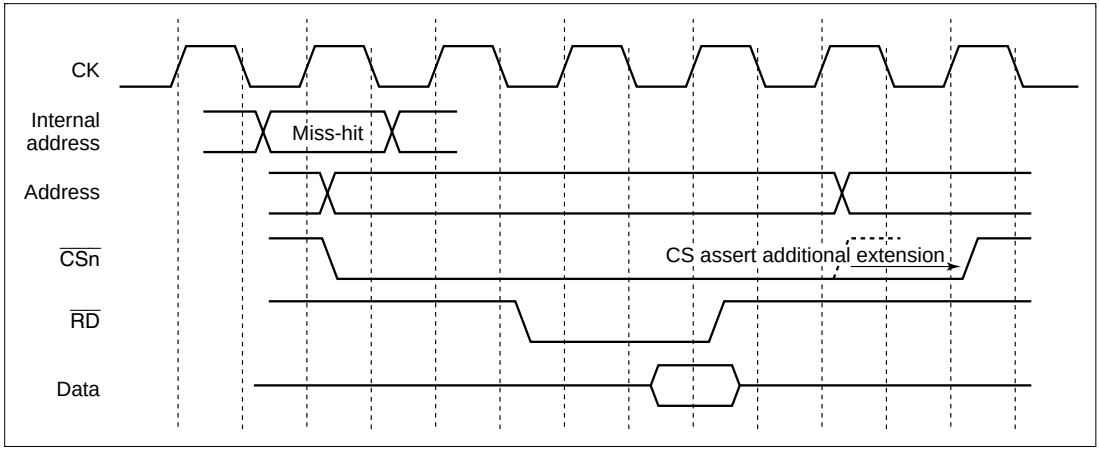


Figure 9.6 Cache Fill Timing in Case of Consecutive Cache Misses from Normal Space (No Wait, CS Assert Extension)

- Bits 11–8—Resource Select 3–0 (RS3–RS0): These bits specify the transfer request source.

Bit 11: RS3	Bit 10: RS2	Bit 9: RS1	Bit 8: RS0	Description
0	0	0	0	External request, dual address mode (initial value)
0	0	0	1	Prohibited
0	0	1	0	External request, single address mode. External address space → external device.
0	0	1	1	External request, single address mode. External device → external address space.
0	1	0	0	Auto-request
0	1	0	1	Prohibited
0	1	1	0	MTU TGI0A
0	1	1	1	MTU TGI1A
1	0	0	0	MTU TGI2A
1	0	0	1	MTU TGI3A
1	0	1	0	MTU TGI4A
1	0	1	1	A/D ADI*
1	1	0	0	SCI0 TXI0
1	1	0	1	SCI0 RXI0
1	1	1	0	SCI1 TXI1
1	1	1	1	SCI1 RXI1

Notes: External request designations are valid only for channels 0 and 1. No transfer request sources can be set for channels 2 or 3.

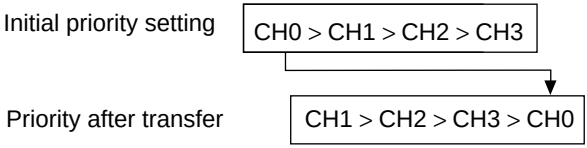
* ADI1 for A mask.

- Bit 7—Reserved bits: Data is 0 when read. The write value always be 0.
- Bit 6—$\overline{\text{DREQ}}$ Select (DS): Sets the sampling method for the $\overline{\text{DREQ}}$ pin in external request mode to either low-level detection or falling-edge detection. This bit is valid only with CHCR0 and CHCR1. For CHCR2 and CHCR3, this bit always reads as 0 and cannot be modified.

  Even with channels 0 and 1, when specifying an on-chip peripheral module or auto-request as the transfer request source, this bit setting is ignored. The sampling method is fixed at falling-edge detection in cases other than auto-request.

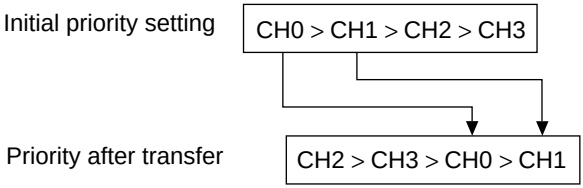
Bit 6: DS	Description
0	Low-level detection (initial value)
1	Falling-edge detection

Transfer on channel 0



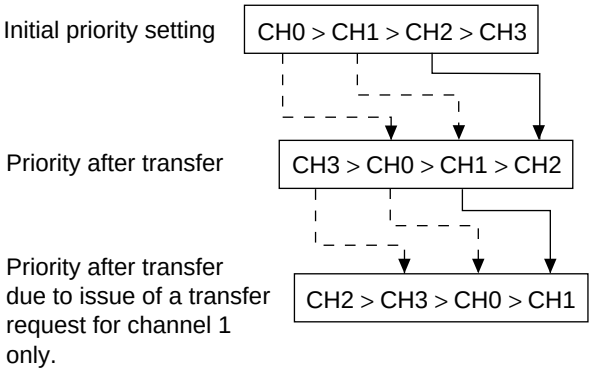
Channel 0 is given the lowest priority.

Transfer on channel 1



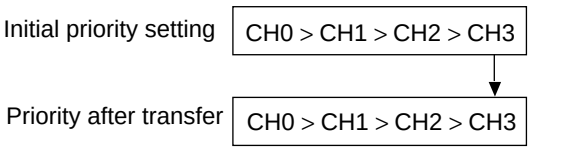
When channel 1 is given the lowest priority, the priority of channel 0, which was above channel 1, is also shifted simultaneously.

Transfer on channel 2



When channel 2 receives the lowest priority, the priorities of channel 0 and 1, which were above channel 2, are also shifted simultaneously. Immediately thereafter, if there is a transfer request for channel 1 only, channel 1 is given the lowest priority, and the priorities of channels 3 and 0 are simultaneously shifted down.

Transfer on channel 3



No change in priority.

Figure 11.3 Round Robin Mode

— Complementary PWM mode: By combining channels 3 and 4, a triangle wave comparator type six-phase PWM output is possible with non-overlapping times.

- High speed access via internal 16-bit bus
- Twenty-three interrupt sources
  — Channels 0, 3, and 4 have four compare-match/input capture interrupts and one overflow interrupt which can be requested independently.
  — Channels 1 and 2 have two compare-match/input capture interrupts, one overflow interrupt, and one underflow interrupt which can be requested independently.
- Automatic transfer of register data

  Block transfer, 1-word data transfers and 1-byte data transfers are possible through DTC or DMAC activation.
- A/D converter conversion start trigger can be generated
  — Channels 0–4 compare-match/input capture signals can be used as A/D converter conversion start triggers.

12.2.5 Timer Status Register (TSR)

The timer status register (TSR) is an 8-bit register that indicates the status of each channel. The MTU has five TSR registers, one each for channel. TSR is initialized to H'C0 by a power-on reset or by standby mode. This register is not initialized by a manual reset.

Channel 0: TSR0:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 writes to clear the flags are possible.

Channels 1, 2: TSR1, TSR2:

Bit:	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Note: * Only 0 writes to clear the flags are possible.

Channels 3, 4: TSR3, TSR4:

Bit:	7	6	5	4	3	2	1	0
	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 writes to clear the flags are possible.

- Bit 7—Count Direction Flag (TCFD): This status flag indicates the count direction of the channel 1, 2, 3, 4 TCNT counters.

  This bit is reserved in channel 0. This bit always reads as 1. The write value should always be 1.

Bit 7: TCFD	Description
0	TCNT counts down
1	TCNT counts up (initial value)

- Bit 6—Reserved: This bit always reads as 1. The write value should always be 1.

12.7.16 Contention between Overflow/Underflow and Counter Clearing

If overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence.

Figure 12.93 shows the operation timing when a TGR compare-match is specified as the clearing source, and H'FFFF is set in TGR.

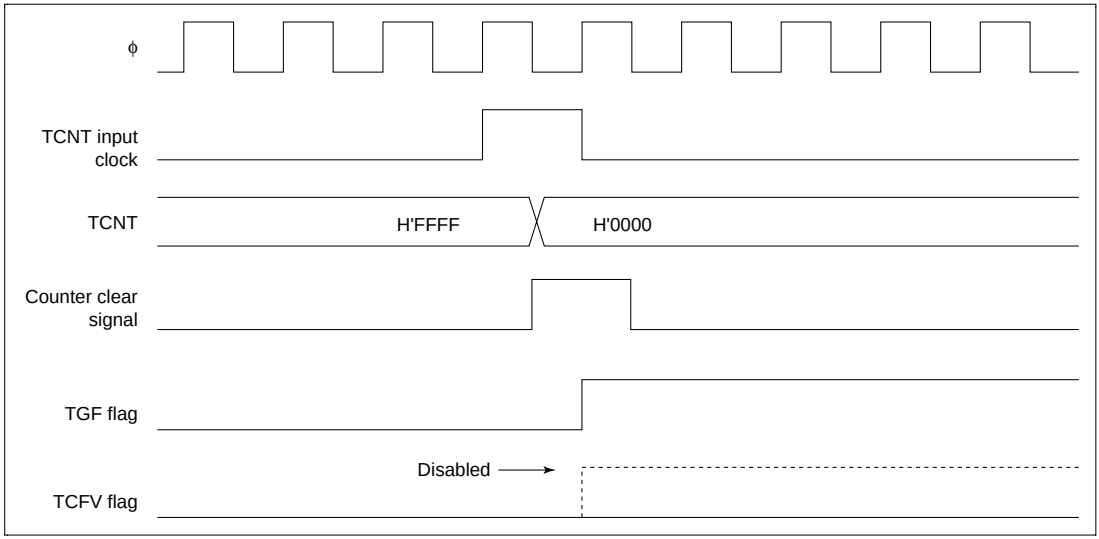


Figure 12.93 Contention between Overflow and Counter Clearing

Figure 14.19 shows an example of SCI transmit operation.

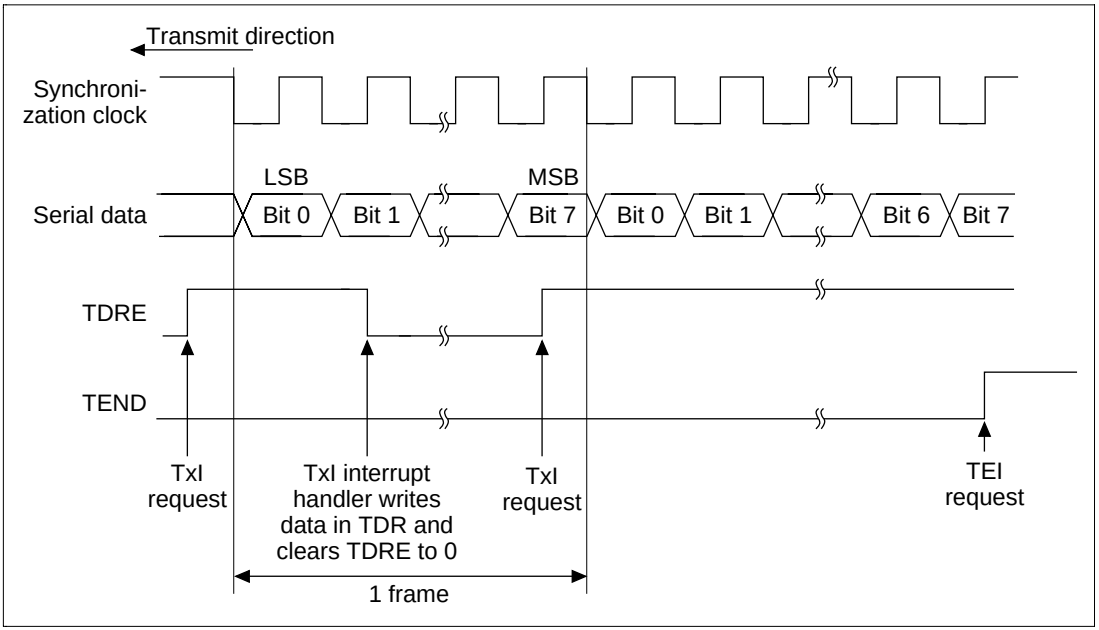


Figure 14.19 Example of SCI Transmit Operation

SCI serial transmission operates as follows.

1. The SCI monitors the TDRE bit in the SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data and loads this data from the TDR into the transmit shift register (TSR).
2. After loading the data from the TDR into the TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) in the SCR is set to 1, the SCI requests a transmit-data-empty interrupt (TxI) at this time.

   If clock output mode is selected, the SCI outputs eight synchronous clock pulses. If an external clock source is selected, the SCI outputs data in synchronization with the input clock. Data are output from the TxD pin in order from the LSB (bit 0) to the MSB (bit 7).
3. The SCI checks the TDRE bit when it outputs the MSB (bit 7). If TDRE is 0, the SCI loads data from the TDR into the TSR, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in the SSR to 1, transmits the MSB, then holds the transmit data pin (TxD) in the MSB state. If the transmit-end interrupt enable bit (TEIE) in the SCR is set to 1, a transmit-end interrupt (TEI) is requested at this time.
4. After the end of serial transmission, the SCK pin is held in the high state.

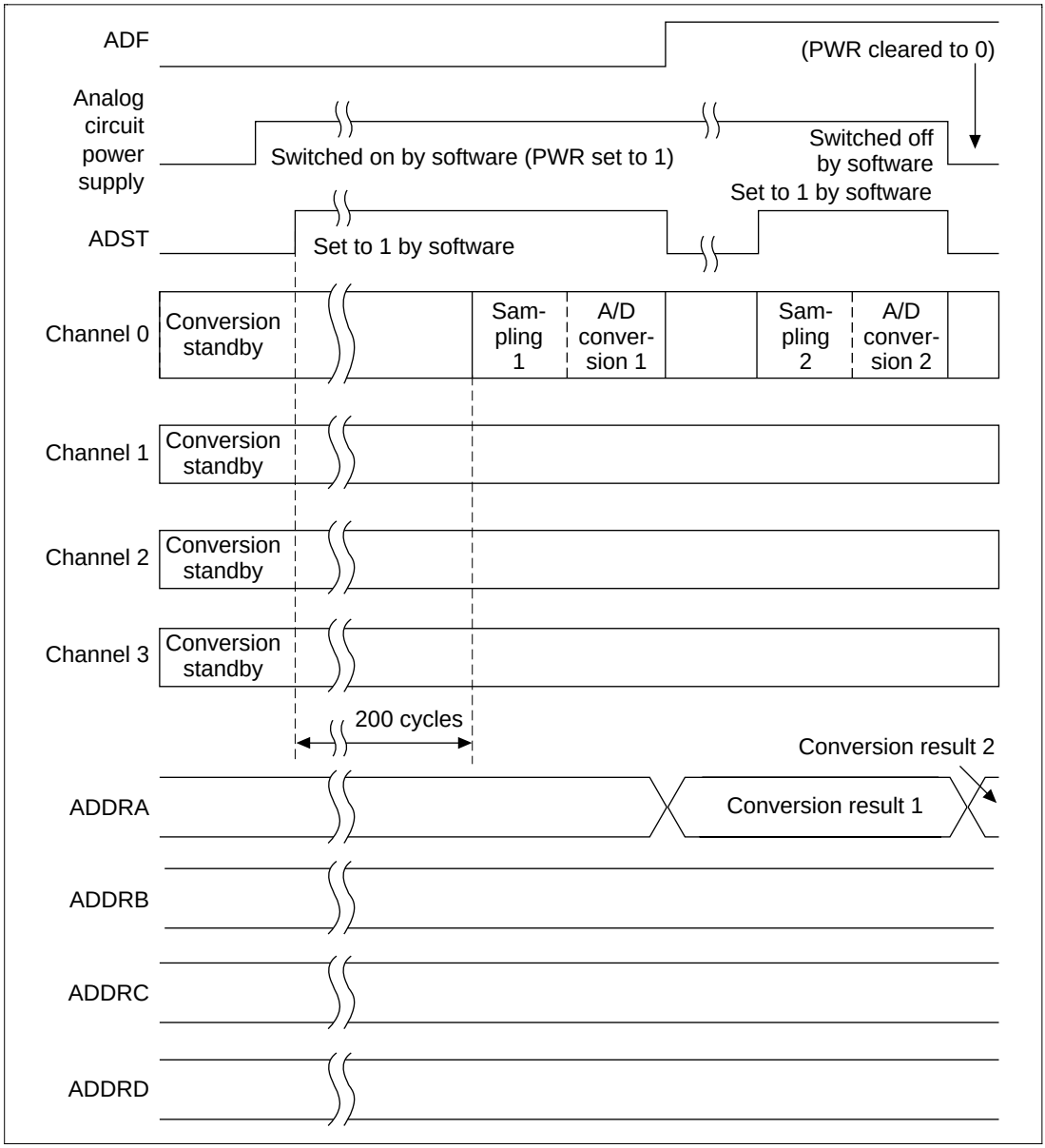


Figure 15.11 Conversion Start Operation (High-Speed Start Mode)

Table 15.10 Analog Input Pin Specification

Item	Min	Max	Unit
Analog input capacity	—	20	pF
Permitted source impedance	—	1	kΩ

16.7 Usage Notes

The following points should be noted when using the mid-speed A/D converter.

16.7.1 Analog Voltage Settings

(1) Analog input voltage range

The voltage applied to analog input pins during A/D conversion should be in the range AVSS ≤ ANn ≤ AV_{ref} (n = 0 to 7).

(2) AV_{CC} and AV_{SS} input voltages

For the AV_{CC} and AV_{SS} input voltages, set $AV_{CC} = V_{CC} \pm 10\%$ and $AV_{SS} = V_{SS}$. When the medium-speed A/D converter is not used, set $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$.

(3) AVref input voltage

For the AV_{ref} pin input voltage analog reference, set $AV_{ref} \leq AV_{CC}$. When the medium-speed A/D converter is not used, set $AV_{ref} = AV_{CC}$.

(4) AV_{CC} and AV_{ref} must be connected to the power supply (V_{CC}) even if the medium-speed A/D converter is not used or is in standby mode.

16.7.2 Handling of Analog Input Pins

To prevent damage from surges and other abnormal voltages at the analog input pins (AN0-AN7), connect a protection circuit such as that shown in figure 16.8. This circuit also includes a CR filter function that suppresses error due to noise. The circuit shown here is only a design example; circuit constants must be decided on the basis of the actual operating conditions.

Figure 16.9 shows an equivalent circuit for the analog input pins, and table 16.6 summarizes the analog input pin specifications.

Port D Control Register H2 (PDCRH2):

Bit:	15	14	13	12	11	10	9	8
	PD23 MD1	PD23 MD0	PD22 MD1	PD22 MD0	PD21 MD1	PD21 MD0	PD20 MD1	PD20 MD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PD19 MD1	PD19 MD0	PD18 MD1	PD18 MD0	PD17 MD1	PD17 MD0	PD16 MD1	PD16 MD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 and 14—PD23 Mode 1, 0 (PD23MD1 and PD23MD0): These bits select the function of the PD23/D23/$\overline{\text{IRQ7}}$ pin.

Bit 15: PD23MD1	Bit 14: PD23MD0	Description
0	0	General input/output (PD23) (initial value) (D23 with no ROM and CS0 = 32 bit width)
	1	Data input/output (D23) (PD23 in single chip mode)
1	0	Interrupt request input ($\overline{\text{IRQ7}}$)
	1	Reserved

- Bits 13 and 12—PD22 Mode 1, 0 (PD22MD1 and PD22MD0): These bits select the function of the PD22/D22/$\overline{\text{IRQ6}}$ pin.

Bit 13: PD22MD1	Bit 12: PD22MD0	Description
0	0	General input/output (PD22) (initial value) (D22 with no ROM and CS0 = 32 bit width)
	1	Data input/output (D22) (PD22 in single chip mode)
1	0	Interrupt request input ($\overline{\text{IRQ6}}$)
	1	Reserved

Section 25 Electrical Characteristics (5V, 28.7 MHz Version)

25.1 Absolute Maximum Ratings

Table 25.1 shows the absolute maximum ratings.

Table 25.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Programmable voltage (ZTAT version only)	V_{PP}	–0.3 to +13.5	V
Input voltage (other than A/D ports)	V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (A/D ports)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog reference voltage (QFP-144 only)	AV_{ref}	–0.3 to AV_{CC} + 0.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75*1	°C
Programming temperature (ZTAT version only)	T_{we}	–20 to +75*2	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: Operating the LSI in excess of the absolute maximum ratings may result in permanent damage.

*1 Normal Products : T_{OPR} = –40 to + 85°C for wide-temperature range products.

*2 Normal Products: T_{we} = –20 to +85°C for wide-temperature range products.

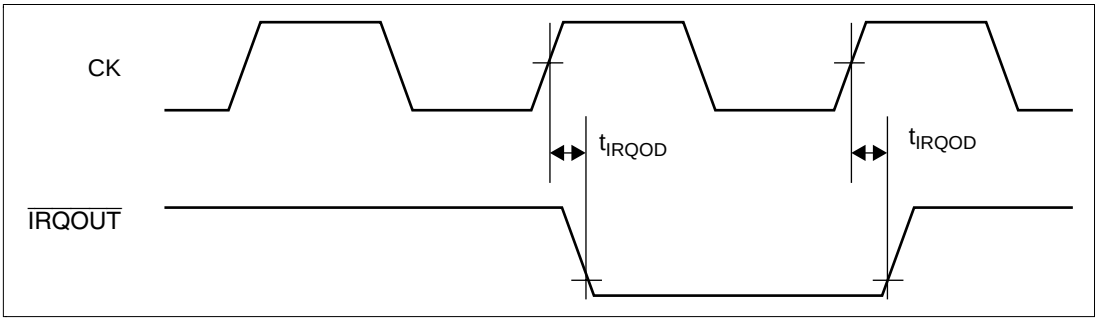
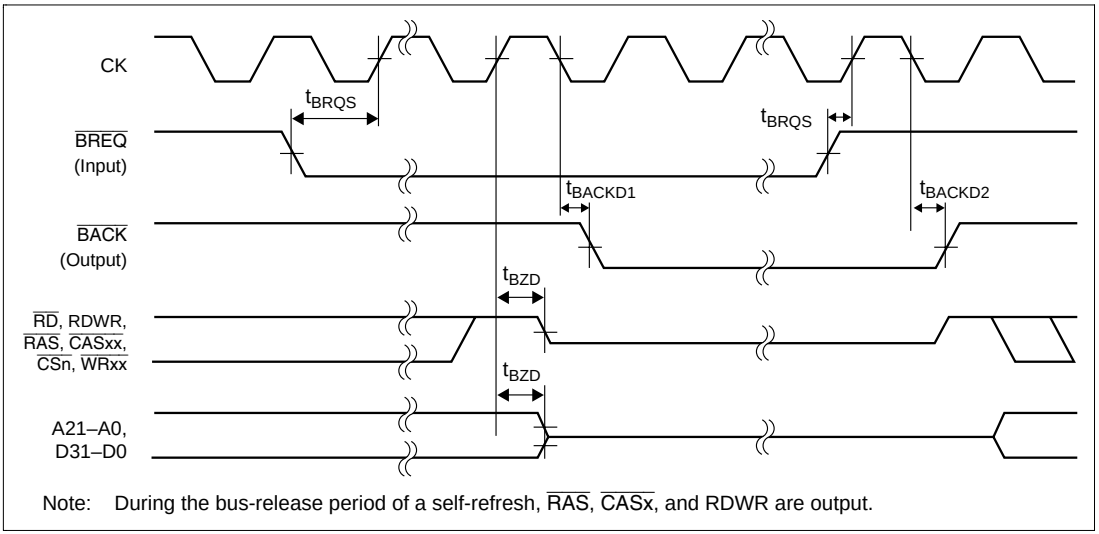


Figure 26.6 Interrupt Signal Output Timing



Note: During the bus-release period of a self-refresh, RAS, CASx, and RDWR are output.

Figure 26.7 Bus Right Release Timing

Table A.1 On-Chip I/O Register Addresses (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF821A	TGR3B									MTU
H'FFFF821B										
H'FFFF821C	TGR4A									
H'FFFF821D										
H'FFFF821E	TGR4B									
H'FFFF821F										
H'FFFF8220	TCNTS									
H'FFFF8221										
H'FFFF8222	TCBR									
H'FFFF8223										
H'FFFF8224	TGR3C									
H'FFFF8225										
H'FFFF8226	TGR3D									
H'FFFF8227										
H'FFFF8228	TGR4C									
H'FFFF8229										
H'FFFF822A	TGR4D									
H'FFFF822B										
H'FFFF822C	TSR3	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
H'FFFF822D	TSR4	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
H'FFFF822E	—	—	—	—	—	—	—	—	—	
H'FFFF822F	—	—	—	—	—	—	—	—	—	
H'FFFF8230 to H'FFFF823F	—	—	—	—	—	—	—	—	—	
H'FFFF8240	TSTR	CST4	CST3	—	—	—	CST2	CST1	CST0	
H'FFFF8241	TSYR	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0	
H'FFFF8242 to H'FFFF825F	—	—	—	—	—	—	—	—	—	
H'FFFF8260	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	
H'FFFF8261	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0	
H'FFFF8262	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
H'FFFF8263	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
H'FFFF8264	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
H'FFFF8265	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
H'FFFF8266	TCNT0									
H'FFFF8267										