Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28.7MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6477042af28v

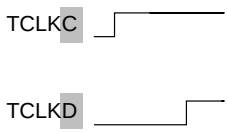
Section	Page	Description
11.2.3 DMA Transfer Count Registers 0–3 (DMATCR0–DMATCR3)	220	Description amended The data for the upper 8 bits of a DMATCR is 0 when read.
11.2.4 DMA Channel Control Registers 0–3 (CHCR0–CHCR3)	221	Description amended • Bits 31–21—Reserved bits: Data are 0 when read. The write value always be 0.
	224	Description amended • Bit 7—Reserved bits: Data is 0 when read. The write value always be 0.
11.2.5 DMAC Operation Register (DMAOR)	226	Description amended • Bits 15–10—Reserved bits: Data are 0 when read. The write value always be 0.
	227	Description amended • Bits 7–3—Reserved bits: Data are 0 when read. The write value always be 0.
11.3.3 Channel Priority Figure 11.3 Round Robin Mode	233	Figure amended Channel 0 is given the lowest priority.
12.4.5 Cascade Connection Mode Figure 12.23 Cascade Connection Operation Example (Phase Counting Mode)	337	Figure amended 
12.4.9 Complementary PWM Mode Figure 12.55 Example of Output Phase Switching by External Input (1)	373	Figure amended **When BDC = 1, N = 0, P = 0, FB = 0, output active level = high**

Table 1.4 Pin Arrangement by Mode for SH7041, SH7043 (QFP-144 Pin)

Pin No.	MCU Mode	PROM Mode
1	PA23/$\overline{\text{WRHH}}$	NC
2	PE14/TIOC4C/DACK0/$\overline{\text{AH}}$	V_{CC}
3	PA22/$\overline{\text{WRHL}}$	NC
4	PA21/$\overline{\text{CASHH}}$	NC
5	PE15/TIOC4D/DACK1/$\overline{\text{IRQOUT}}$	$\overline{\text{CE}}$
6	V_{SS}	V_{SS}
7	PC0/A0	A0
8	PC1/A1	A1
9	PC2/A2	A2
10	PC3/A3	A3
11	PC4/A4	A4
12	V_{CC}	V_{CC}
13	PC5/A5	A5
14	V_{SS}	V_{SS}
15	PC6/A6	A6
16	PC7/A7	A7
17	PC8/A8	A8
18	PC9/A9	NC
19	PC10/A10	A10
20	PC11/A11	A11
21	PC12/A12	A12
22	PC13/A13	A13
23	PC14/A14	A14
24	PC15/A15	A15
25	PB0/A16	A16
26	V_{CC}	V_{CC}
27	PB1/A17	NC
28	V_{SS}	V_{SS}
29	PA20/$\overline{\text{CASHL}}$	NC
30	PA19/$\overline{\text{BACK}}$/DRAK1	NC

Table 2.8 Addressing Modes and Effective Addresses (cont)

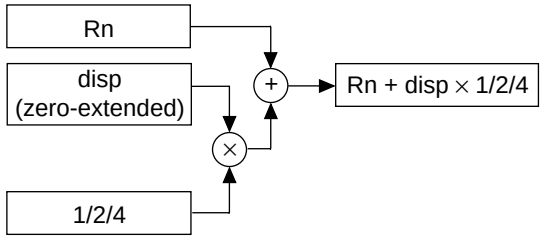
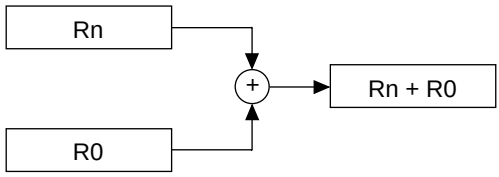
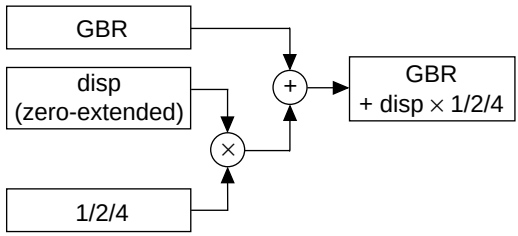
Addressing Mode	Instruction Format	Effective Addresses Calculation	Equation
Indirect register addressing with displacement	@(disp:4, Rn)	The effective address is Rn plus a 4-bit displacement (disp). The value of disp is zero-extended, and remains the same for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation. 	Byte: Rn + disp Word: Rn + disp × 2 Longword: Rn + disp × 4
Indirect indexed register addressing	@(R0, Rn)	The effective address is the Rn value plus R0. 	Rn + R0
Indirect GBR addressing with displacement	@(disp:8, GBR)	The effective address is the GBR value plus an 8-bit displacement (disp). The value of disp is zero-extended, and remains the same for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation. 	Byte: GBR + disp Word: GBR + disp × 2 Longword: GBR + disp × 4

Table 2.13 Arithmetic Operation Instructions (cont)

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
DMULS.L	Rm,Rn	0011nnnnmmmm1101	Signed operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bit	2 to 4*	—
DMULU.L	Rm,Rn	0011nnnnmmmm0101	Unsigned operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bit	2 to 4*	—
DT	Rn	0100nnnn00010000	Rn – 1 → Rn, when Rn is 0, 1 → T. When Rn is nonzero, 0 → T	1	Comparison result
EXTS.B	Rm,Rn	0110nnnnmmmm1110	A byte in Rm is sign-extended → Rn	1	—
EXTS.W	Rm,Rn	0110nnnnmmmm1111	A word in Rm is sign-extended → Rn	1	—
EXTU.B	Rm,Rn	0110nnnnmmmm1100	A byte in Rm is zero-extended → Rn	1	—
EXTU.W	Rm,Rn	0110nnnnmmmm1101	A word in Rm is zero-extended → Rn	1	—
MAC.L	@Rm+,@Rn+	0000nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 32 × 32 → 64 bit	3/(2 to 4)*	—
MAC.W	@Rm+,@Rn+	0100nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 16 × 16 + 64 → 64 bit	3/(2)*	—
MUL.L	Rm,Rn	0000nnnnmmmm0111	Rn × Rm → MACL, 32 × 32 → 32 bit	2 to 4*	—
MULS.W	Rm,Rn	0010nnnnmmmm1111	Signed operation of Rn × Rm → MAC 16 × 16 → 32 bit	1 to 3*	—
MULU.W	Rm,Rn	0010nnnnmmmm1110	Unsigned operation of Rn × Rm → MAC 16 × 16 → 32 bit	1 to 3*	—
NEG	Rm,Rn	0110nnnnmmmm1011	0–Rm → Rn	1	—
NEGC	Rm,Rn	0110nnnnmmmm1010	0–Rm–T → Rn, Borrow → T	1	Borrow

8.3.2 Activating Sources

The DTC performs write operations to the DTCSR with either interrupt sources or software as its activating sources. Each interrupt source is designated by specific DTER bits to determine whether it becomes an interrupt request to the CPU or a DTC activating source.

When the DISEL bit is 1, an interrupt, established as the DTC activating source, is requested of the CPU after each data transfer in DRC. When the DISEL bit is a 0, a request is made only after the completion of a designated number of data transfers. When the activating source interrupt is requested of the CPU, the corresponding DTER bit is automatically cleared.

In the case of software activation also, when the DISEL bit is a 1, a software DTC activation interrupt (SWDTCE) is requested of the CPU after each data transfer. When the DISEL bit is a 0, a request is made only after the completion of a designated number of data transfers. When no SWDTCE interrupt is requested of the CPU, the SWDTE bit of the DTCSR is automatically cleared. When a request is made of the CPU, the SWDTE bit is maintained as a 1.

When multiple DTC activating sources occur simultaneously, they are accepted and the DTC is activated in accordance with the default priority rankings shown in table 8.2.

Figure 8.3 shows a block diagram of activating source control.

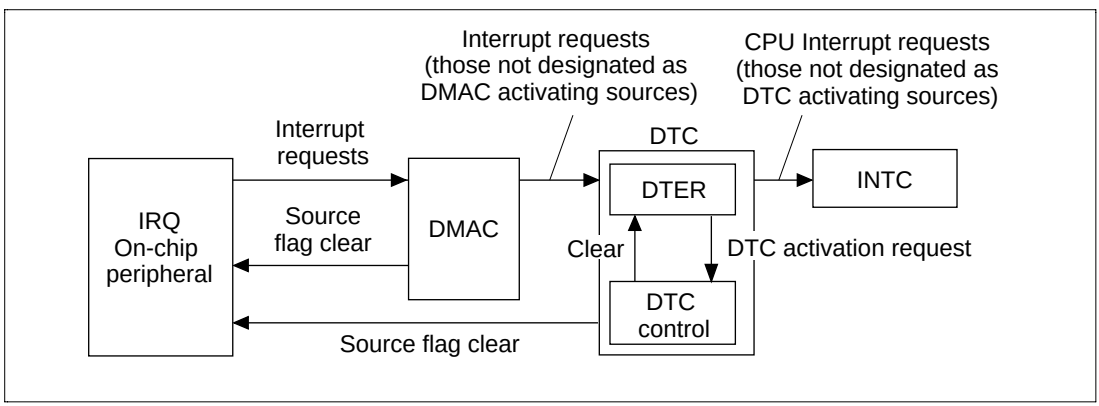


Figure 8.3 Activating Source Control Block Diagram

8.3.3 DTC Vector Table

Figure 8.4 shows the correspondence between DTC vector addresses and register information placement. For each DTC activating source there are 2 bytes in the DTC vector table, which contain the register information start address.

Table 8.2 shows the correspondence between activating sources and vector addresses. When activating with software, the vector address is calculated as H'0400 + DTVEC[7:0].

10.1.5 Address Map

Figure 10.2 shows the address format used by the SH7040 Series.

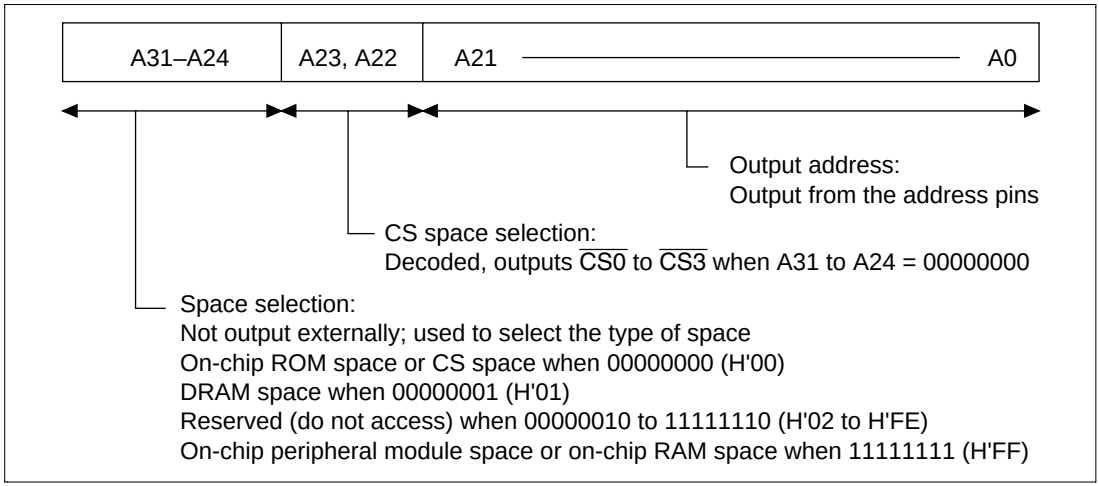


Figure 10.2 Address Format

This LSI uses 32-bit addresses:

- A31–A24 are used to select the type of space and are not output externally.
- Bits A23 and A22 are decoded and output as chip select signals ($\overline{CS0}$–$\overline{CS3}$) for the corresponding areas when bits A31–A24 are 00000000.
- A21–A0 are output externally.

Table 10.3 shows an address map for on-chip ROM effective mode. Table 10.4 shows an address map for on-chip ROM ineffective mode.

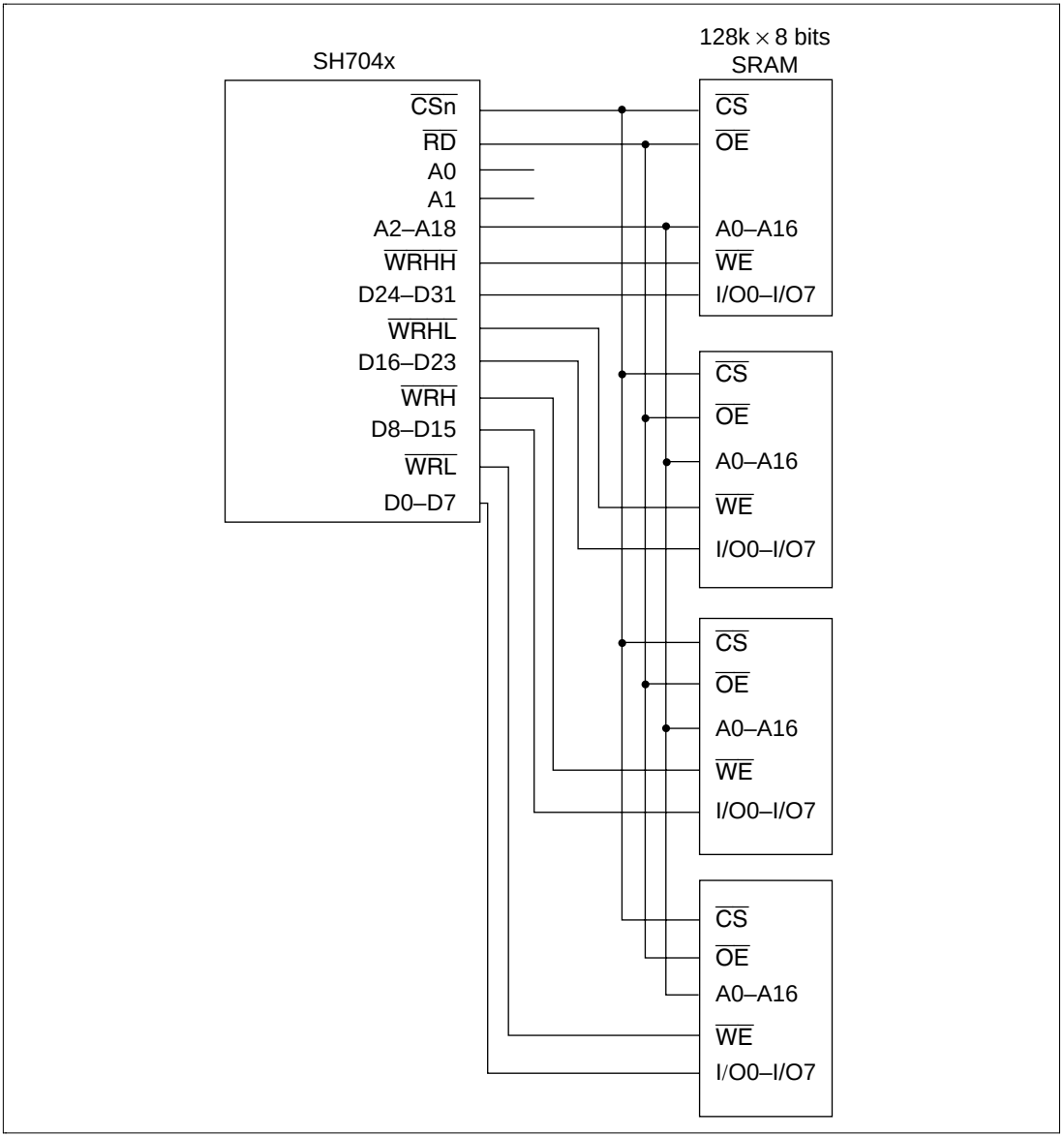


Figure 10.28 32-Bit Data Bus Width SRAM Connection

- Bits 3–0—I/O Control C3–C0 (IOC3–IOC0): These bits set the TGR4C register function.

Bit 3: IOC3	Bit 2: IOC2	Bit 1: IOC1	Bit 0: IOC0	Description		
0	0	0	0	TGR4C	Output disabled (initial value)	
			1	is an	Initial	Output 0 on compare-match
		1	0	output	output	Output 1 on compare-match
			1	compare	is 0	Toggle output on compare-match
	1	0	0	register	Output disabled	
			1		Initial	Output 0 on compare-match
		1	0		output	Output 1 on compare-match
			1		is 1	Toggle output on compare-match
1	0	0	0	TGR4C	Capture	Input capture on rising edge
			1	is an	input source	Input capture on falling edge
		1	0	input	is the	Input capture on both edges
			1	capture	TIOC4C pin	
	1	0	0	register		Input capture on rising edge
			1			Input capture on falling edge
		1	0			Input capture on both edges
			1			

Note: When the BFA bit of TMDR4 is set to 1 and TGR4C is being used as a buffer register, these settings become ineffective and input capture/output compares do not occur.

12.2.4 Timer Interrupt Enable Register (TIER)

The TIER is an 8-bit register that controls the enable/disable of interrupt requests for each channel. The MTU has five TIER registers, one each for channel. TIER is initialized to H'40 by a reset or by standby mode.

Channel 0: TIER0:

Bit:	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value:	0	1	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W

12.4.5 Cascade Connection Mode

Cascade connection mode is a function that connects the 16-bit counters of two channels together to act as a 32-bit counter.

This function operates by using the TPSC2–TPSC0 bits of the TCR register to set the channel 1 counter clock to count by TCNT2 counter overflow/underflow.

Note: When channel 1 is set to phase counting mode, the counter clock settings become ineffective.

Table 12.6 shows the cascade connection combinations.

Table 12.6 Cascade Connection Combinations

Combination	Upper 16 Bits	Lower 16 Bits
Channel 1, channel 2	TCNT1	TCNT2

Procedure for Setting Cascade Connection Mode (Figure 12.22):

1. Set the TPSC2–TPSC 0 bits of the channel 1 timer control register (TCR) to B'111 to select "count by TCNT2 overflow/underflow."
2. Set the CST bits corresponding to the upper and lower 16 bits in the TSTR to 1 to start the count operation.

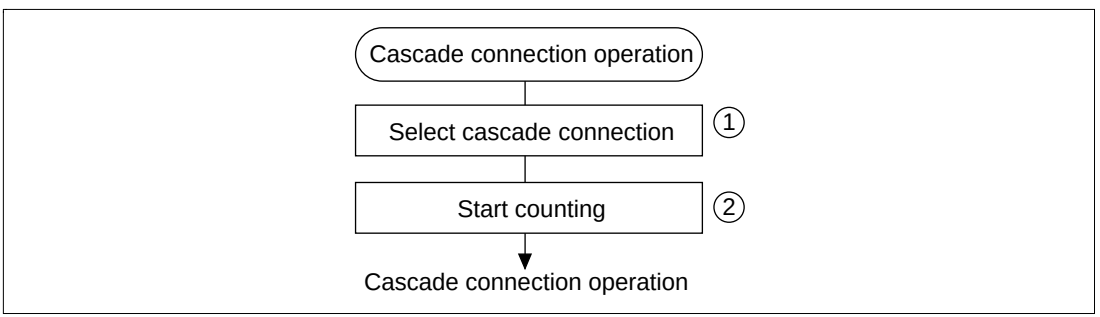


Figure 12.22 Procedure for Selecting Cascade Connection Mode

12.7.7 Contention between TGR Write and Input Capture

If an input capture signal is issued in the T_2 state of the TGR read cycle, input capture has priority, and TGR write does not occur (figure 12.82).

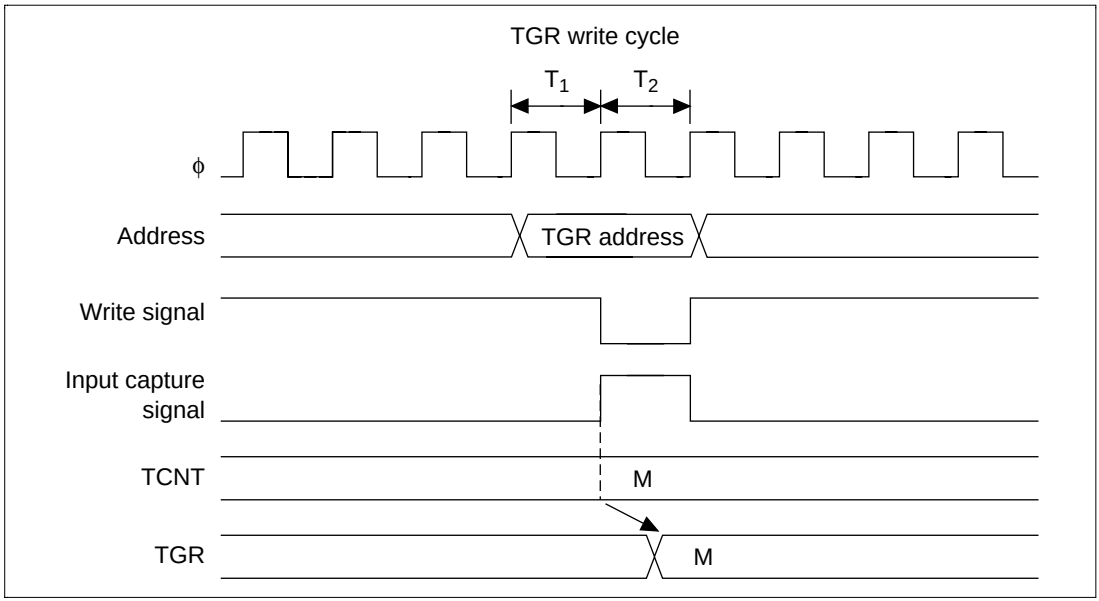


Figure 12.82 TGR Write and Input Capture Contention

12.10 POE Register Descriptions

12.10.1 Input Level Control/Status Register (ICSR)

The input level control/status register (ICSR) is a 16-bit read/write register that selects the $\overline{\text{POE0}}$–$\overline{\text{POE3}}$ pin input modes, controls the enable/prohibit of interrupts, and indicates status. If any of the POE3F–POE0F bits are set to 1, the high current pins become high impedance state.

ICSR is initialized to H'0000 by power-on resets; however, it is not initialized for manual resets, standby mode, or sleep mode, so the previous data is maintained.

Bit:	15	14	13	12	11	10	9	8
	POE3F	POE2F	POE1F	POE0F	—	—	—	PIE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R	R/W

Bit:	7	6	5	4	3	2	1	0
	POE3M1	POE3M0	POE2M1	POE2M0	POE1M1	POE1M0	POE0M1	POE0M0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Only 0 writes are possible to clear the flags.

- Bit 15—POE3 Flag (POE3F): This flag indicates that a high impedance request has been input to the $\overline{\text{POE3}}$ pin.

Bit 15: POE3F	Description
0	Clear condition: By writing 0 to POE3F after reading a POE3F = 1 (initial value)
1	Set condition: When the input set by ICSR bits 7 and 6 occurs at the $\overline{\text{POE3}}$ pin

- Bit 14—POE2 Flag (POE2F): This flag indicates that a high impedance request has been input to the $\overline{\text{POE2}}$ pin.

Bit 14: POE2F	Description
0	Clear condition: By writing 0 to POE2F after reading a POE2F = 1 (initial value)
1	Set condition: When the input set by ICSR bits 5 and 4 occurs at the $\overline{\text{POE2}}$ pin

12.10.2 Output Level Control/Status Register (OCSR)

The output level control/status register (OCSR) is a 16-bit read/write register that controls the enable/disable of both output level comparison and interrupts, and indicates status. If the OSF bit is set to 1, the high current pins become high impedance.

OCSR is initialized to H'0000 by an external power-on reset; however, it is not initialized for manual resets, reset by WDT standby mode, or sleep mode, so the previous data is maintained.

Bit:	15	14	13	12	11	10	9	8
	OSF	—	—	—	—	—	OCE	OIE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R	R	R	R	R	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Note: * Only 0 writes are possible to clear the flag.

- Bit 15—Output Short Flag (OSF): This flag indicates that among the three pairs of 2 phase outputs compared, the outputs of at least one pair have simultaneously become Low level output.

Bit 15: OSF	Description
0	Clear condition: By writing 0 to OSF after reading an OSF = 1 (initial value)
1	Set condition: When any one pair of the 2-phase outputs simultaneously become Low level

- Bits 14–10—Reserved: These bits always read as 0. The write value should always be 0.

14.5.3 Break Detection and Processing

Break signals can be detected by reading the RxD pin directly when a framing error (FER) is detected. In the break state, the input from the RxD pin consists of all 0s, so FER is set and the parity error flag (PER) may also be set. In the break state, the SCI receiver continues to operate, so if the FER bit is cleared to 0, it will be set to 1 again.

14.5.4 Sending a Break Signal

The TxD pin becomes a general I/O pin with the I/O direction and level determined by the I/O port data register (DR) and pin function controller (PFC) control register (CR). These conditions allow break signals to be sent. The DR value is substituted for the marking status until the PFC is set. Consequently, the output port is set to initially output a 1. To send a break in serial transmission, first clear the DR to 0, then establish the TxD pin as an output port using the PFC. When TE is cleared to 0, the transmission section is initialized regardless of the present transmission status.

14.5.5 Receive Error Flags and Transmitter Operation (Clock Synchronous Mode Only)

When a receive error flag (ORER, PER, or FER) is set to 1, the SCI will not start transmitting even if TDRE is set to 1. Be sure to clear the receive error flags to 0 before starting to transmit. Note that clearing RE to 0 does not clear the receive error flags.

14.5.6 Receive Data Sampling Timing and Receive Margin in the Asynchronous Mode

In the asynchronous mode, the SCI operates on a base clock of 16 times the bit rate frequency. In receiving, the SCI synchronizes internally with the falling edge of the start bit, which it samples on the base clock. Receive data is latched on the rising edge of the eighth base clock pulse (figure 14.24).

- Sample 32-byte programming program

  The wait time set values (number of loops) are for the case where f = 28.7 MHz. For other frequencies, the set value is given by the following expression:

  Wait time (μs) × f (MHz) ÷ 4

Registers Used

R4 (input): Program data storage address
R5 (input): Programming destination address
R7 (output): OK (normal) or NG (error)
R0-3, 8-13: Work registers

```
FLMCR1          .EQU    H'80
FLMCR2          .EQU    H'81
OK              .EQU    H'0
NG              .EQU    H'1
Wait10u         .EQU    72
Wait50u         .EQU    359
Wait4u          .EQU    29
Wait2u          .EQU    14
Wait200u        .EQU    1435
WDT_TCSR        .EQU    H'FFFF8610
WDT_573u        .EQU    H'A579
SWESET          .EQU    B'01000000
PSU1SET         .EQU    B'00010000
P1SET           .EQU    B'00000001
P1CLEAR         .EQU    B'11111110
PSU1CLEAR       .EQU    B'11101111
PVSET           .EQU    B'00000100
PVCLEAR         .EQU    B'11111011
SWECLEAR        .EQU    B'10111111
MAXVerify       .EQU    1000
;
FlashProgram    .EQU    $
        MOV     #H'01,R2            ; R2 work register (1)
        MOV.L   #PdataBuff,R0       ; Save program data to work area
        MOV     R4,R12
        MOV     #8,R13
COPY_LOOP       .EQU    $
```

Table 24.3 Register States in the Standby Mode

Module	Registers Initialized	Registers that Retain Data	Registers with Undefined Contents
Interrupt controller (INTC)	—	All registers	—
User break controller (UBC)	—	All registers	—
Data transfer controller (DTC)	All registers (excluding transfer data in memory and DTDR)	—	—
Cache memory (CAC)	—	All registers	—
Bus state controller (BSC)	—	All registers	—
Direct memory access controller (DMAC)	• DMA channel control registers 0–3 (CHCR0–CHCR3) • DMA operation register (DMAOR)	—	• DMA source address registers 0–3 (SAR0–SAR3) • DMA destination address registers 0–3 (DAR0–DAR3) • DMA transfer count registers 0–3 (DMATCR0–DMATCR3)
Multifunction timer pulse unit (MTU)	MTU associated registers	POE associated registers	—
Watchdog timer (WDT)	• Bits 7–5 (OVF, WT/$\overline{IT}$, TME) of the timer control status register (TCSR) • Reset control/status register (RSTCSR)	• Bits 2–0 (CKS2–CKS0) of the TCSR • Timer counter (TCNT)	—
Serial communication interface (SCI)	• Receive data register (RDR) • Transmit data register (TDR) • Serial mode register (SMR) • Serial control register (SCR) • Serial status register (SSR) • Bit rate register (BBR)	—	—
A/D converter (A/D)	All registers	—	—
Compare match timer (CMT)	All registers	—	—

25.3.2 Control Signal Timing

Table 25.5 Control Signal Timing (Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75° C)

Item	Symbol	Min	Max	Unit	Figure
$\overline{RES}$ rise/fall	t_{RESr}, t_{RESf}	—	200	ns	25.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
$\overline{MRES}$ pulse width	t_{MRESW}	20	—	t_{cyc}	
NMI rise/fall	t_{NMIr}, t_{NMIf}	—	200	ns	25.5
$\overline{RES}$ setup time*	t_{RESS}	35	—	ns	25.4, 25.5
$\overline{MRES}$ setup time*	t_{MRESS}	35	—	ns	
NMI setup time*	t_{NMIS}	35	—	ns	
$\overline{IRQ7}$–$\overline{IRQ0}$ setup time (edge detection)	t_{IRQES}	35	—	ns	
$\overline{IRQ7}$–$\overline{IRQ0}$ setup time (level detection)	t_{IRQLS}	35	—	ns	
NMI hold time	t_{NMIH}	35	—	ns	25.5
$\overline{IRQ7}$–$\overline{IRQ0}$ hold time	t_{IRQEH}	35	—	ns	
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	—	35	ns	25.6
Bus request setup time	t_{BRQS}	35	—	ns	25.7
Bus acknowledge delay time 1	t_{BACKD1}	—	35	ns	
Bus acknowledge delay time 2	t_{BACKD2}	—	35	ns	
Bus three-state delay time	t_{BZD}	—	35	ns	

Note: * The $\overline{RES}$, $\overline{MRES}$, NMI, $\overline{BREQ}$, and $\overline{IRQ7}$–$\overline{IRQ0}$ signals are asynchronous inputs, but when thesetup times shown here are provided, the signals are considered to have produced changes at clock rise (for $\overline{RES}$, $\overline{MRES}$, $\overline{BREQ}$) or clock fall (for NMI and $\overline{IRQ7}$–$\overline{IRQ0}$). If the setup times are not provided, recognition is delayed until the next clock rise or fall.

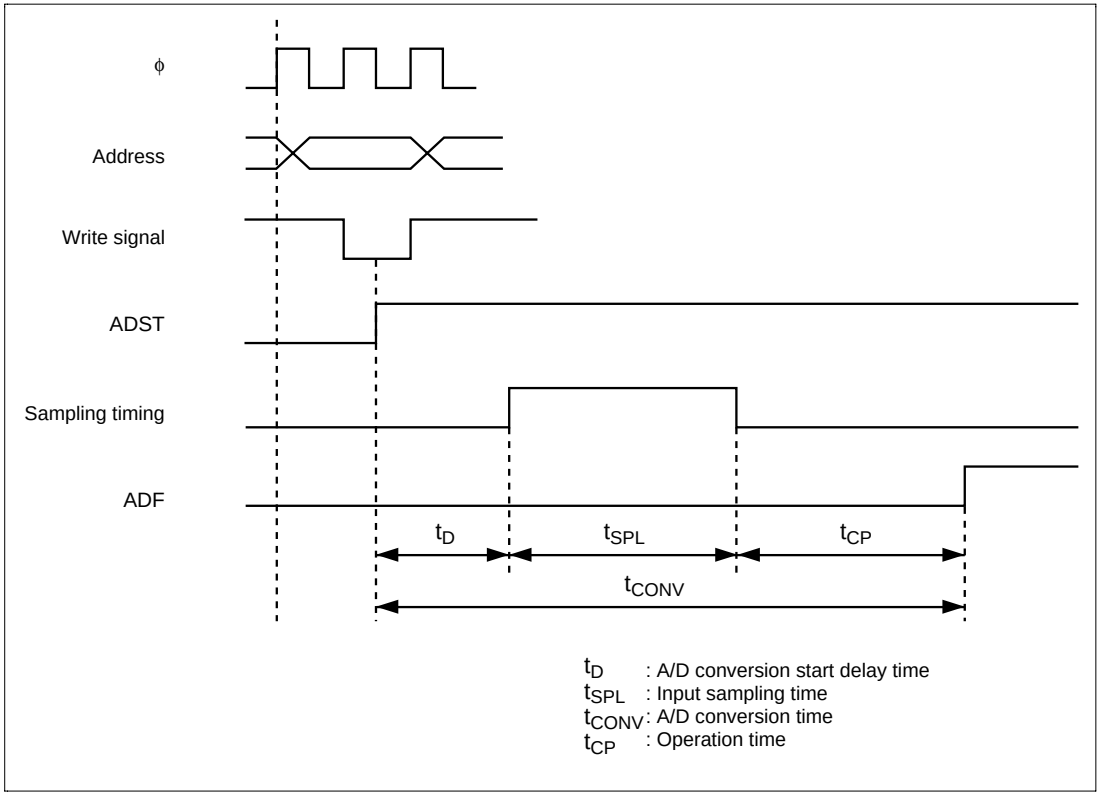


Figure 25.30 Analog Conversion Timing

25.4 A/D Converter Characteristics

Table 25.15 A/D Converter Timing (excluding A mask) (Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = – 20 to +75°C)

	28.7 MHz			
Item	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	Bits
Conversion time (when CKS = 1)	—	—	2.9	µs
Analog input capacitance	—	—	20	pF
Permitted signal source impedance	—	—	1	kΩ
Non-linear error*	—	—	±8	LSB
Offset error*	—	—	±8	LSB
Full-scale error*	—	—	±8	LSB
Quantization error*	—	—	±0.5	LSB
Absolute error (when CKS = 1)	—	—	±15	LSB

Note: * Reference values

Table 25.16 A/D Converter Timing (A mask) (Condition: Vcc=5.0 ± 10%, AVcc=5.0 ± 10%, AVcc=Vcc ± 10%, AVref=4.5V to AVcc, Vss=AVss=0V, Ta=-20 to +75°C)

	28.7 MHz			20 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time (when CKS=0)	—	—	9.3	—	—	13.4	µs
Analog input capacity	—	—	20	—	—	20	pF
Permission signal source impedance	—	—	1	—	—	1	kΩ
Non-linearity error*	—	—	±3	—	—	±3	LSB
Offset error*	—	—	±3	—	—	±3	LSB
Full scale error*	—	—	±3	—	—	±3	LSB
Quantize error*	—	—	±0.5	—	—	±0.5	LSB
Absolute error	—	—	±4	—	—	±4	LSB

Note: * Reference value

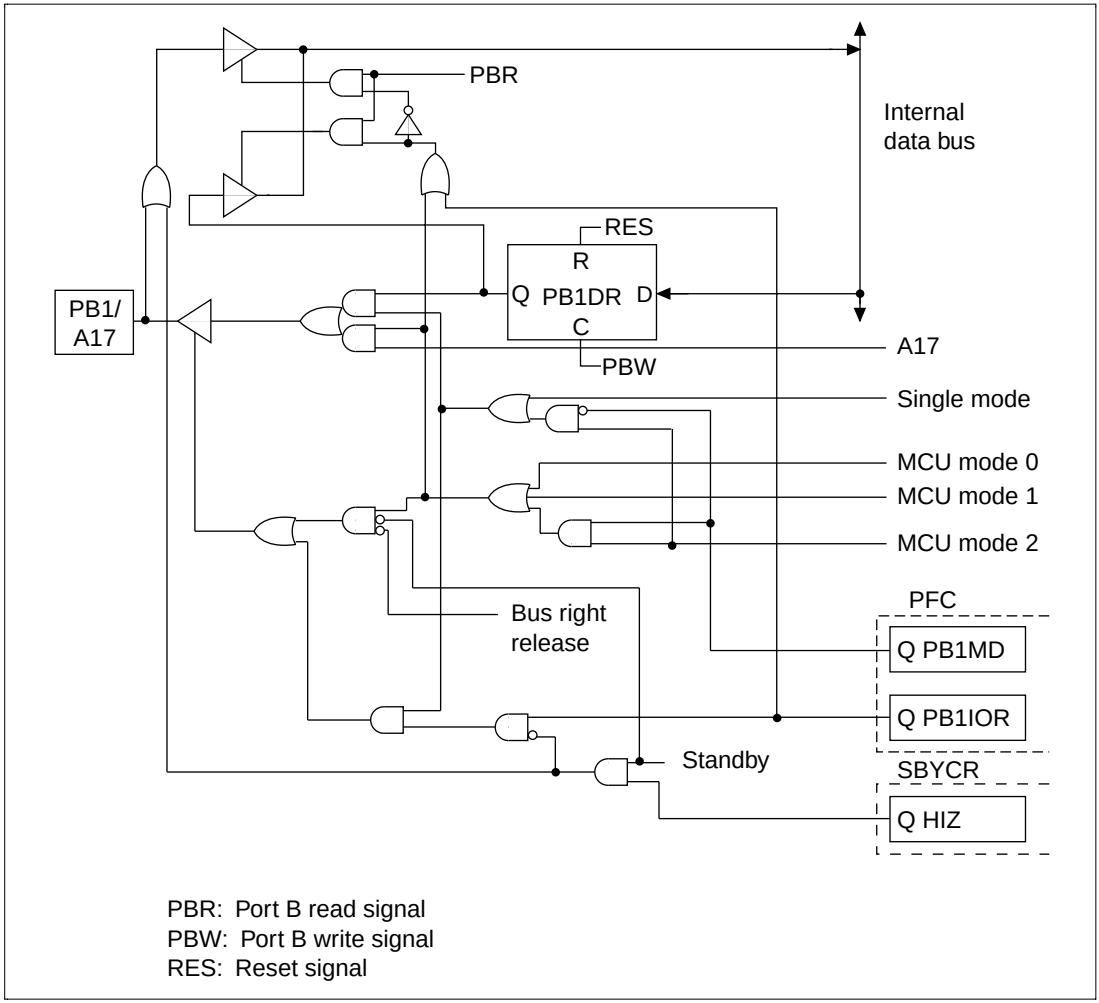


Figure B.16 PB1/A17 Block Diagram