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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28.7MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f7045f28v

1.3.2 Pin Arrangement by Mode

Table 1.2 Pin Arrangement by Mode for SH7040, SH7042 (QFP-112 Pin)

Pin No.	MCU Mode	PROM Mode
1	PE14/TIOC4C/DACK0/$\overline{AH}$	V_{CC}
2	PE15/TIOC4D/DACK1/$\overline{IRQOUT}$	$\overline{CE}$
3	V_{SS}	V_{SS}
4	PC0/A0	A0
5	PC1/A1	A1
6	PC2/A2	A2
7	PC3/A3	A3
8	PC4/A4	A4
9	PC5/A5	A5
10	PC6/A6	A6
11	PC7/A7	A7
12	PC8/A8	A8
13	PC9/A9	NC
14	PC10/A10	A10
15	PC11/A11	A11
16	PC12/A12	A12
17	PC13/A13	A13
18	PC14/A14	A14
19	PC15/A15	A15
20	PB0/A16	A16
21	V_{CC}	V_{CC}
22	PB1/A17	NC
23	V_{SS}	V_{SS}
24	PB2/$\overline{IRQ0}$/$\overline{POE0}$/$\overline{RAS}$	NC
25	PB3/$\overline{IRQ1}$/$\overline{POE1}$/$\overline{CASL}$	$\overline{OE}$
26	PB4/$\overline{IRQ2}$/$\overline{POE2}$/$\overline{CASH}$	$\overline{PGM}$
27	V_{SS}	V_{SS}
28	PB5/$\overline{IRQ3}$/$\overline{POE3}$/RDWR	V_{CC}

Table 1.5 Pin Arrangement by Mode for SH7044 (QFP-112 Pin) (cont)

PinNo.	MCU	Writer mode
33	V_{SS}	V_{SS}
34	PA14/$\overline{RD}$	NC
35	$\overline{WDTOVF}$	NC
36	PA13/$\overline{WRH}$	NC
37	V_{CC}	V_{CC}
38	PA12/$\overline{WRL}$	NC
39	V_{SS}	V_{SS}
40	PA11/$\overline{CS1}$	NC
41	PA10/$\overline{CS0}$	NC
42	PA9/TCLKD/$\overline{IRQ3}$	$\overline{CE}$
43	PA8/TCLKC/$\overline{IRQ2}$	$\overline{OE}$
44	PA7/TCLKB/$\overline{CS3}$	$\overline{WE}$
45	PA6/TCLKA/$\overline{CS2}$	NC
46	PA5/SCK1/$\overline{DREQ1}$/$\overline{IRQ1}$	V_{CC}
47	PA4/TXD1	NC
48	PA3/RXD1	NC
49	PA2/SCK0/$\overline{DREQ0}$/$\overline{IRQ0}$	V_{CC}
50	PA1/TXD0	V_{CC}
51	PA0/RXD0	NC
52	PD15/D15	NC
53	PD14/D14	NC
54	PD13/D13	NC
55	V_{SS}	V_{SS}
56	PD12/D12	NC
57	PD11/D11	NC
58	PD10/D10	NC
59	PD9/D9	NC
60	PD8/D8	NC
61	V_{SS}	V_{SS}
62	PD7/D7	D7
63	PD6/D6	D6
64	PD5/D5	D5

Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range	Default Priority
		Vector No.	Vector Table Address Offset				
SCI1	ERI1	132	H'00000210–H'00000213	0–15 (0)	IPRF (3–0)	High	High
	RXI1	133	H'00000214–H'00000217	0–15 (0)			
	TXI1	134	H'00000218–H'0000021B	0–15 (0)			
	TEI1	135	H'0000021C–H'0000021F	0–15 (0)		Low	
A/D*	ADI	136	H'00000220–H'00000223	0–15 (0)	IPRG (15–12)	—	
DTC	SWDTCE	140	H'00000230–H'00000233	0–15 (0)	IPRG (11–8)	—	
CMT0	CMI0	144	H'00000240–H'00000243	0–15 (0)	IPRG (7–4)	—	
CMT1	CMI1	148	H'00000250–H'00000253	0–15 (0)	IPRG (3–0)	—	
WDT	ITI	152	H'00000260–H'00000263	0–15 (0)	IPRH (15–12)	High	
BSC	CMI	153	H'00000264–H'00000267	0–15 (0)		Low	
I/O	OEI	156	H'00000270–H'00000273	0–15 (0)	IPRH (11–8)	—	Low

Note: * For A mask products, A/D is as follows

A/D	ADI0	136	H'00000220–H'00000223	0–15 (0)	IPRG (15–12)	High
	ADI1	137	H'00000224–H'00000227	0–15 (0)		Low

2. Register settings: UBARH = H'0015
   UBARL = H'389C
   UBBR = H'0058
   Conditions set: Address: H'0015389C
   Bus cycle: CPU, instruction fetch, write
   (operand size not included in conditions)

A user break interrupt does not occur because the instruction fetch cycle is not a write cycle.

3. Register settings: UBARH = H'0003
   UBARL = H'0147
   UBBR = H'0054
   Conditions set: Address: H'00030147
   Bus cycle: CPU, instruction fetch, read
   (operand size not included in conditions)

A user break interrupt does not occur because the instruction fetch was performed for an even address. However, if the first instruction fetch address after the branch is an odd address set by these conditions, user break interrupt exception processing will be done after address error exception processing.

7.4.2 Break on CPU Data Access Cycle

1. Register settings: UBARH = H'0012
   UBARL = H'3456
   UBBR = H'006A
   Conditions set: Address: H'00123456
   Bus cycle: CPU, data access, write, word

A user break interrupt occurs when word data is written into address H'00123456.

2. Register settings: UBARH = H'00A8
   UBARL = H'0391
   UBBR = H'0066
   Conditions set: Address: H'00A80391
   Bus cycle: CPU, data access, read, word

A user break interrupt does not occur because the word access was performed on an even address.

10.1.4 Register Configuration

The BSC has eight registers. These registers are used to control wait states, bus width, and interfaces with memories like DRAM, ROM, and SRAM, as well as refresh control. The register configurations are listed in table 10.2.

All registers are 16 bits. Do not access DRAM space before completing the memory interface settings. All BSC registers are all initialized by a power-on reset, but are not by a manual reset. Values are maintained in standby mode.

Table 10.2 Register Configuration

Name	Abbr.	R/W	Initial Value	Address	Access Size
Bus control register 1	BCR1	R/W	H'200F	H'FFFF8620	8, 16, 32
Bus control register 2	BCR2	R/W	H'FFFF	H'FFFF8622	8, 16, 32
Wait state control register 1	WCR1	R/W	H'FFFF	H'FFFF8624	8, 16, 32
Wait state control register 2	WCR2	R/W	H'000F	H'FFFF8626	8, 16, 32
DRAM area control register	DCR	R/W	H'0000	H'FFFF862A	8, 16, 32
Refresh timer control/status register	RTCSR	R/W	H'0000	H'FFFF862C	8, 16, 32
Refresh timer counter	RTCNT	R/W	H'0000	H'FFFF862E	8, 16, 32
Refresh time constant register	RTCOR	R/W	H'0000	H'FFFF8630	8, 16, 32

- Bits 11–10—DRAM Write Cycle Wait Count (DWW1–DWW0): Specifies the number of DRAM write cycle column address output cycles.

Bit 11 (DWW1)	Bit 10 (DWW0)	Description
0	0	2-cycle (no wait) external wait disabled (initial value)
	1	3-cycle (1 wait) external wait disabled
1	0	4-cycle (2 wait) external wait enabled
	1	5-cycle (3 wait) external wait enabled

- Bits 9–8—DRAM Read Cycle Wait Count (DWR1–DWR0): Specifies the number of DRAM read cycle column address output cycles.

Bit 9 (DWR1)	Bit 8 (DWR0)	Description
0	0	2-cycle (no wait) external wait disabled (initial value)
	1	3-cycle (1 wait) external wait disabled
1	0	4-cycle (2 wait) external wait enabled
	1	5-cycle (3 wait) external wait enabled

- Bit 7—DRAM Idle Cycle Count (DIW): Specifies whether to insert idle cycles, either when accessing a different external space (CS space) or when doing a DRAM write, after DRAM reads.

Bit 7 (DIW)	Description
0	No idle cycles (initial value)
1	1 idle cycle

- Bit 6—Reserved: This bit always reads as 0. The write value should always be 0.
- Bit 5—Burst Enable (BE): Specifies the DRAM operation mode.

Bit 5 (BE)	Description
0	Burst disabled (initial value)
1	DRAM high-speed page mode enabled.

- Bit 4—RAS Down Mode (RASD): Specifies the DRAM operation mode.

Bit 4 (RASD)	Description
0	Access DRAM by RAS up mode (initial value)
1	Access DRAM by RAS down mode

- Bit 0—Refresh Mode (RMD): When the RFSH bit is 1, this bit selects normal refresh or self-refresh. When the RFSH bit is 1, self-refresh mode is entered immediately after the RMD bit is set to 1. When RMD is cleared to 0, a CAS-before-RAS refresh is performed at the interval set in the refresh time constant register (RTCNT).

  When set for self-refresh, the SH7040 Series enters self-refresh mode immediately unless it is in the middle of a DRAM access. If it is, it enters self-refresh mode when the access ends. Refresh requests from the interval timer are ignored in self-refresh mode.

Bit 0 (RMD)	Description
0	CAS-before-RAS refresh (initial value)
1	Self-refresh

10.2.7 Refresh Timer Counter (RTCNT)

RTCNT is a 16-bit read/write register that is used as an 8-bit up counter for refreshes or generating interrupt requests.

RTCNT counts up with the clock selected by the CKS2–CKS0 bits of the RTCSR. RTCNT values can always be read/written by the CPU. When RTCNT matches RTCOR, RTCNT is cleared to H'0000 and the CMF flag of the RTCSR is set to 1. If the RFSH bit of RTCSR is 1 and the RMD bit is 0 at this time, a CAS-before-RAS refresh is performed. Additionally, if the CMIE bit of RTCSR is a 1, a compare match interrupt (CMI) is generated.

Bits 15–8 are reserved and play no part in counter operation. They are always read as 0.

RTCNT is initialized by power-on resets H'0000, but is not initialized by manual resets or software standbys.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

When the processing of a one unit transfer is complete. In a dual address mode direct address transfer, even if an address error occurs or the NMI flag is set during read processing, the transfer will not be halted until after completion of the following write processing. In such a case, SAR, DAR, and TCR values are updated. In the same manner, the transfer is not halted in dual address mode indirect address transfers until after the final write processing has ended.

- When DME is cleared to 0 in DMAOR: Clearing the DME bit to 0 in the DMAOR aborts the transfers on all channels. The TE bit is not set.

11.3.13 DMAC Access from CPU

The space addressed by the DMAC is 3-cycle space. Therefore, when the CPU becomes the bus master and accesses the DMAC, a minimum of three basic clock (CLK) cycles are required for one bus cycle. Also, since the DMAC is located in word space, while a word-size access to the DMAC is completed in one bus cycle, a longword-size access is automatically divided into two word accesses, requiring two bus cycles (six basic clock cycles). These two bus cycles are executed consecutively; a different bus cycle is never inserted between the two word accesses. This applies to both write accesses and read accesses.

11.4 Examples of Use

11.4.1 Example of DMA Transfer between On-Chip SCI and External Memory

In this example, on-chip serial communication interface channel 0 (SCI0) received data is transferred to external memory using the DMAC channel 3.

Table 11.7 indicates the transfer conditions and the setting values of each of the registers.

Table 11.7 Transfer Conditions and Register Set Values for Transfer between On-Chip SCI and External Memory

Transfer Conditions	Register	Value
Transfer source: RDR0 of on-chip SCI0	SAR3	H'FFFF81A5
Transfer destination: external memory	DAR3	H'00400000
Transfer count: 64 times	DMATCR3	H'00000040
Transfer source address: fixed	CHCR3	H'00004D05
Transfer destination address: incremented		
Transfer request source: SCI0 (RDR0)		
Bus mode: cycle steal		
Transfer unit: byte		
Interrupt request generation at end of transfer		
Channel priority ranking: 0 > 1 > 2 > 3	DMAOR	H'0001

- Bit 5—Master Enable TIOC4D (OE4D): Enables or disables the TIOC4D pin MTU output.

Bit 5: OE4D	Description
0	Disable TIOC4D pin MTU output (initial value)
1	Enable TIOC4D pin MTU output

- Bit 4—Master Enable TIOC4C (OE4C): Enables or disables the TIOC4C pin MTU output.

Bit 4: OE4C	Description
0	Disable TIOC4C pin MTU output (initial value)
1	Enable TIOC4C pin MTU output

- Bit 3—Master Enable TIOC3D (OE3D): Enables or disables the TIOC3D pin MTU output.

Bit 3: OE3D	Description
0	Disable TIOC3D pin MTU output (initial value)
1	Enable TIOC3D pin MTU output

- Bit 2—Master Enable TIOC4B (OE4B): Enables or disables the TIOC4B pin MTU output.

Bit 2: OE4B	Description
0	Disable TIOC4B pin MTU output (initial value)
1	Enable TIOC4B pin MTU output

- Bit 1—Master Enable TIOC4A (OE4A): Enables or disables the TIOC4A pin MTU output.

Bit 1: OE4A	Description
0	Disable TIOC4A pin MTU output (initial value)
1	Enable TIOC4A pin MTU output

- Bit 0—Master Enable TIOC3B (OE3B): Enables or disables the TIOC3B pin MTU output.

Bit 0: OE3B	Description
0	Disable TIOC3B pin MTU output (initial value)
1	Enable TIOC3B pin MTU output

13.2.3 Reset Control/Status Register (RSTCSR)

The RSTCSR is an 8-bit readable and writable register. (The RSTCSR differs from other registers in that it is more difficult to write. See section 13.2.4, Register Access, for details.) It controls output of the internal reset signal generated by timer counter (TCNT) overflow and selects the internal reset signal type. RSTCR is initialized to H'1F by input of a reset signal from the $\overline{\text{RES}}$ pin, but is not initialized by the internal reset signal generated by the overflow of the WDT. It is initialized to H'1F in standby mode.

Bit:	7	6	5	4	3	2	1	0
	WOVF	RSTE	RSTS	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/(W)*	R/W	R/W	R	R	R	R	R

Note: * Only 0 can be written in bit 7 to clear the flag.

- Bit 7—Watchdog Timer Overflow Flag (WOVF): Indicates that the TCNT has overflowed (H'FF–H'00) in the watchdog timer mode. It is not set in the interval timer mode.

Bit 7: WOVF	Description
0	No TCNT overflow in watchdog timer mode (initial value) Cleared when software reads WOVF, then writes 0 in WOVF
1	Set by TCNT overflow in watchdog timer mode

- Bit 6—Reset Enable (RSTE): Selects whether to reset the chip internally if the TCNT overflows in the watchdog timer mode.

Bit 6: RSTE	Description
0	Not reset when TCNT overflows (initial value). LSI not reset internally, but TCNT and TCSR reset within WDT.
1	Reset when TCNT overflows

- Bit 5—Reset Select (RSTS): Selects the type of internal reset generated if the TCNT overflows in the watchdog timer mode.

Bit 5: RSTS	Description
0	Power-on reset (initial value)
1	Manual reset

- Bits 4–0—Reserved: These bits always read as 1. The write value should always be 1.

14.5 Notes on Use

Sections 14.5.1 through 14.5.9 provide information for using the SCI.

14.5.1 TDR Write and TDRE Flags

The TDRE bit in the serial status register (SSR) is a status flag indicating loading of transmit data from TDR into TSR. The SCI sets TDRE to 1 when it transfers data from TDR to TSR. Data can be written to TDR regardless of the TDRE bit status. If new data is written in TDR when TDRE is 0, however, the old data stored in TDR will be lost because the data has not yet been transferred to the TSR. Before writing transmit data to the TDR, be sure to check that TDRE is set to 1.

14.5.2 Simultaneous Multiple Receive Errors

Table 14.13 indicates the state of the SSR status flags when multiple receive errors occur simultaneously. When an overrun error occurs, the RSR contents cannot be transferred to the RDR, so receive data is lost.

Table 14.13 SSR Status Flags and Transfer of Receive Data

	SSR Status Flags				Receive Data Transfer
Receive Error Status	**RDRF**	**ORER**	**FER**	**PER**	**RSR → RDR**
Overrun error	1	1	0	0	X
Framing error	0	0	1	0	O
Parity error	0	0	0	1	O
Overrun error + framing error	1	1	1	0	X
Overrun error + parity error	1	1	0	1	X
Framing error + parity error	0	0	1	1	O
Overrun error + framing error + parity error	1	1	1	1	X

Notes: O = Receive data is transferred from RSR to RDR.
X = Receive data is not transferred from RSR to RDR.

15.2 Register Descriptions

15.2.1 A/D Data Registers A–H (ADDRA–ADDRH)

The ADDR are 16-bit read only registers for storing A/D conversion results. There are eight of these registers, ADDRA through ADDRH.

The A/D converted data is 10-bit data which is sent to the ADDR for the corresponding converted channel for storage. The lower 8 bits of the A/D converted data are transferred to and stored in the lower byte (bits 7–0) of the ADDR, and the upper 2 bits are stored into the upper byte (bits 9, 8). Bits 15–10 always read as 0. Data reads can be either byte or word. The upper 8 bits of the converted data are transferred upon byte data reads. Additionally, buffered operation is possible by combining ADDRA–ADDRD.

Table 15.3 shows the correspondence between the analog input channels and the ADDR.

The ADDR are initialized to H'0000 by power-on reset or in standby mode. Manual reset does not initialize ADDR.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	AD9	AD8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

16.1.3 Pin Configuration

Table 16.1 shows the input pins used with the mid-speed A/D converter.

The AV_{CC} and AV_{SS} pins are for the mid-speed A/D converter internal analog section power supply. AVref pin is the A/D conversion standard voltage.

Table 16.1 Pin Configuration

Pin		Abbreviation	I/O	Function
Analog supply		Av_{CC}	I	Analog section power supply
Analog ground		AV_{SS}	I	Analog section ground and A/D conversion standard voltage
Standard voltage		AVref*	I	A/D conversion standard voltage (SH7041A, SH7043A, and SH7045 only)
A/D0	Analog input 0	AND	I	Analog input channel 0
	Analog input 1	AN1	I	Analog input channel 1
	Analog input 2	AN2	I	Analog input channel 2
	Analog input 3	AN3	I	Analog input channel 3
A/D1	Analog input 4	AN4	I	Analog input channel 4
	Analog input 5	AN5	I	Analog input channel 5
	Analog input 6	AN6	I	Analog input channel 6
	Analog input 7	AN7	I	Analog input channel 7
A/D external trigger input		$\overline{\text{ADTRG}}$	I	External trigger for A/D conversion start

Note: * In the SH7040A, SH7042A, and SH7044, AV_{ref} is connected to AV_{CC} internally.

Table 18.2 Pin Arrangement by Mode

Pin NO.			Pin Name								
			On-Chip ROM Disabled				On-Chip ROM Enabled				
			MPU Mode0		MPU Mode 1		MPU Mode2		Single Chip Mode		
TFP120	FP144	FP112	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities	PROM Mode
22, 40, 70, 82, 111	12,26,40,63 77,85,112 135	21,37,65 103	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
4, 24, 28, 36, 42, 58, 66, 76, 97, 108, 117	6,14,28,35 42,55,61,71 79,87,93 117,129,141	3,23,27,33 39,55,61,71 90,101,109	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss
75	92	70	D0	D0	D0	D0	PD0	PD0/D0	PD0	PD0	D0
74	91	69	D1	D1	D1	D1	PD1	PD1/D1	PD1	PD1	D1
73	90	68	D2	D2	D2	D2	PD2	PD2/D2	PD2	PD2	D2
72	89	67	D3	D3	D3	D3	PD3	PD3/D3	PD3	PD3	D3
71	88	66	D4	D4	D4	D4	PD4	PD4/D4	PD4	PD4	D4
69	86	64	D5	D5	D5	D5	PD5	PD5/D5	PD5	PD5	D5
68	84	63	D6	D6	D6	D6	PD6	PD6/D6	PD6	PD6	D6
67	83	62	D7	D7	D7	D7	PD7	PD7/D7	PD7	PD7	D7
65	82	60	D8	D8	D8	D8	PD8	PD8/D8	PD8	PD8	NC
64	81	59	D9	D9	D9	D9	PD9	PD9/D9	PD9	PD9	NC
63	80	58	D10	D10	D10	D10	PD10	PD10/D10	PD10	PD10	NC
62	78	57	D11	D11	D11	D11	PD11	PD11/D11	PD11	PD11	NC
59	76	56	D12	D12	D12	D12	PD12	PD12/D12	PD12	PD12	NC
57	75	54	D13	D13	D13	D13	PD13	PD13/D13	PD13	PD13	NC
56	74	53	D14	D14	D14	D14	PD14	PD14/D14	PD14	PD14	NC
55	73	52	D15	D15	D15	D15	PD15	PD15/D15	PD15	PD15	NC
—	72	—	PD16	PD16/D16/$\overline{\text{IRQ0}}$	D16	D16	PD16	PD16/D16/$\overline{\text{IRQ0}}$	PD16	PD16/$\overline{\text{IRQ0}}$	NC
—	70	—	PD17	PD17/D17/$\overline{\text{IRQ1}}$	D17	D17	PD17	PD17/D17/$\overline{\text{IRQ1}}$	PD17	PD17/$\overline{\text{IRQ1}}$	NC
—	69	—	PD18	PD18/D18/$\overline{\text{IRQ2}}$	D18	D18	PD18	PD18/D18/$\overline{\text{IRQ2}}$	PD18	PD18/$\overline{\text{IRQ2}}$	NC
—	68	—	PD19	PD19/D19/$\overline{\text{IRQ3}}$	D19	D19	PD19	PD19/D19/$\overline{\text{IRQ3}}$	PD19	PD19/$\overline{\text{IRQ3}}$	NC
—	67	—	PD20	PD20/D20/$\overline{\text{IRQ4}}$	D20	D20	PD20	PD20/D20/$\overline{\text{IRQ4}}$	PD20	PD20/$\overline{\text{IRQ4}}$	NC
—	66	—	PD21	PD21/D21/$\overline{\text{IRQ5}}$	D21	D21	PD21	PD21/D21/$\overline{\text{IRQ5}}$	PD21	PD21/$\overline{\text{IRQ5}}$	NC
—	65	—	PD22	PD22/D22/$\overline{\text{IRQ6}}$	D22	D22	PD22	PD22/D22/$\overline{\text{IRQ6}}$	PD22	PD22/$\overline{\text{IRQ6}}$	NC
—	64	—	PD23	PD23/D23/$\overline{\text{IRQ7}}$	D23	D23	PD23	PD23/D23/$\overline{\text{IRQ7}}$	PD23	PD23/$\overline{\text{IRQ7}}$	NC
—	62	—	PD24	PD24/D24/$\overline{\text{DREQ0}}$	D24	D24	PD24	PD24/D24/$\overline{\text{DREQ0}}$	PD24	PD24	NC
—	60	—	PD25	PD25/D25/$\overline{\text{DREQ1}}$	D25	D25	PD25	PD25/D25/$\overline{\text{DREQ1}}$	PD25	PD25	NC
—	59	—	PD26	PD26/D26/DACK0	D26	D26	PD26	PD26/D26/DACK0	PD26	PD26	NC
—	58	—	PD27	PD27/D27/DACK1	D27	D27	PD27	PD27/D27/DACK1	PD27	PD27	NC
—	57	—	PD28	PD28/D28/$\overline{\text{CS2}}$	D28	D28	PD28	PD28/D28/$\overline{\text{CS2}}$	PD28	PD28	NC
—	56	—	PD29	PD29/D29/$\overline{\text{CS3}}$	D29	D29	PD29	PD29/D29/$\overline{\text{CS3}}$	PD29	PD29	NC
—	46	—	PD30	PD30/D30/$\overline{\text{IRQOUT}}$	D30	D30	PD30	PD30/D30/$\overline{\text{IRQOUT}}$	PD30	PD30	NC
—	45	—	PD31	PD31/D31/$\overline{\text{ADTRG}}$	D31	D31	PD31	PD31/D31/$\overline{\text{ADTRG}}$	PD31	PD31/$\overline{\text{ADTRG}}$	NC
5	7	4	A0	A0	A0	A0	PC0	PC0/A0	PC0	PC0	A0
6	8	5	A1	A1	A1	A1	PC1	PC1/A1	PC1	PC1	A1
7	9	6	A2	A2	A2	A2	PC2	PC2/A2	PC2	PC2	A2
8	10	7	A3	A3	A3	A3	PC3	PC3/A3	PC3	PC3	A3
9	11	8	A4	A4	A4	A4	PC4	PC4/A4	PC4	PC4	A4
10	13	9	A5	A5	A5	A5	PC5	PC5/A5	PC5	PC5	A5
11	15	10	A6	A6	A6	A6	PC6	PC6/A6	PC6	PC6	A6
12	16	11	A7	A7	A7	A7	PC7	PC7/A7	PC7	PC7	A7
13	17	12	A8	A8	A8	A8	PC8	PC8/A8	PC8	PC8	A8
14	18	13	A9	A9	A9	A9	PC9	PC9/A9	PC9	PC9	NC
15	19	14	A10	A10	A10	A10	PC10	PC10/A10	PC10	PC10	A10
16	20	15	A11	A11	A11	A11	PC11	PC11/A11	PC11	PC11	A11
17	21	16	A12	A12	A12	A12	PC12	PC12/A12	PC12	PC12	A12

19.5.2 Port D Data Register H (PDDRH)

PDDRH is a 16-bit read/write register that stores data for port D. The bits PD31DR–PD16DR correspond to the PD31/D31/$\overline{\text{ADTRG}}$–PD16/D16/$\overline{\text{IRQ0}}$ pins. When the pins are used as ordinary outputs, they will output whatever value is written in the PDDRH; when PDDRH is read, the register value will be read regardless of the pin status. When the pins are used as ordinary inputs, the pin status rather than the register value is read directly when PDDRH is read. When a value is written to PDDRH, that value can be written into PDDRH, but it will not affect the pin status. Table 19.14 shows the read/write operations of the port D data register.

PDDRH is initialized by an external power-on reset. However, PDDRH is not initialized for a manual reset, reset by WDT, standby mode, or sleep mode.

These register settings function only for the 144-pin version. There are no pins corresponding to this register in the 112-pin version. However, read/writes are possible.

Bit:	15	14	13	12	11	10	9	8
	PD31DR	PD30DR	PD29DR	PD28DR	PD27DR	PD26DR	PD25DR	PD24DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PD23DR	PD22DR	PD21DR	PD20DR	PD19DR	PD18DR	PD17DR	PD16DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- User Program Mode

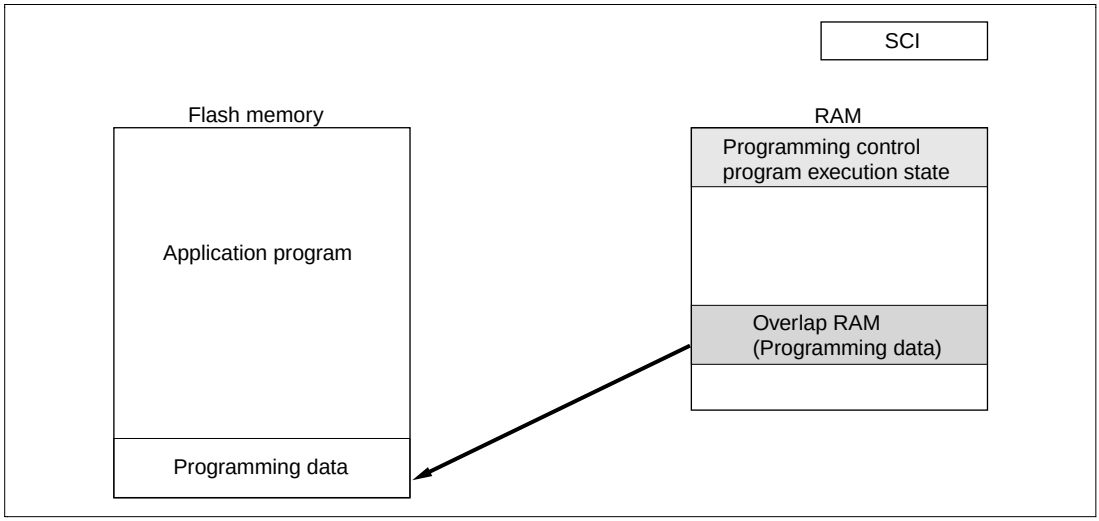

Figure 22.6 Programming to the Flash Memory

22.2.5 Differences between Boot Mode and User Program Mode

Table 22.1 Differences between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	(2)	(1) (2) (3)

(1) Erase/erase-verify

(2) Program/program-verify

(3) Emulation

Note: * To be prepared by the user according to the recommended algorithm.

26.3.7 Watchdog Timer Timing

Table 26.11 Watchdog Timer Timing (Conditions: V_{CC} = 3.0* to 3.6V, AV_{CC} = 3.0* to 3.6V, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 3.0* to AV_{CC}, V_{SS} = AV_{SS} = 0V, T_a = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	26.26

Note: * SH7042/43 ZTAT (excluding A mask) are 3.2V.

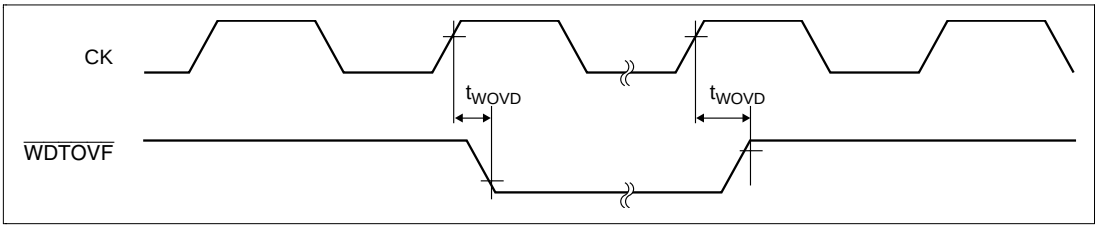

Figure 26.26 Watchdog Timer Timing

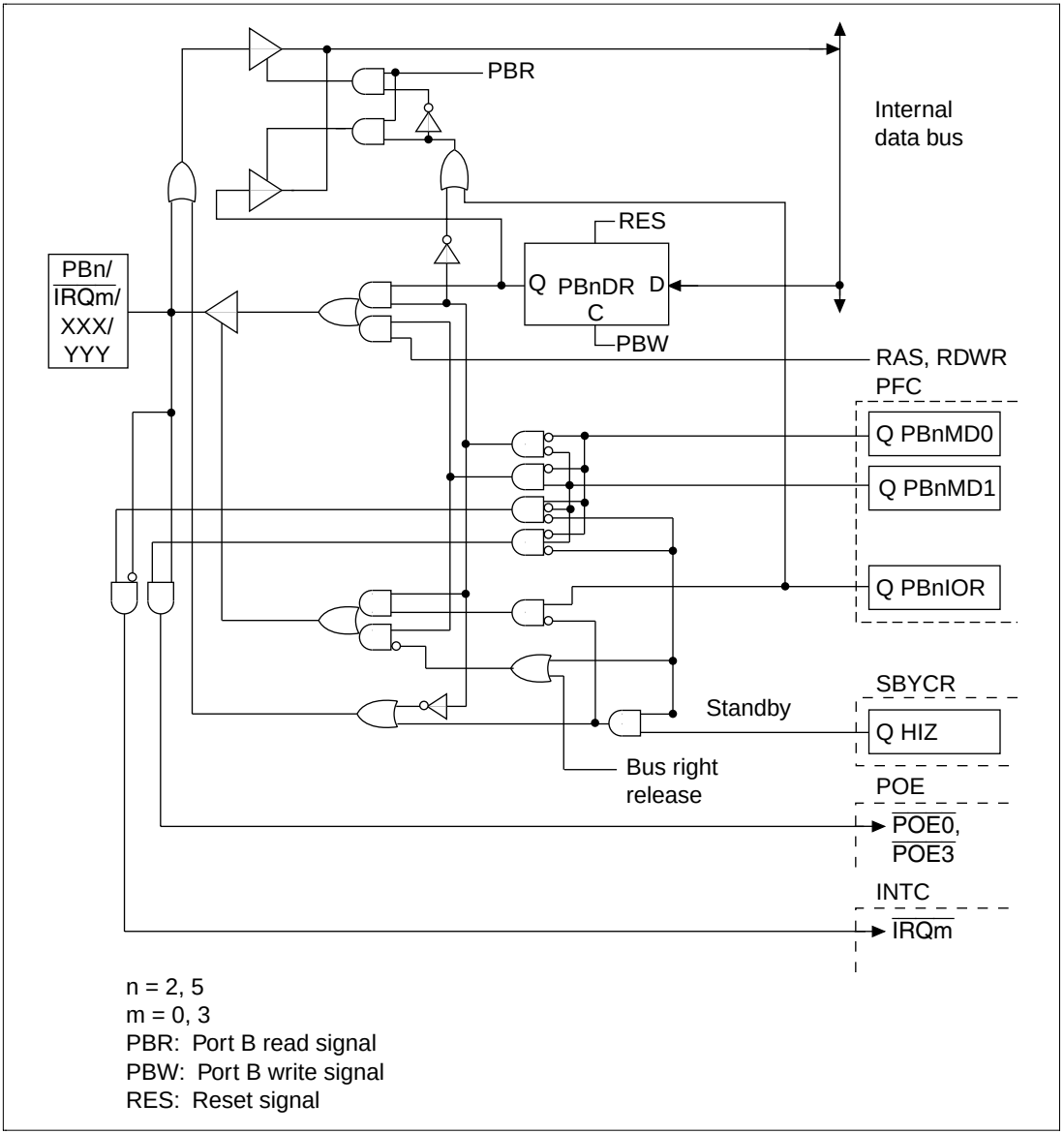

Figure B.21 PBn/IRQm/XXXX/YYYY Block Diagram

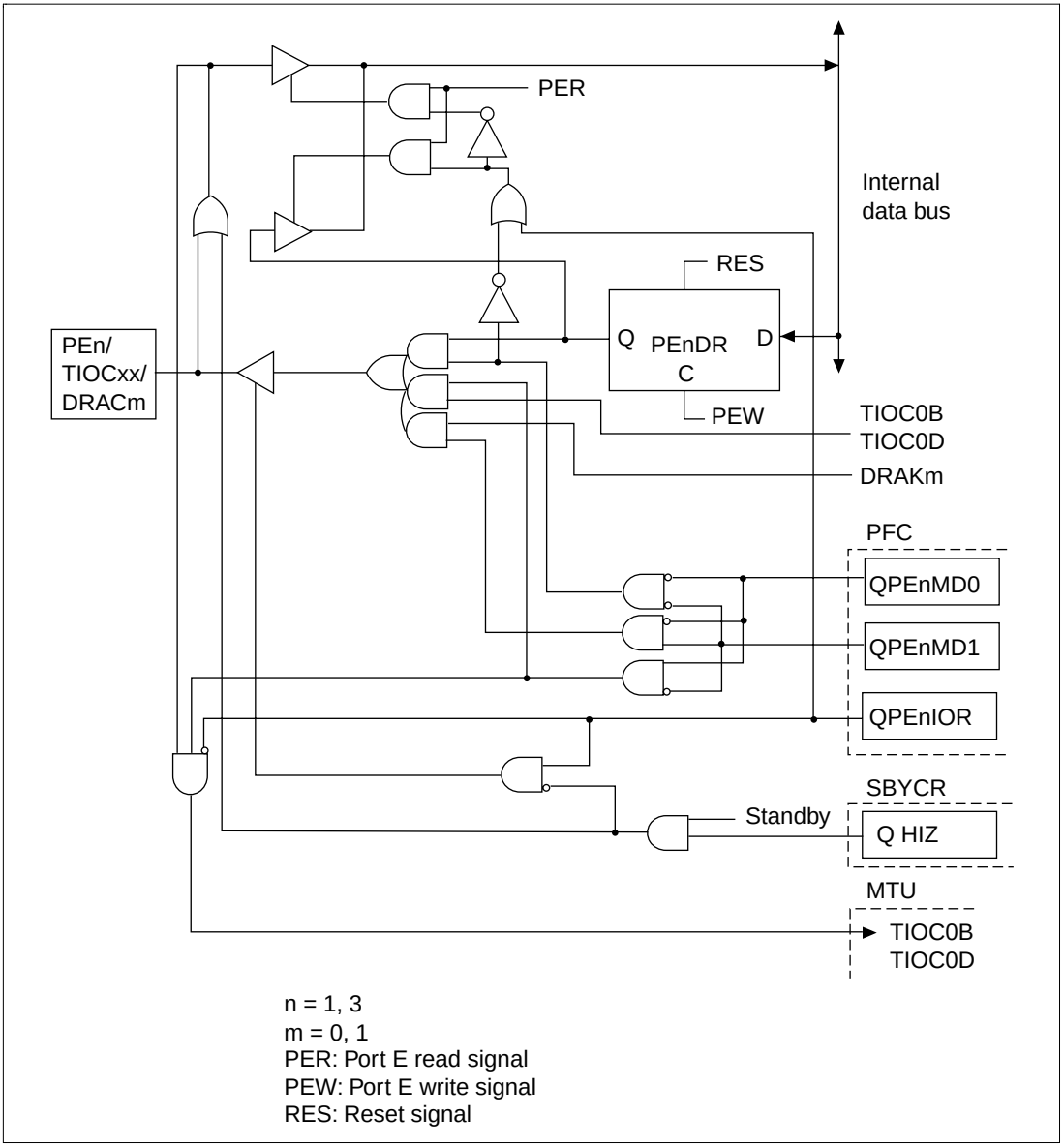

Figure B.37 PEn/TIOCXX/DRAKm Block Diagram