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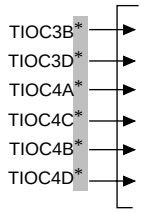
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28.7MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f7045fi28v

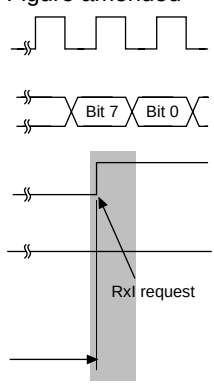
Section	Page	Description
12.9.2 Block Diagram Figure 12.125 POE Block Diagram	444	Note added  Note: * Includes multiplexed pins.
12.11.5 Usage Notes	453	Section added
14.2.8 Bit Rate Register (BRR) Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)	491	Table amended

Bit Rate (Bits/s)	27.0336		
	n	N	Error (%)
110	3	119	0.00
150	3	87	0.00
300	2	175	0.00
600	1	87	0.00
1200	1	175	0.00
2400	1	87	0.00
4800	0	175	0.00
9600	0	87	0.00
14400	0	58	–0.56
19200	0	43	0.00
28800	0	28	1.15
31250	0	26	0.12
38400	0	21	0.00

Table 14.4 Bit Rates and BRR Settings in Clocked Synchronous Mode (cont)	495	Table amended

3.5M	—	—	—	—	0	1
5M	0	0*	—	—	—	—
7M			—	—	0	0*

14.3.4 Clock Synchronous Operation Figure 14.22 Example of SCI Receive Operation	529	Figure amended



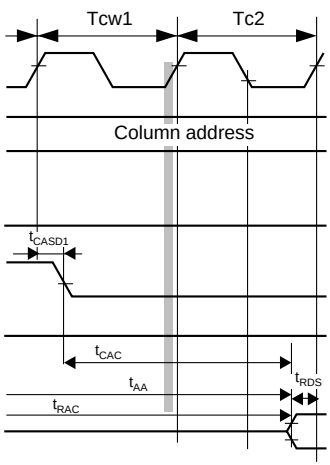
Section	Page	Description
25.4 A/D Converter Characteristics Table 25.16 A/D Converter Timing (A mask)	779	Table amended Non-linearity error* Offset error* Full scale error* Quantize error*
26.2 DC Characteristics Table 26.2 DC Characteristics	782	Table amended Schmitt trigger input voltage — PA2, PA5, PA6–PA9, PE0–PE15 — $V_T^+ - V_T^-$ — $V_{CC}\times 0.07$ — — V — $VT^+ \geq V_{CC}\times 0.9V$ (min); $VT^- \leq V_{CC}\times 0.2V$ (max)
	783	Table amended Analog supply current — AI_{CC} — — 4 8 mA f = 16.7MHz AI_{ref} — — 0.5 1*3 mA QFP144 version only *3 2 mA in the A mask version of MASK products.
26.3.2 Control Signal Timing Table 26.5 Control Signal Timing	786	Note amended Notes: *1 SH7042/43 ZTAT (excluding A mask) are 3.2V. *2 The $\overline{RES}$, $\overline{MRES}$, NMI, $\overline{BREQ}$, and $\overline{IRQ7}$–$\overline{IRQ0}$ signals are asynchronous inputs, but when the setup times shown here are provided, the signals are considered to have produced changes at clock rise (for $\overline{RES}$, $\overline{MRES}$, $\overline{BREQ}$) or clock fall (for NMI and $\overline{IRQ7}$–$\overline{IRQ0}$). If the setup times are not provided, recognition is delayed until the next clock rise or fall.
26.3.3 Bus Timing Figure 26.12 DRAM Cycle (Normal Mode, 1 Wait, TPC = 0, RCD = 0)	795	Figure amended 

Table 1.5 Pin Arrangement by Mode for SH7044 (QFP-112 Pin) (cont)

PinNo.	MCU	Writer mode
65	V_{CC}	V_{CC}
66	PD4/D4	D4
67	PD3/D3	D3
68	PD2/D2	D2
69	PD1/D1	D1
70	PD0/D0	D0
71	V_{SS}	V_{SS}
72	XTAL	XTAL
73	MD3	MD3
74	EXTAL	EXTAL
75	MD2	MD2
76	NMI	V_{CC}
77	V_{CC} (FWP)*	FWE
78	MD1	MD1
79	MD0	MD0
80	$PLLV_{CC}$	$PLLV_{CC}$
81	PLLCAP	PLLCAP
82	$PLLV_{SS}$	$PLLV_{SS}$
83	PA15/CK	NC
84	$\overline{RES}$	$\overline{RES}$
85	PE0/TIOCA/$\overline{DREQ0}$	NC
86	PE1/TIOCB/DRAK0	NC
87	PE2/TIOCC/$\overline{DREQ1}$	NC
88	PE3/TIOCD/DRAK1	NC
89	PE4/TIOC1A	NC
90	V_{SS}	V_{SS}
91	PF0/AN0	V_{SS}
92	PF1/AN1	V_{SS}
93	PF2/AN2	V_{SS}
94	PF3/AN3	V_{SS}
95	PF4/AN4	V_{SS}
96	PF5/AN5	V_{SS}

Note: * V_{CC} in the mask version; FWP in the F-ZTAT version (however, FWE in the writer mode)

Table 2.12 Data Transfer Instructions (cont)

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
MOV.W	Rm,@(R0,Rn)	0000nnnnmmmm0101	Rm → (R0 + Rn)	1	—
MOV.L	Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B	@(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W	@(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L	@(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B	R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W	R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L	R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B	@(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W	@(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L	@(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA	@(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT	Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B	Rm,Rn	0110nnnnmmmm1000	Rm → Swap the bottom two bytes → Rn	1	—
SWAP.W	Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT	Rm,Rn	0010nnnnmmmm1101	Rm: Middle 32 bits of Rn → Rn	1	—

- Bits 3–2—DRAM Bus Width Specification (SZ1, SZ0): Specifies the DRAM space bus width.

Bit 3 (SZ1)	Bit 2 (SZ0)	Description
0	0	Byte (8 bits) (initial value)
	1	Word (16 bits)
1	Don't care	Longword (32 bits)

- Bits 1–0—DRAM Address Multiplex (AMX1–AMX0): Specifies the DRAM address multiplex count.

Bit 1 (AMX1)	Bit 0 (AMX0)	Description
0	0	9 bit (initial value)
	1	10 bit
1	0	11 bit
	1	12 bit

10.2.6 Refresh Timer Control/Status Register (RTCSR)

RTCSR is a 16-bit read/write register that selects the refresh mode and the clock input to the refresh timer counter (RTCNT), and controls compare match interrupts (CMI).

RTCSR is initialized by power-on resets and hardware standbys to H'0000, but is not initialized by manual resets or software standbys.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	CMF	CMIE	CKS2	CKS1	CKS0	RFSH	RMD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15–7—Reserved: These bits always read as 0. The write value should always be 0.

- Bits 11–8—Resource Select 3–0 (RS3–RS0): These bits specify the transfer request source.

Bit 11: RS3	Bit 10: RS2	Bit 9: RS1	Bit 8: RS0	Description
0	0	0	0	External request, dual address mode (initial value)
0	0	0	1	Prohibited
0	0	1	0	External request, single address mode. External address space → external device.
0	0	1	1	External request, single address mode. External device → external address space.
0	1	0	0	Auto-request
0	1	0	1	Prohibited
0	1	1	0	MTU TGI0A
0	1	1	1	MTU TGI1A
1	0	0	0	MTU TGI2A
1	0	0	1	MTU TGI3A
1	0	1	0	MTU TGI4A
1	0	1	1	A/D ADI*
1	1	0	0	SCI0 TXI0
1	1	0	1	SCI0 RXI0
1	1	1	0	SCI1 TXI1
1	1	1	1	SCI1 RXI1

Notes: External request designations are valid only for channels 0 and 1. No transfer request sources can be set for channels 2 or 3.

* ADI1 for A mask.

- Bit 7—Reserved bits: Data is 0 when read. The write value always be 0.
- Bit 6—$\overline{\text{DREQ}}$ Select (DS): Sets the sampling method for the $\overline{\text{DREQ}}$ pin in external request mode to either low-level detection or falling-edge detection. This bit is valid only with CHCR0 and CHCR1. For CHCR2 and CHCR3, this bit always reads as 0 and cannot be modified.

  Even with channels 0 and 1, when specifying an on-chip peripheral module or auto-request as the transfer request source, this bit setting is ignored. The sampling method is fixed at falling-edge detection in cases other than auto-request.

Bit 6: DS	Description
0	Low-level detection (initial value)
1	Falling-edge detection

- Example of AC synchronous motor (brushless DC motor) drive waveform output

  In complementary PWM mode, a brushless DC motor can easily be controlled using the timer gate control register (TGCR). Figures 12.55 to 12.58 show examples of brushless DC motor drive waveforms created using TGCR.

  When output phase switching for a 3-phase brushless DC motor is performed by means of external signals detected with a Hall element, etc., clear the FB bit in TGCR to 0. In this case, the external signals indicating the polarity position are input to channel 0 timer input pins TIOC0A, TIOC0B, and TIOC0C (set with PFC). When an edge is detected at pin TIOC0A, TIOC0B, or TIOC0C, the output on/off state is switched automatically.

  When the FB bit is 1, the output on/off state is switched when the UF, VF, or WF bit in TGCR is cleared to 0 or set to 1.

  The drive waveforms are output from the complementary PWM mode 6-phase output pins. With this 6-phase output, in the case of on output, it is possible to use complementary PWM mode output and perform chopping output by setting the N bit or P bit to 1. When the N bit or P bit is 0, level output is selected.

  The 6-phase output active level (on output level) can be set with the OLSN and OLSP bits in the timer output control register (TOCR) regardless of the setting of the N and P bits. When using this mode, set the 6-phase output waveform to High active (Low active is also permitted for A masks).

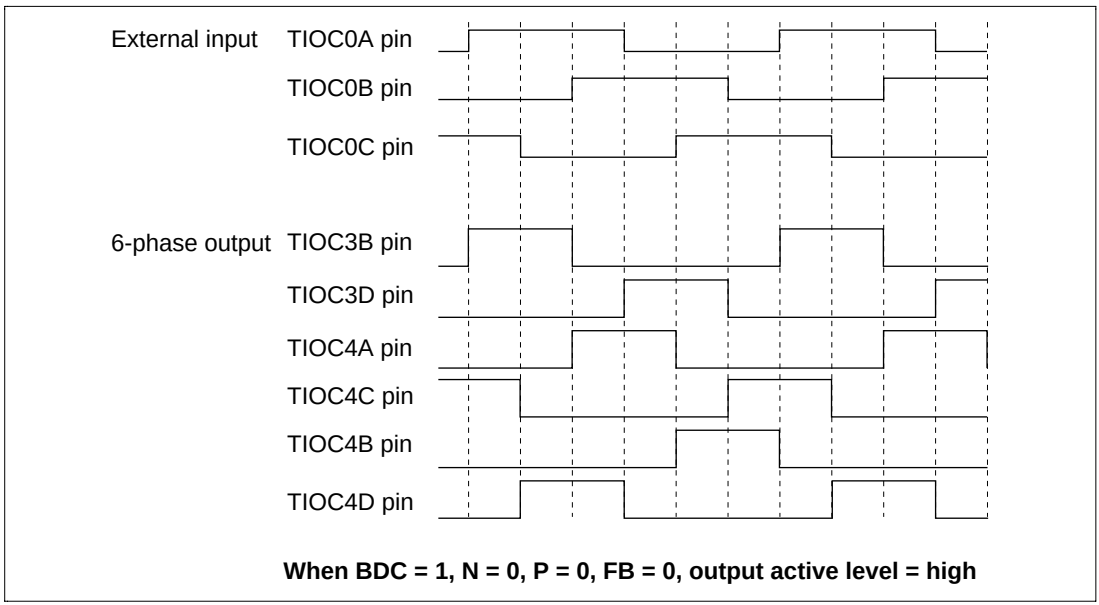


Figure 12.55 Example of Output Phase Switching by External Input (1)

13.1.4 Register Configuration

Table 13.2 summarizes the three WDT registers. They are used to select the clock, switch the WDT mode, and control the reset signal.

Table 13.2 WDT Registers

				Address	
Name	**Abbreviation**	**R/W**	**Initial Value**	**Write*1**	**Read*2**
Timer control/status register	TCSR	R/(W)*3	H'18	H'FFFF8610	H'FFFF8610
Timer counter	TCNT	R/W	H'00		H'FFFF8611
Reset control/status register	RSTCSR	R/(W)*3	H'1F	H'FFFF8612	H'FFFF8613

Notes: *1 Write by word transfer. It cannot be written in byte or longword.
*2 Read by byte transfer. It cannot be read in word or longword.
*3 Only 0 can be written in bit 7 to clear the flag.

13.2 Register Descriptions

13.2.1 Timer Counter (TCNT)

The TCNT is an 8-bit read/write upcounter. (The TCNT differs from other registers in that it is more difficult to write to. See section 13.2.4, Register Access, for details.) When the timer enable bit (TME) in the timer control/status register (TCSR) is set to 1, the watchdog timer counter starts counting pulses of an internal clock selected by clock select bits 2–0 (CKS2–CKS0) in the TCSR. When the value of the TCNT overflows (changes from H'FF to H'00), a watchdog timer overflow signal ($\overline{\text{WDTOVF}}$) or interval timer interrupt (ITI) is generated, depending on the mode selected in the WT/$\overline{\text{IT}}$ bit of the TCSR.

The TCNT is initialized to H'00 by a power-on reset and when the TME bit is cleared to 0. It is not initialized in the standby mode. The TCNT is not initialized by a manual reset from an external source ($\overline{\text{MRES}}$), but is initialized by a manual reset from the WDT.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Section 14 Serial Communication Interface (SCI)

14.1 Overview

The SH7040 Series has a serial communication interface (SCI) with two independent channels, both of which possess the same functions.

The SCI supports both asynchronous and clock synchronous serial communication. It also has a multiprocessor communication function for serial communication among two or more processors.

14.1.1 Features

- Select asynchronous or clock synchronous as the serial communications mode.
  - — Asynchronous mode: Serial data communications are synched by start-stop in character units. The SCI can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other chip that employs a standard asynchronous serial communication. It can also communicate with two or more other processors using the multiprocessor communication function. There are twelve selectable serial data communication formats.
    - Data length: seven or eight bits
    - Stop bit length: one or two bits
    - Parity: even, odd, or none
    - Multiprocessor bit: one or none
    - Receive error detection: parity, overrun, and framing errors
    - Break detection: by reading the RxD level directly when a framing error occurs
  - — Clocked synchronous mode: Serial data communication is synchronized with a clock signal. The SCI can communicate with other chips having a clock synchronous communication function. There is one serial data communication format.
    - Data length: eight bits
    - Receive error detection: overrun errors
- Full duplex communication: The transmitting and receiving sections are independent, so the SCI can transmit and receive simultaneously. Both sections use double buffering, so continuous data transfer is possible in both the transmit and receive directions.
- On-chip baud rate generator with selectable bit rates.
- Internal or external transmit/receive clock source: baud rate generator (internal) or SCK pin (external).
- Four types of interrupts: Transmit-data-empty, transmit-end, receive-data-full, and receive-error interrupts are requested independently. The transmit-data-empty and receive-data-full interrupts can start the direct memory access controller (DMAC)/data transfer controller (DTC) to transfer data.

Table 14.4 Bit Rates and BRR Settings in Clocked Synchronous Mode

Bit Rate (Bits/s)	φ (MHz)							
	4		8		10		12	
	n	N	n	N	n	N	n	N
110	3	141						
250	2	249	3	124	3	155	3	187
500	2	124	2	249	3	77	3	93
1k	1	249	2	124	2	155	2	187
2.5k	1	99	1	199	1	249	2	74
5k	0	199	1	99	1	124	1	149
10k	0	99	0	199	0	249	1	74
25k	0	39	0	79	0	99	0	119
50k	0	19	0	39	0	49	0	59
100k	0	9	0	19	0	24	0	29
250k	0	3	0	7	0	9	0	11
500k	0	1	0	3	0	4	0	5
1M	0	0*	0	1	—	—	0	2
2.5M					0	0*	0	0*
5M								

16.4.3 Input Sampling and A/D Conversion Time

The mid-speed A/D converter is equipped with a sample and hold circuit. The mid-speed A/D converter samples input after t_D hours has elapsed since setting the ADST bit of the A/D control/status register (ADCSR) to 1, then begins conversion. The A/D conversion timing is shown in table 16.4.

The A/D conversion time, as shown in figure 16.5, includes both t_D and input sampling time. Here, t_D is determined by the write timing to ADCSR and is not constant. Thus the conversion time changes in the range shown in table 16.4.

The conversion time shown in table 16.4 is the time for the first conversion. For the second conversion and after, the time will be 256 state (fixed) for CKS=0 and 128 state (fixed) for CKS=1.

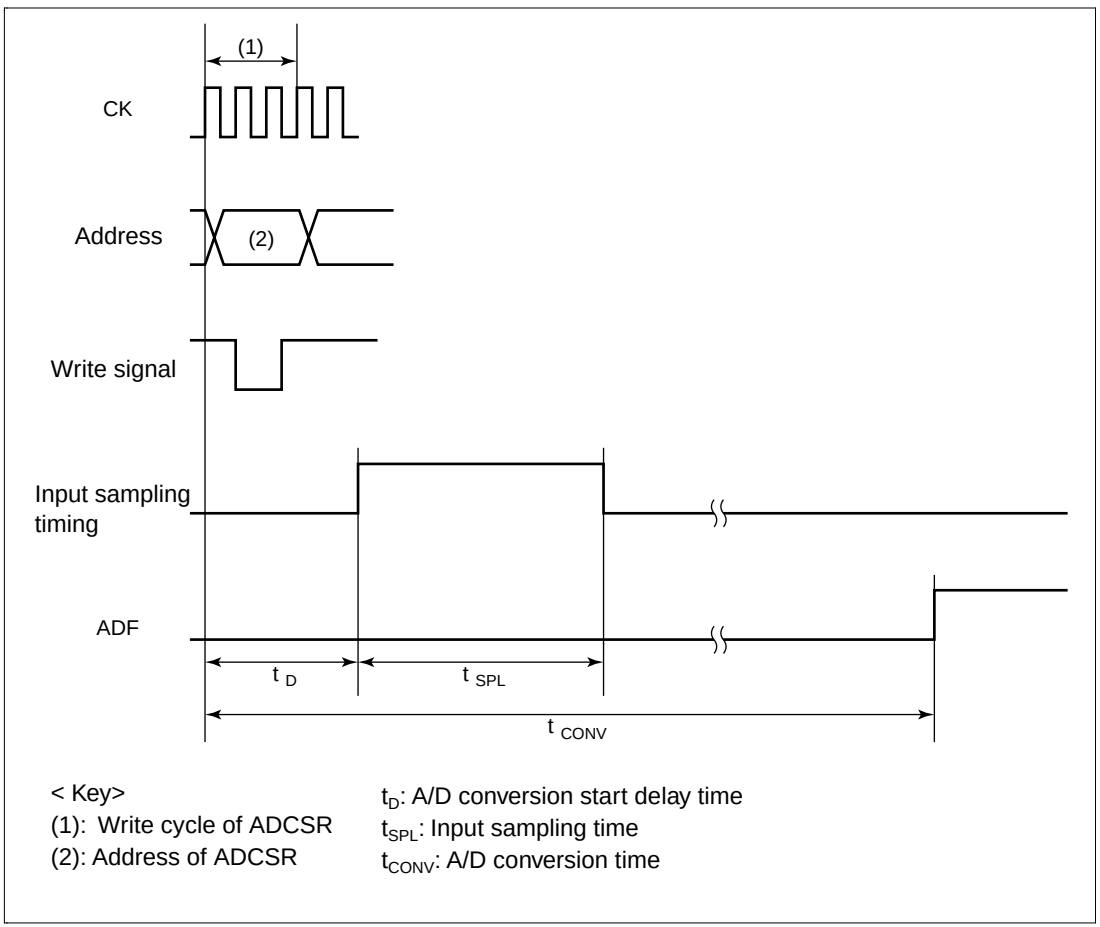


Figure 16.5 A/D Conversion Timing

16.6 A/D Conversion Precision Definitions

The medium-speed A/D converter converts analog values input from analog input channels to 10-bit digital values by comparing them with an analog reference voltage. In this operation, the absolute precision of the A/D conversion (i.e. the deviation between the input analog value and the output digital value) includes the following kinds of error.

(1) Offset error
(2) Full-scale error
(3) Quantization error
(4) Nonlinearity error

The above four kinds of error are described below with reference to figure 16.7. For the sake of clarity, this figure shows 3-bit medium-speed A/D conversion rather than 10-bit medium-speed A/D conversion. Offset error (see figure 16.7 (1)) is the deviation between the actual A/D conversion characteristic and the ideal A/D conversion characteristic when the digital output value changes from the minimum value (zero voltage) of 0000000000 (000 in the figure) to 0000000001 (001 in the figure). Full-scale error (see figure 16.7 (2)) is the deviation between the actual A/D conversion characteristic and the ideal A/D conversion characteristic when the digital output value changes from 1111111110 (110 in the figure) to the maximum value (full-scale voltage) of 111111111 (111 in the figure). Quantization error is the deviation inherent in the medium-speed A/D converter, given by 1/2 LSB (see figure 16.7 (3)). Nonlinearity error is the deviation between the actual A/D conversion characteristic and the ideal A/D conversion characteristic from zero voltage to full-scale voltage (see figure 16.7 (4)). This does not include offset error, full-scale error, and quantization error.

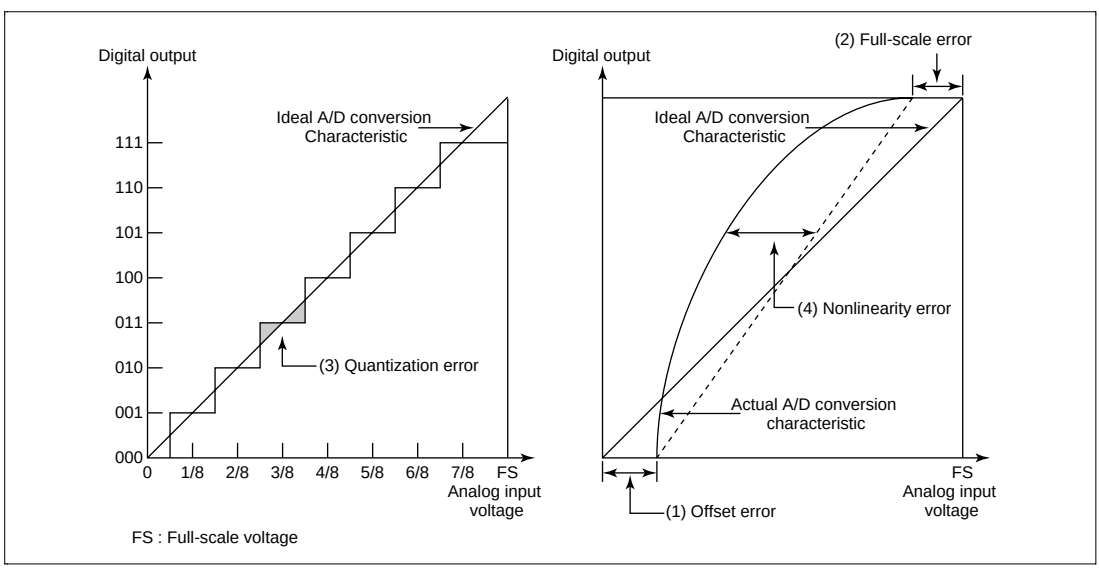


Figure 16.7 A/D Conversion Precision Definitions

18.3.12 Port D Control Register L (PDCRL)

PDCRL is a 16-bit read/write register that selects the multiplexed pin functions for the least significant sixteen port D pins. There are instances when these register settings will be ignored, depending on the operation mode.

On-Chip ROM-Disabled Extended Mode:

- 144-pin version:
  - Mode 0 (16-bit bus): Port D pins are data I/O pins; PDCRL settings are disabled.
  - Mode 1 (32-bit bus): Port D pins are data I/O pins; PDCRL settings are disabled.
- 112-pin and 120-pin versions:
  - Mode 0 (8-bit bus): Port D pins are data I/O pins; PDCRL settings are disabled.
  - Mode 1 (16-bit bus): Port D pins are data I/O pins; PDCRL settings are disabled.

On-Chip ROM-Enabled Extended Mode: The port D pins are shared as data I/O pins and general I/O pins; PDCRL settings are enabled.

Single Chip Mode: The port D pins are general I/O pins; PDCRL settings are disabled.

PDCRL is initialized to H'0000 by external power-on reset but is not initialized for manual resets, reset by WDT, standby mode, or sleep mode, so the previous data is maintained.

Port D Control Register L (PDCRL)

Bit:	15	14	13	12	11	10	9	8
	PD15 MD	PD14 MD	PD13 MD	PD12 MD	PD11 MD	PD10 MD	PD9 MD	PD8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PD7 MD	PD6 MD	PD5 MD	PD4 MD	PD3 MD	PD2 MD	PD1 MD	PD0 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.3 Register States in the Standby Mode (cont)

Module	Registers Initialized	Registers that Retain Data	Registers with Undefined Contents
Pin function controller (PFC)	—	All registers	—
I/O port (I/O)	—	All registers	—
Power-down state related	—	Standby control register (SBYCR)	—

24.4.2 Canceling the Standby Mode

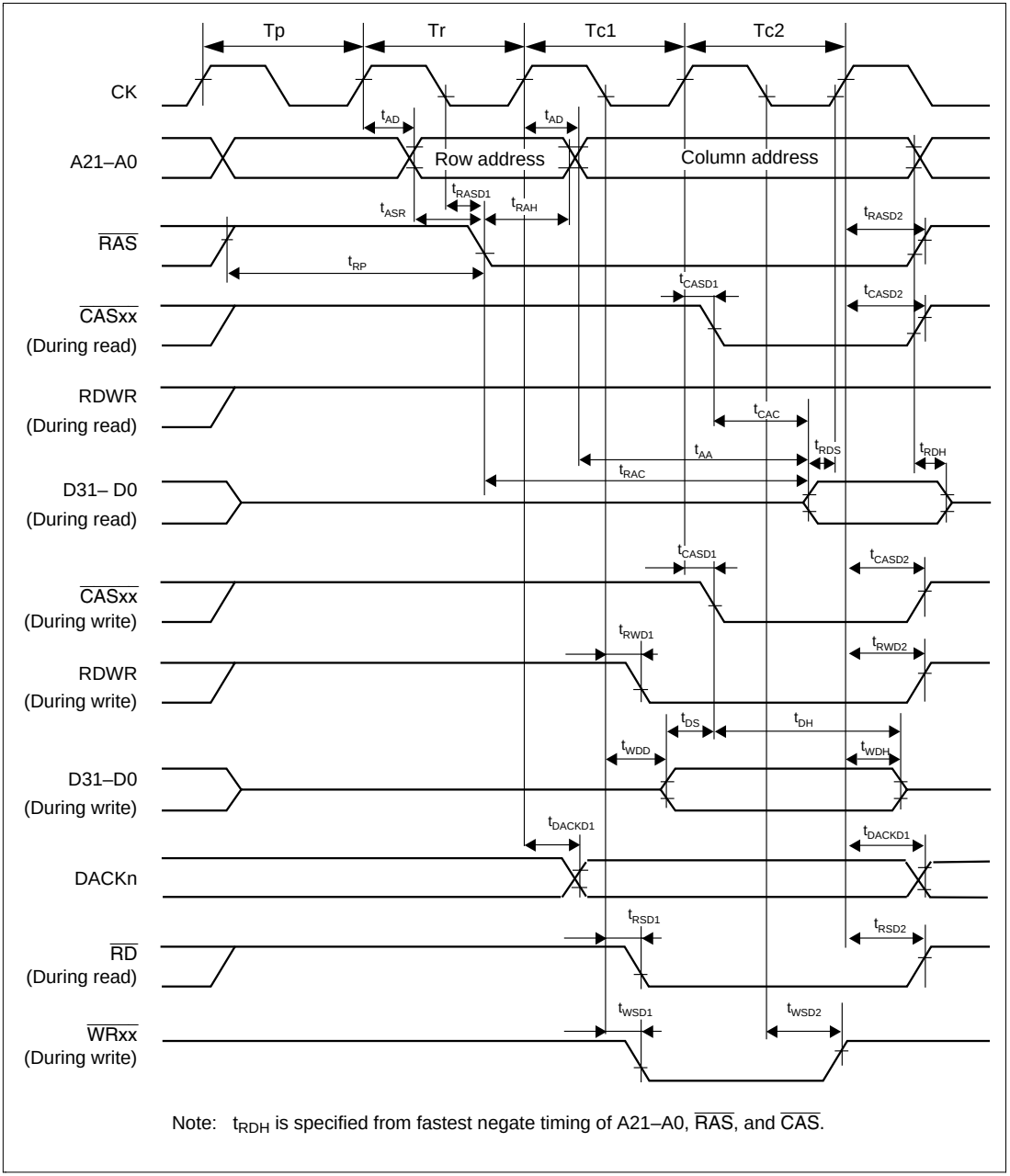
The standby mode is canceled by an NMI interrupt, a power-on reset, or a manual reset.

Cancellation by an NMI: Clock oscillation starts when a rising edge or falling edge (selected by the NMI edge select bit (NMIE) of the interrupt control register (ICR) of the INTC) is detected in the NMI signal. This clock is supplied only to the watchdog timer (WDT). A WDT overflow occurs if the time established by the clock select bits (CKS2–CKS0) in the TCSR of the WDT elapses before transition to the standby mode. The occurrence of this overflow is used to indicate that the clock has stabilized, so the clock is supplied to the entire chip, the standby mode is canceled, and NMI exception processing begins.

When canceling standby mode with NMI interrupts, set the CKS2–CKS0 bits so that the WDT overflow period is longer than the oscillation stabilization time.

When canceling standby mode with an NMI pin set for falling edge, be sure that the NMI pin level upon entering standby (when the clock is halted) is high level, and that the NMI pin level upon returning from standby (when the clock starts after oscillation stabilization) is low level. When canceling standby mode with an NMI pin set for rising edge, be sure that the NMI pin level upon entering standby (when the clock is halted) is low level, and that the NMI pin level upon returning from standby (when the clock starts after oscillation stabilization) is high level.

Cancellation by a Power-On Reset: A power-on reset caused by setting the $\overline{\text{RES}}$ pin to low level cancels the standby mode.



Note: t_{RDH} is specified from fastest negate timing of A21–A0, $\overline{RAS}$, and $\overline{CAS}$.

Figure 26.11 DRAM Cycle (Normal Mode, No Wait, TPC = 0, RCD = 0)

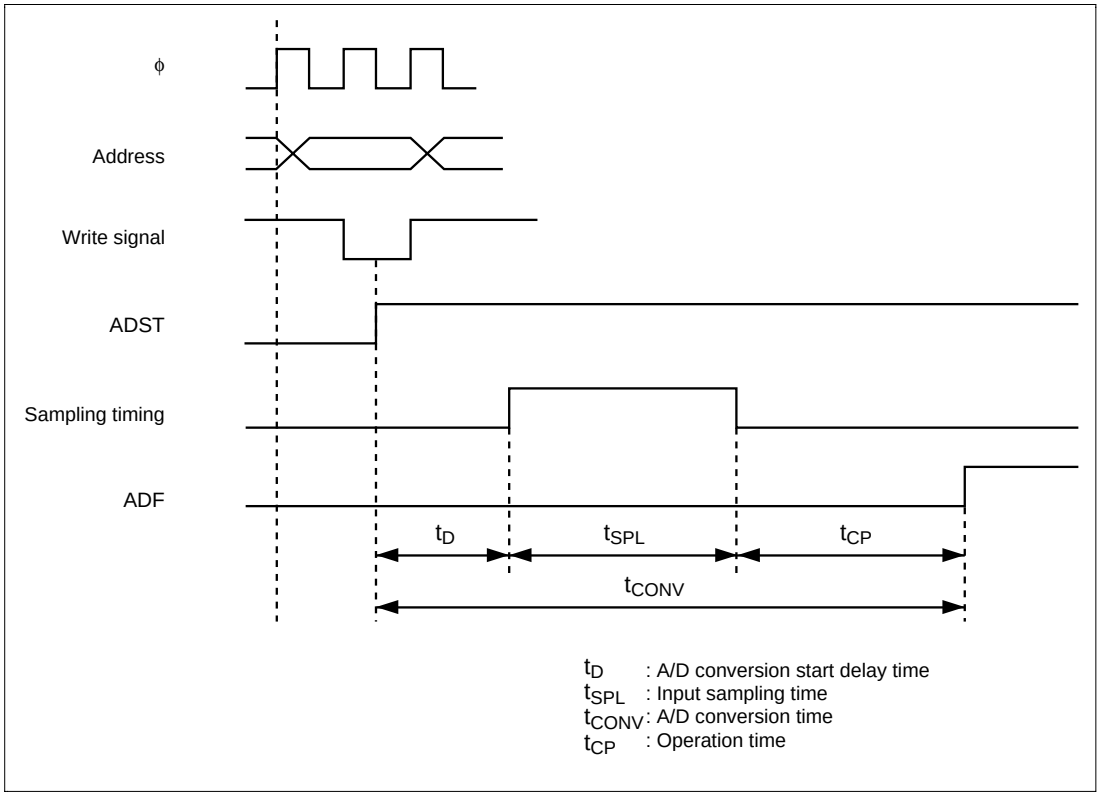


Figure 26.30 Analog Conversion Timing

Table A.1 On-Chip I/O Register Addresses (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF821A	TGR3B									MTU
H'FFFF821B										
H'FFFF821C	TGR4A									
H'FFFF821D										
H'FFFF821E	TGR4B									
H'FFFF821F										
H'FFFF8220	TCNTS									
H'FFFF8221										
H'FFFF8222	TCBR									
H'FFFF8223										
H'FFFF8224	TGR3C									
H'FFFF8225										
H'FFFF8226	TGR3D									
H'FFFF8227										
H'FFFF8228	TGR4C									
H'FFFF8229										
H'FFFF822A	TGR4D									
H'FFFF822B										
H'FFFF822C	TSR3	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
H'FFFF822D	TSR4	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
H'FFFF822E	—	—	—	—	—	—	—	—	—	
H'FFFF822F	—	—	—	—	—	—	—	—	—	
H'FFFF8230 to H'FFFF823F	—	—	—	—	—	—	—	—	—	
H'FFFF8240	TSTR	CST4	CST3	—	—	—	CST2	CST1	CST0	
H'FFFF8241	TSYR	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0	
H'FFFF8242 to H'FFFF825F	—	—	—	—	—	—	—	—	—	
H'FFFF8260	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	
H'FFFF8261	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0	
H'FFFF8262	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
H'FFFF8263	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
H'FFFF8264	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
H'FFFF8265	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
H'FFFF8266	TCNT0									
H'FFFF8267										

Table A.1 On-Chip I/O Register Addresses (cont)

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF8406	ADDRD0	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D(Mid-
H'FFFF8407		AD1	AD0	—	—	—	—	—	—	speed)
H'FFFF8408	ADDRA1	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	(A mask
H'FFFF8409		AD1	AD0	—	—	—	—	—	—	only)
H'FFFF840A	ADDRB1	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'FFFF840B		AD1	AD0	—	—	—	—	—	—	
H'FFFF840C	ADDRC1	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'FFFF840D		AD1	AD0	—	—	—	—	—	—	
H'FFFF840E	ADDRD1	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'FFFF840F		AD1	AD0	—	—	—	—	—	—	
H'FFFF8410	ADCSR0	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
H'FFFF8411	ADCSR1	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
H'FFFF8412	AADCR0	TRGE	—	—	—	—	—	—	—	
H'FFFF8413	AADCR1	TRGE	—	—	—	—	—	—	—	
H'FFFF8414 to H'FFFF857F	—	—	—	—	—	—	—	—	—	
H'FFFF8580	FLMCR1	FWE	SWE	ESU1	PSU1	EV1	PV1	E1	P1	FLASH
H'FFFF8581	FLMCR2	FLER	—	ESU2	PSU2	EV2	PV2	E2	P2	(F-ZTAT
H'FFFF8582	EBR1	—	—	—	—	EB3	EB2	EB1	EB0	version-
H'FFFF8583	EBR2	EB11	EB10	EB9	EB8	EB7	EB6	EB5	EB4	only)
H'FFFF8584 to H'FFFF859F	—	—	—	—	—	—	—	—	—	
H'FFFF8600	UBARH	UBA31	UBA30	UBA29	UBA28	UBA27	UBA26	UBA25	UBA24	UBC
H'FFFF8601		UBA23	UBA22	UBA21	UBA20	UBA19	UBA18	UBA17	UBA16	
H'FFFF8602	UBARL	UBA15	UBA14	UBA13	UBA12	UBA11	UBA10	UBA9	UBA8	
H'FFFF8603		UBA7	UBA6	UBA5	UBA4	UBA3	UBA2	UBA1	UBA0	
H'FFFF8604	UBAMRH	UBM31	UBM30	UBM29	UBM28	UBM27	UBM26	UBM25	UBM24	
H'FFFF8605		UBM23	UBM22	UBM21	UBM20	UBM19	UBM18	UBM17	UBM16	
H'FFFF8606	UBAMRL	UBM15	UBM14	UBM13	UBM12	UBM11	UBM10	UBM9	UBM8	
H'FFFF8607		UBM7	UBM6	UBM5	UBM4	UBM3	UBM2	UBM1	UBM0	
H'FFFF8608	UBBR	—	—	—	—	—	—	—	—	
H'FFFF8609		CP1	CP0	ID1	ID0	RW1	RW0	SZ1	SZ0	
H'FFFF860A to H'FFFF860F	—	—	—	—	—	—	—	—	—	
H'FFFF8610	TCSR	OVF	WT/IT	TME	—	—	CKS2	CKS1	CKS0	WDT

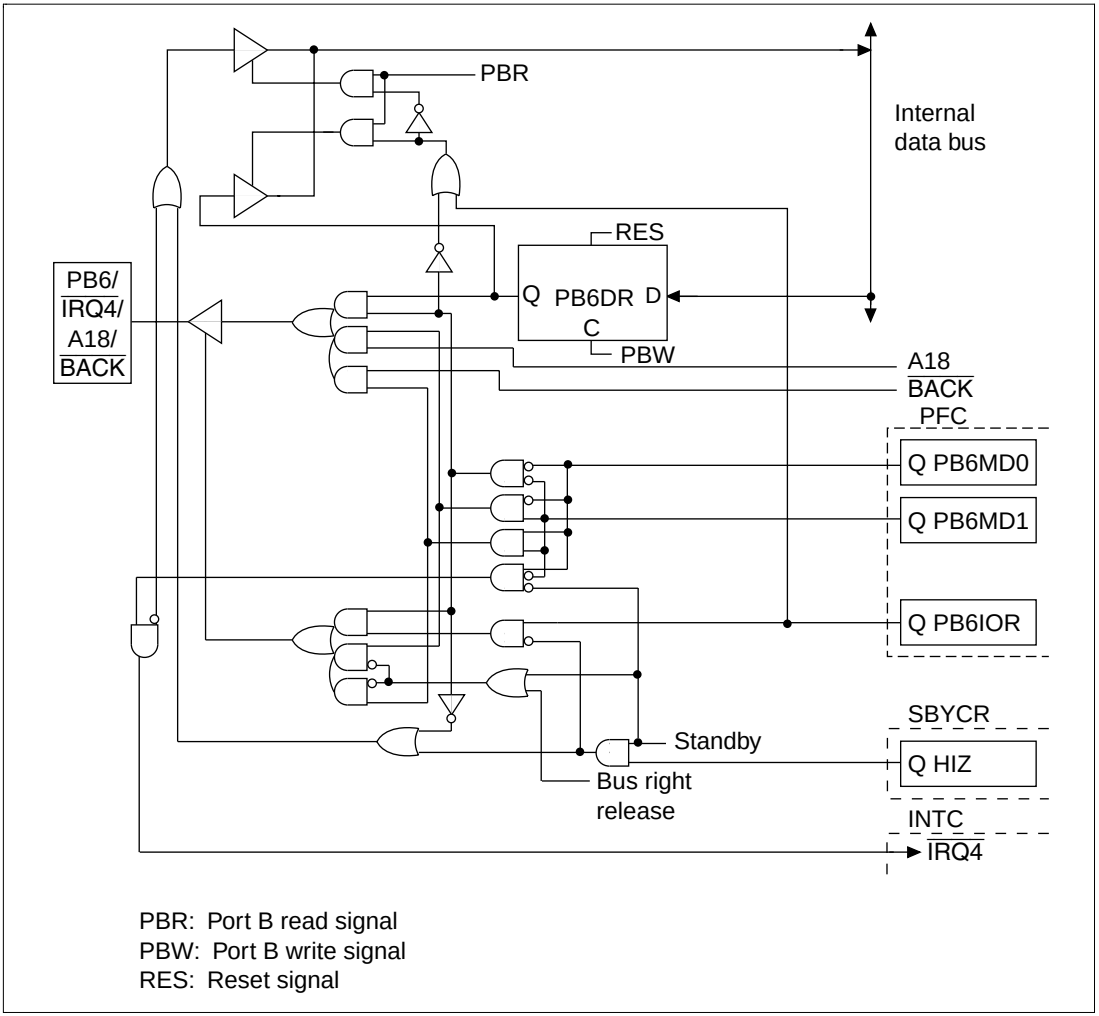


Figure B.17 PB6/$\overline{\text{IRQ4}}$/A18/$\overline{\text{BACK}}$ Block Diagram