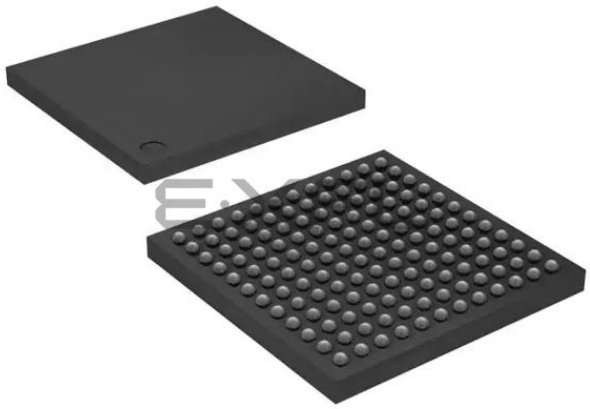

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 53x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk61fx512vmd12

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4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage[1]	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL0/XTAL0, and EXTAL1/XTAL1) [2]	–0.3	5.5	V
V_{AIO}	Analog[3], $\overline{\text{RESET}}$, EXTAL0/XTAL0, and EXTAL1/XTAL1 input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{USB1_DM}	USB1_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. It applies for all port pins except Tamper pins.

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H} V_{LVW2H} V_{LVW3H} V_{LVW4H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV=00) • Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	1
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L} V_{LVW2L} V_{LVW3L} V_{LVW4L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00) • Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	1.74 1.84 1.94 2.04	1.80 1.90 2.00 2.10	1.86 1.96 2.06 2.16	V V V V	1
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength	V_{DD} – 0.5	—	—	V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—		V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	— — 	 V V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
I_{OHT_io60}	Output high current total for fast digital ports	—	—	100	mA	
V_{OH_Tamper}	Output high voltage — high drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —	— —	V V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —	— —	V V	
I_{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	 — —	— — 	 0.5 0.5	 V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1 mA	 — —	— — 	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
V_{OL_Tamper}	Output low voltage — high drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA	— —	— —	0.5 0.5	V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA	— —	— —	0.5 0.5	V V	
I_{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	

I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs
	• V_{SS} ≤ V_{IN} ≤ V_{DD}
	  • All pins except EXTAL32, XTAL32, EXTAL, XTAL
	  • EXTAL (PTA18) and XTAL (PTA19)
	  • EXTAL32, XTAL32
		
		—
		—
		—
			
			0.002
			0.004
			0.075
				
				0.5
				1.5
				10
					
					µA
					µA
					µA
						1, 2

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{IND}	Input leakage current, digital pins					2, 3
	• $V_{SS} \le V_{IN} \le V_{IL}$					
	• All digital pins	—	0.002	0.5	µA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	µA	
	• PTD7	—	0.004	1	µA	
I_{IND}	Input leakage current, digital pins					2, 3, 4
	• $V_{IL} < V_{IN} < V_{DD}$					
	• V_{DD} = 3.6 V	—	18	26	µA	
	• V_{DD} = 3.0 V	—	12	19	µA	
	• V_{DD} = 2.5 V	—	8	13	µA	
	• V_{DD} = 1.7 V	—	3	6	µA	
I_{IND}	Input leakage current, digital pins					2, 3
	• $V_{DD} < V_{IN} < 5.5$ V	—	1	50	µA	
Z_{IND}	Input impedance examples, digital pins					2, 5
	• V_{DD} = 3.6 V	—	—	48	kΩ	
	• V_{DD} = 3.0 V	—	—	55	kΩ	
	• V_{DD} = 2.5 V	—	—	57	kΩ	
	• V_{DD} = 1.7 V	—	—	85	kΩ	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	µA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	—	50	kΩ	6
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	—	50	kΩ	7

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
3. Internal pull-up/pull-down resistors disabled.
4. Characterized, not tested in production.
5. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V. See Figure 2.
6. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
7. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{SYS_USBFS}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{SYS_USBHS}	System and core clock when High Speed USB in operation	60	—	MHz	
f_{ENET}	System and core clock when ethernet in operation • 10 Mbps • 100 Mbps	 5 50	 — —	MHz	
f_{BUS}	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	

Table continues on the next page...

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature[1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

5.4.2 Thermal attributes

Board type	Symbol	Description	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	30	°C/W	1, 2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	41	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	27	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

NOTES:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$$T_{NFC} = T_L + T_H = \frac{T_{input\ clock}}{SCALER}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

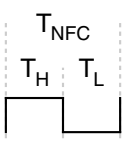
$$SCALER = \frac{SIM\_CLKDIV4[NFCFRAC] + 1}{SIM\_CLKDIV4[NFCDIV] + 1}$$

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means $T_H = T_L$. In case the reciprocal of SCALER is not an integer:

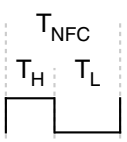
$$T_L = (1 + SCALER / 2) \times \frac{T_{NFC}}{2}$$

$$T_H = (1 - SCALER / 2) \times \frac{T_{NFC}}{2}$$

For example, if SCALER is 0.2, then $T_H = T_L = T_{NFC}/2$.



However, if SCALER is 0.667, then $T_L = 2/3 \times T_{NFC}$ and $T_H = 1/3 \times T_{NFC}$.



NOTE

The reciprocal of SCALER must be a multiple of 0.5. For example, 1, 1.5, 2, 2.5, etc.

Table 25. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns

Table continues on the next page...

Table 25. NFC specifications (continued)

Num	Description	Min.	Max.	Unit
t_{WP}	$\overline{\text{NFC\_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC\_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC\_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

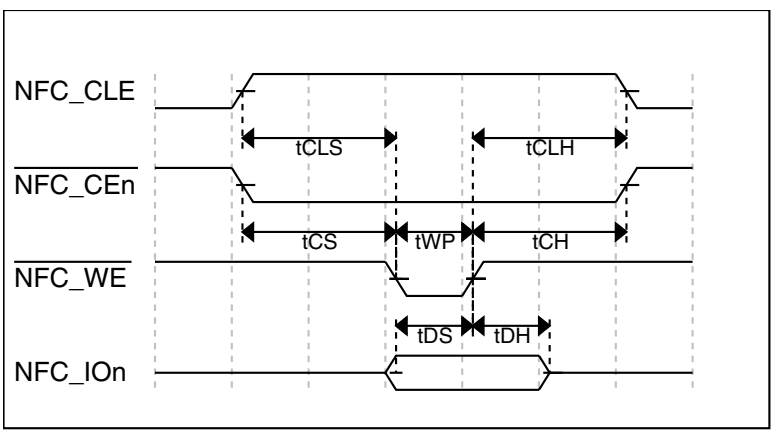


Figure 13. Command latch cycle timing

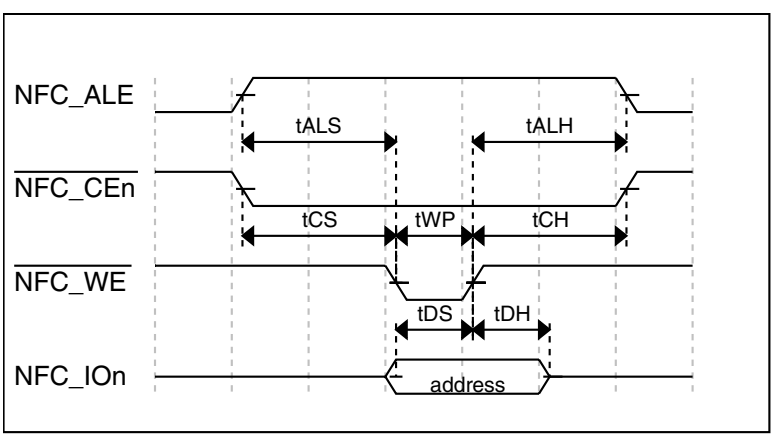


Figure 14. Address latch cycle timing

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 26. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE/BWE}n}$, $\overline{\text{FB\_CS}n}$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 27. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE/BWE}n}$, $\overline{\text{FB\_CS}n}$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 29. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode	 82 78	 95 90	 — —	dB dB	7

Table continues on the next page...

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• Avg = 32					
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

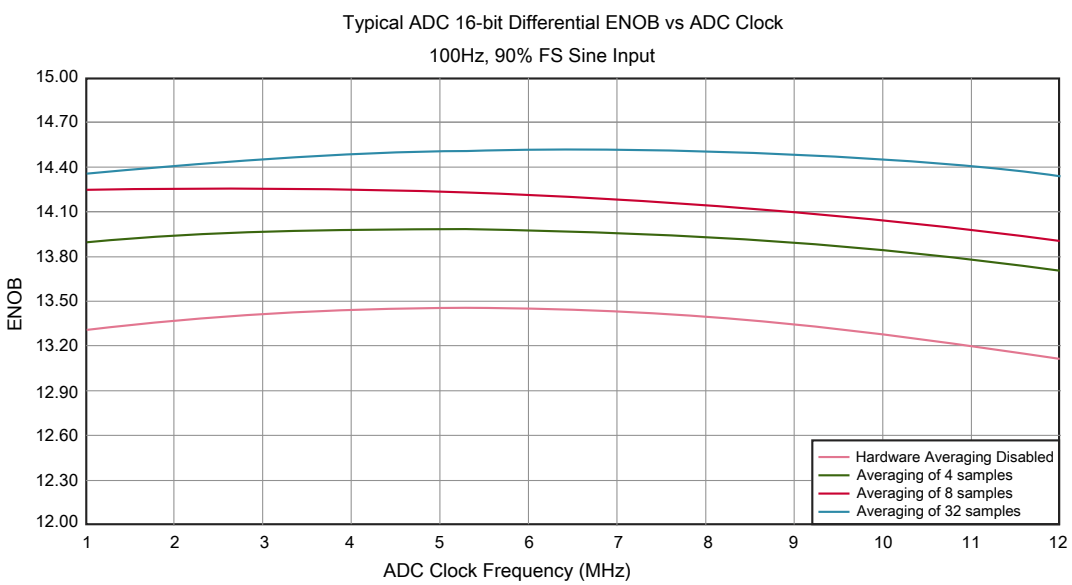


Figure 21. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Table 36. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = + 1.0 mA • current = - 1.0 mA	 — —	 2 5	 — —	mV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 37. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 38. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces

6.8.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.8.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 39. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

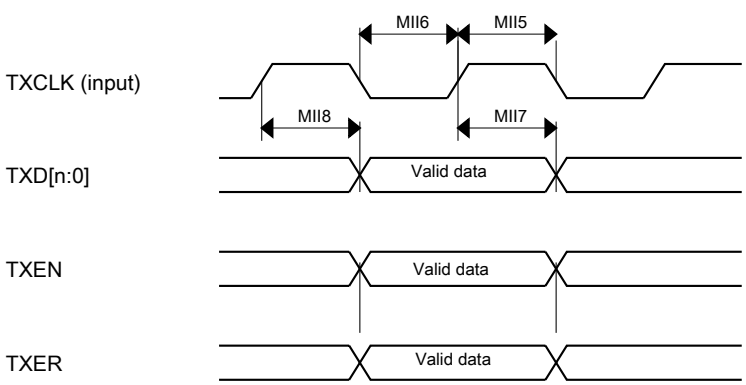


Figure 27. RMII/MII transmit signal timing diagram

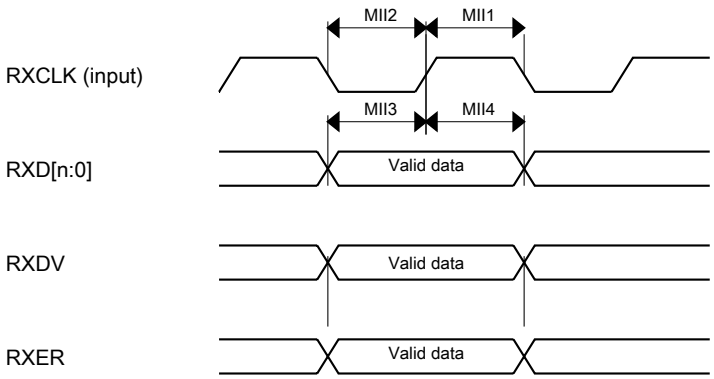


Figure 28. RMII/MII receive signal timing diagram

6.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 40. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.8.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

NOTE

The MCGPLLCLK meets the USB jitter specifications for certification with the use of an external clock/crystal for both Device and Host modes.

Table 45. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

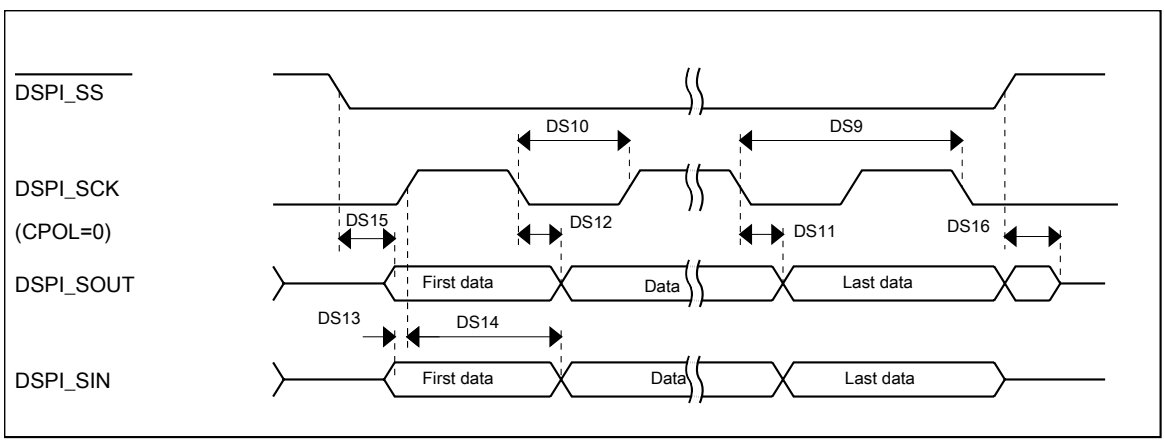


Figure 31. DSPI classic SPI timing — slave mode

6.8.8 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 46. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	

Table continues on the next page...

is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.12.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 51. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
F7	VSS	VSS	VSS								
H3	VSS	VSS	VSS								
H1	USB0_DP	USB0_DP	USB0_DP								
H2	USB0_DM	USB0_DM	USB0_DM								
G1	VOUT33	VOUT33	VOUT33								
G2	VREGIN	VREGIN	VREGIN								
J1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1								
J2	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1								
K1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1								
K2	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1								
L1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
L2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
M1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
M2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
H5	VDDA	VDDA	VDDA								
G5	VREFH	VREFH	VREFH								
G6	VREFL	VREFL	VREFL								
H6	VSSA	VSSA	VSSA								
K3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
J3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								

144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
L3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
L4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23								
L5	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B								
K5	TAMPER1	TAMPER1	TAMPER1								
K4	TAMPER2	TAMPER2	TAMPER2								
J4	TAMPER3	TAMPER3	TAMPER3								
H4	TAMPER4	TAMPER4	TAMPER4								
M4	TAMPER5	TAMPER5	TAMPER5								
M7	XTAL32	XTAL32	XTAL32								
M6	EXTAL32	EXTAL32	EXTAL32								
L6	VBAT	VBAT	VBAT								
J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
K6	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
K7	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
M8	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_RXER/ MII0_RXER	CMP2_OUT	I2S0_TX_ BCLK	JTAG_TRST_ b	
E7	VDD	VDD	VDD								
G7	VSS	VSS	VSS								
J7	PTA6	ADC3_SE6a	ADC3_SE6a	PTA6	ULPI_CLK	FTM0_CH3	I2S1_RXD0			TRACE_ CLKOUT	
J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7	ULPI_DIR	FTM0_CH4	I2S1_RX_ BCLK			TRACE_D3	
K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8	ULPI_NXT	FTM1_CH0	I2S1_RX_FS		FTM1_QD_ PHA	TRACE_D2	
L8	PTA9	ADC3_SE5a	ADC3_SE5a	PTA9	ULPI_STP	FTM1_CH1	MII0_RXD3		FTM1_QD_ PHB	TRACE_D1	
M9	PTA10	ADC3_SE4a	ADC3_SE4a	PTA10	ULPI_DATA0	FTM2_CH0	MII0_RXD2		FTM2_QD_ PHA	TRACE_D0	
L9	PTA11	ADC3_SE15	ADC3_SE15	PTA11	ULPI_DATA1	FTM2_CH1	MII0_RXCLK		FTM2_QD_ PHB		