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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	729-BBGA
Supplier Device Package	729-PBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1bg729">https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1bg729</a>

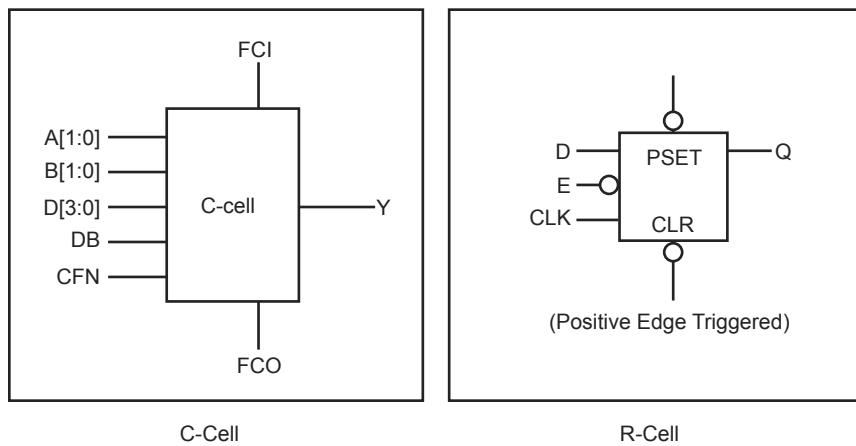
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**Figure 1-2 • Axcelerator Family Interconnect Elements**

## Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

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**Figure 1-3 • AX C-Cell and R-Cell**

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

**Table 2-22 • 3.3 V LVTTL I/O Module**
**Worst-Case Commercial Conditions  $VCCA = 1.425\text{ V}$ ,  $VCCI = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$  (continued)**

Parameter	Description	-2 Speed		-1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>LVTTL Output Drive Strength =3 (16 mA) / High Slew Rate</b>								
$t_{DP}$	Input Buffer		1.68		1.92		2.26	ns
$t_{PY}$	Output Buffer		3.12		3.56		4.18	ns
$t_{ENZL}$	Enable to Pad Delay through the Output Buffer—Z to Low		3.54		4.04		4.75	ns
$t_{ENZH}$	Enable to Pad Delay through the Output Buffer—Z to High		2.78		3.17		3.72	ns
$t_{ENLZ}$	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
$t_{ENHZ}$	Enable to Pad Delay through the Output Buffer—High to Z		2.58		2.59		2.60	ns
$t_{IOLKQ}$	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
$t_{IOLKY}$	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
$t_{SUD}$	Data Input Set-Up		0.23		0.27		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.26		0.30		0.35	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low		0.39		0.39		0.39	ns
$t_{CPWLH}$	Clock Pulse Width Low to High		0.39		0.39		0.39	ns
$t_{WASYN}$	Asynchronous Pulse Width		0.37		0.37		0.37	ns
$t_{REASYN}$	Asynchronous Recovery Time		0.13		0.15		0.17	ns
$t_{HASYN}$	Asynchronous Removal Time		0.00		0.00		0.00	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

**Micro**

*Axcelerator Family FPGAs*

# Axcelerator Clock Management System

## Introduction

Each member of the Axcelerator family<sup>6</sup> contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20µs

## Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a  $250\ \Omega$  resistor. Furthermore,  $0.1\ \mu\text{F}$  and  $10\ \mu\text{F}$  decoupling capacitors should be connected across the VCCPLL and VCOMPPPLL pins.

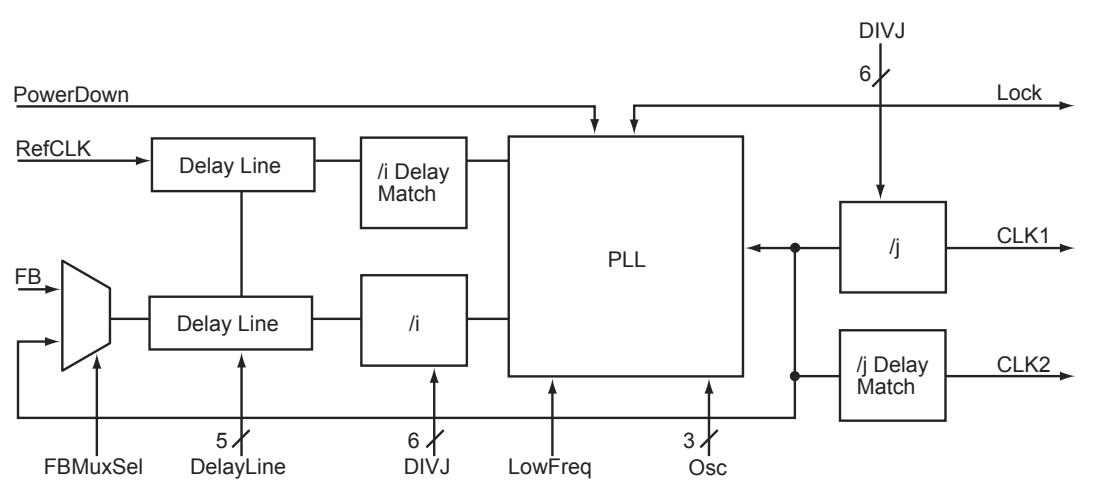


Figure 2-48 • PLL Block Diagram

Note: The VCOMPPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

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6. AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.

## RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-86). Each block has independent read and write ports which enable simultaneous read and write operations.

**Table 2-86 • Memory Block WxD Options**

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

## Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

## RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in Table 2-87.

**Table 2-87 • Allowable RW and WW Values**

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

**Table 2-89 • One RAM Block**

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, TJ = 70°C

Parameter	Description	-2 Speed		-1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>								
t <sub>WDASU</sub>	Write Data Setup vs. WCLK		1.08		1.23		1.45	ns
t <sub>WDAHD</sub>	Write Data Hold vs. WCLK		0.22		0.25		0.30	ns
t <sub>WADSU</sub>	Write Address Setup vs. WCLK		1.08		1.23		1.45	ns
t <sub>WADHD</sub>	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t <sub>WENSU</sub>	Write Enable Setup vs. WCLK		1.08		1.23		1.45	ns
t <sub>WENHD</sub>	Write Enable Hold vs. WCLK		0.22		0.25		0.30	ns
t <sub>WCKH</sub>	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t <sub>WCLK</sub>	WCLK Minimum Low Pulse Width	0.88		0.88		0.88		ns
t <sub>WCKP</sub>	WCLK Minimum Period	1.63		1.63		1.63		ns
<b>Read Mode</b>								
t <sub>RADSU</sub>	Read Address Setup vs. RCLK		0.81		0.92		1.08	ns
t <sub>RADHD</sub>	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t <sub>RENSU</sub>	Read Enable Setup vs. RCLK		0.81		0.92		1.08	ns
t <sub>RENHD</sub>	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t <sub>RCK2RD1</sub>	RCLK-to-OUT (Pipelined)		1.32		1.51		1.77	ns
t <sub>RCK2RD2</sub>	RCLK-to-OUT (Non-Pipelined)		2.16		2.46		2.90	ns
t <sub>RCLKH</sub>	RCLK Minimum High Pulse Width	0.77		0.77		0.77		ns
t <sub>RCLKL</sub>	RCLK Minimum Low Pulse Width	0.93		0.93		0.93		ns
t <sub>RCKP</sub>	RCLK Minimum Period	1.70		1.70		1.70		ns

Note: Timing data for this single block RAM has a depth of 4,096. For all other combinations, use Microsemi's timing software.

**Table 2-90 • Two RAM Blocks Cascaded**

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, TJ = 70°C

Parameter	Description	-2 Speed		-1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>								
t <sub>WDASU</sub>	Write Data Setup vs. WCLK		1.39		1.59		1.87	ns
t <sub>WDAHD</sub>	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t <sub>WADSU</sub>	Write Address Setup vs. WCLK		1.39		1.59		1.87	ns
t <sub>WADHD</sub>	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t <sub>WENSU</sub>	Write Enable Setup vs. WCLK		1.39		1.59		1.87	ns
t <sub>WENHD</sub>	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t <sub>WCKH</sub>	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t <sub>WCLK</sub>	WCLK Minimum Low Pulse Width	1.76		1.76		1.76		ns
t <sub>WCKP</sub>	WCLK Minimum Period	2.51		2.51		2.51		ns
<b>Read Mode</b>								
t <sub>RADSU</sub>	Read Address Setup vs. RCLK		1.71		1.94		2.28	ns
t <sub>RADHD</sub>	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t <sub>RENSU</sub>	Read Enable Setup vs. RCLK		1.71		1.94		2.28	ns
t <sub>RENHD</sub>	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t <sub>RCK2RD1</sub>	RCLK-To-OUT (Pipelined)		1.43		1.63		1.92	ns
t <sub>RCK2RD2</sub>	RCLK-To-OUT (Non-Pipelined)		2.26		2.58		3.03	ns
t <sub>RCLKH</sub>	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t <sub>RCLKL</sub>	RCLK Minimum Low Pulse Width	1.89		1.89		1.89		ns
t <sub>RCKP</sub>	RCLK Minimum Period	2.62		2.62		2.62		ns

Note: Timing data for these two cascaded RAM blocks uses a depth of 8,192. For all other combinations, use Microsemi's timing software.

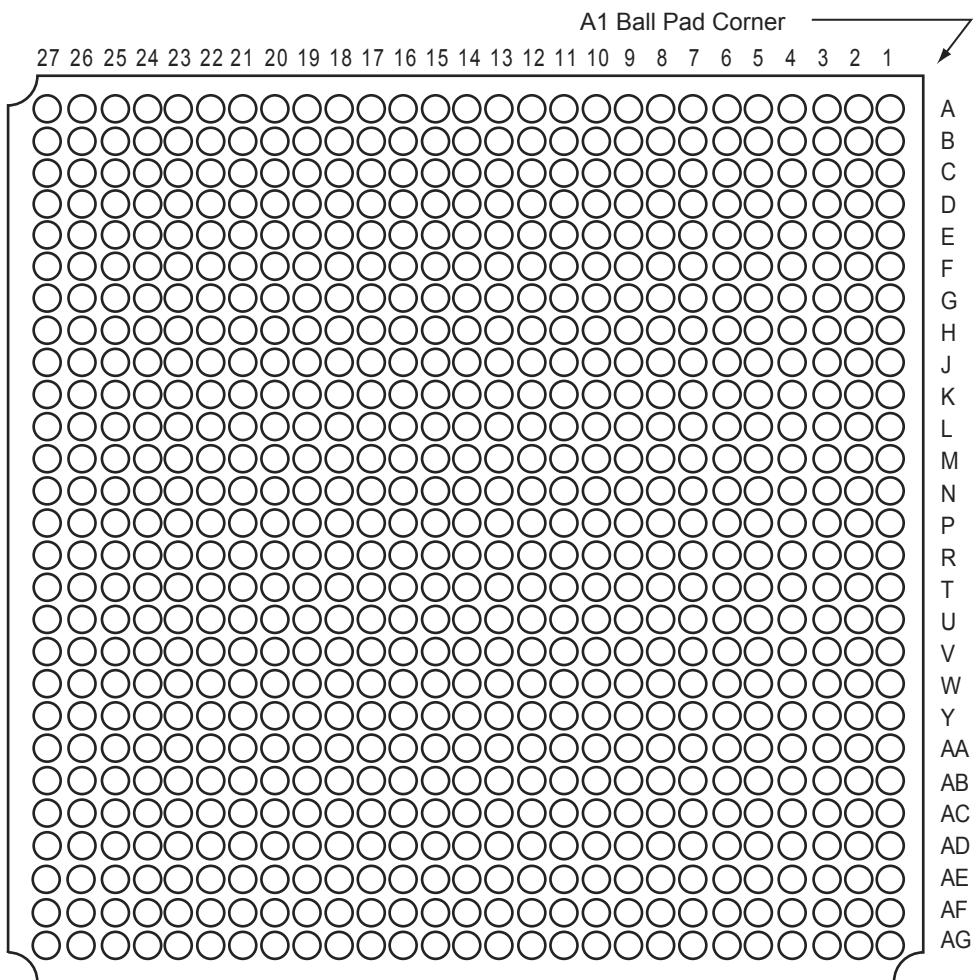
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## 3 – Package Pin Assignments

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**BG729**

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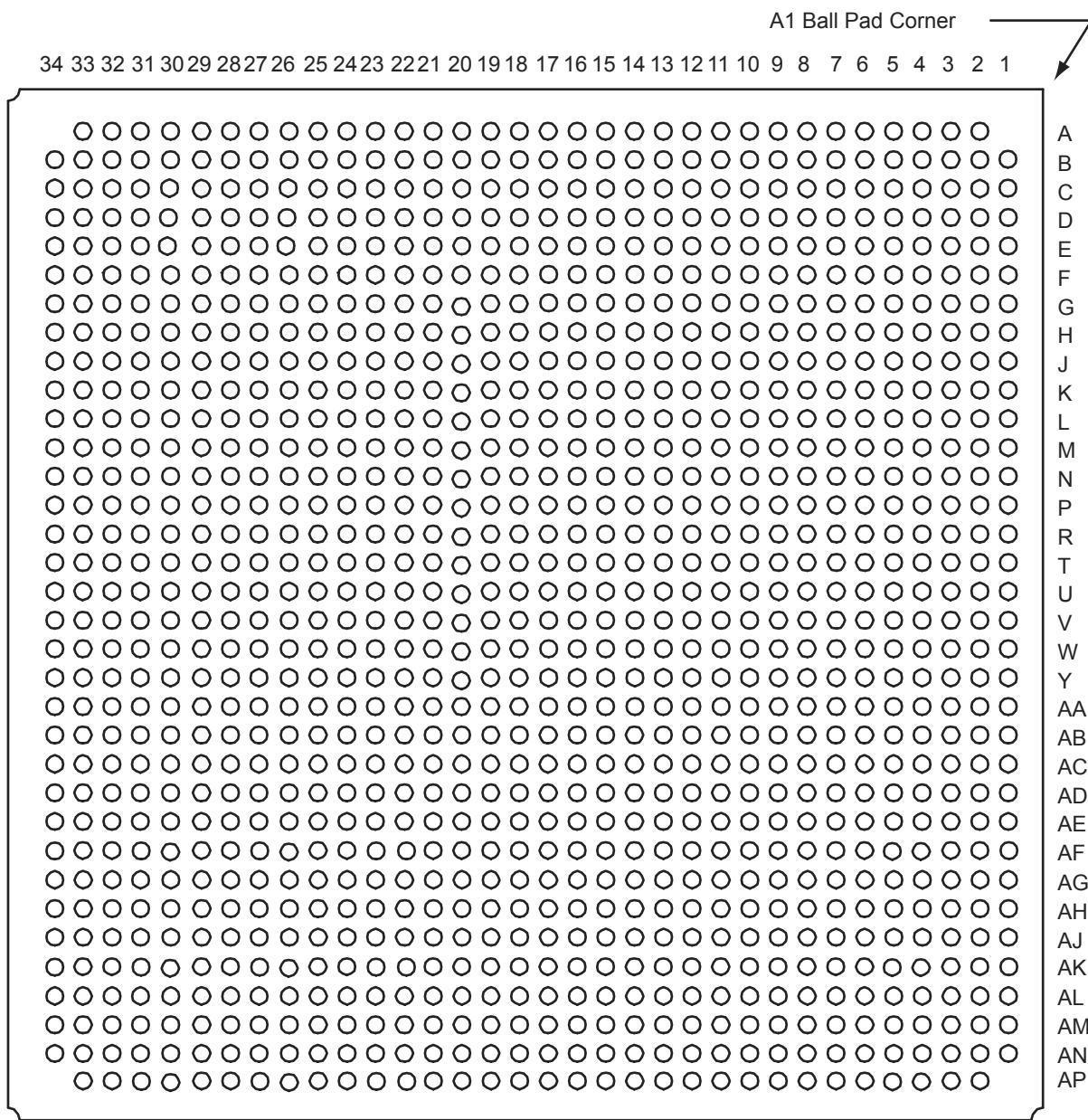
### Note

For Package Manufacturing and Environmental information, visit Resource center at  
<http://www.microsemi.com/soc/products/rescenter/package/index.html>.

<b>BG729</b>		<b>BG729</b>		<b>BG729</b>	
<b>AX1000 Function</b>	<b>Pin Number</b>	<b>AX1000 Function</b>	<b>Pin Number</b>	<b>AX1000 Function</b>	<b>Pin Number</b>
IO54PB1F5	E20	IO72PB2F6	J23	IO91NB2F8	N25
IO55NB1F5	E21	IO73NB2F6	H24	IO91PB2F8	N24
IO55PB1F5	D21	IO73PB2F6	H23	IO92NB2F8	N27
IO56NB1F5	H19	IO74NB2F7	L21	IO92PB2F8	N26
IO56PB1F5	G19	IO74PB2F7	K21	IO93NB2F8	P26
IO57NB1F5	D22	IO75NB2F7	G27	IO93PB2F8	P27
IO57PB1F5	C22	IO75PB2F7	F27	IO94NB2F8	N19
IO58NB1F5	B23	IO76NB2F7	K23	IO94PB2F8	N20
IO58PB1F5	A23	IO76PB2F7	K22	IO95NB2F8	P23
IO59NB1F5	D23	IO77NB2F7	H26	IO95PB2F8	P22
IO59PB1F5	C23	IO77PB2F7	H25	<b>Bank 3</b>	
IO60NB1F5	G21	IO78NB2F7	K25	IO96NB3F9	P25
IO60PB1F5	G20	IO78PB2F7	K24	IO96PB3F9	P24
IO61NB1F5	E23	IO79NB2F7	J26	IO97NB3F9	R26
IO61PB1F5	E22	IO79PB2F7	J25	IO97PB3F9	R27
IO62NB1F5	F22	IO80NB2F7	M20	IO98NB3F9	P21
IO62PB1F5	F21	IO80PB2F7	L20	IO98PB3F9	P20
IO63NB1F5	H20	IO81NB2F7	J27	IO99NB3F9	R24
IO63PB1F5	J19	IO81PB2F7	H27	IO99PB3F9	R25
<b>Bank 2</b>		IO82NB2F7	L23	IO100NB3F9	T26
IO64NB2F6	J21	IO82PB2F7	L22	IO100PB3F9	T27
IO64PB2F6	H21	IO83NB2F7	L25	IO101NB3F9	T24
IO65NB2F6	F24	IO83PB2F7	L24	IO101PB3F9	T25
IO65PB2F6	F23	IO84NB2F7	N21	IO102NB3F9	R20
IO66NB2F6	F26	IO84PB2F7	M21	IO102PB3F9	R21
IO66PB2F6	F25	IO85NB2F8	K27	IO103NB3F9	R23
IO67NB2F6	E26	IO85PB2F8	K26	IO103PB3F9	R22
IO67PB2F6	E25	IO86NB2F8	M23	IO104NB3F9	U26
IO68NB2F6	J22	IO86PB2F8	M22	IO104PB3F9	U27
IO68PB2F6	H22	IO87NB2F8	M25	IO105NB3F9	U24
IO69NB2F6	G24	IO87PB2F8	M24	IO105PB3F9	U25
IO69PB2F6	G23	IO88NB2F8	L27	IO106NB3F9	R19
IO70NB2F6	K20	IO88PB2F8	L26	IO106PB3F9	P19
IO70PB2F6	J20	IO89NB2F8	M27	IO107NB3F10	V26
IO71NB2F6	G26	IO89PB2F8	M26	IO107PB3F10	V27
IO71PB2F6	G25	IO90NB2F8	N23	IO108NB3F10	T23
IO72NB2F6	J24	IO90PB2F8	N22	IO108PB3F10	T22

## FG1152

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### Note

For Package Manufacturing and Environmental information, visit Resource center at  
<http://www.microsemi.com/soc/products/rescenter/package/index.html>.

<b>FG1152</b>	
<b>AX2000 Function</b>	<b>Pin Number</b>
IO155PB3F14	AC29
IO156NB3F14	AE30
IO156PB3F14	AD30
IO157NB3F14	AC26
IO157PB3F14	AB26
IO158NB3F14	AH33
IO158PB3F14	AG33
IO159NB3F14	AD27
IO159PB3F14	AC27
IO160NB3F14	AG32
IO160PB3F14	AF32
IO161NB3F15	AG31
IO161PB3F15	AF31
IO162NB3F15	AF29
IO162PB3F15	AE29
IO163NB3F15	AE28
IO163PB3F15	AD28
IO164NB3F15	AG30
IO164PB3F15	AF30
IO165NB3F15	AE26
IO165PB3F15	AD26
IO166NB3F15	AJ30
IO166PB3F15	AH30
IO167NB3F15	AG28
IO167PB3F15	AF28
IO168NB3F15	AF27
IO168PB3F15	AE27
IO169NB3F15	AH29
IO169PB3F15	AG29
IO170NB3F15	AD25
IO170PB3F15	AC25
<b>Bank 4</b>	
IO171NB4F16	AP29
IO171PB4F16	AN29
IO172NB4F16	AH26

<b>FG1152</b>	
<b>AX2000 Function</b>	<b>Pin Number</b>
IO172PB4F16	AH27
IO173NB4F16	AJ27
IO173PB4F16	AJ28
IO174NB4F16	AL27
IO174PB4F16	AL28
IO175NB4F16	AM28
IO175PB4F16	AM29
IO176NB4F16	AG25
IO176PB4F16	AG26
IO177NB4F16	AK26
IO177PB4F16	AK27
IO178NB4F16	AF25
IO178PB4F16	AE25
IO179NB4F16	AP28
IO179PB4F16	AN28
IO180NB4F16	AJ25
IO180PB4F16	AJ26
IO181NB4F17	AM26
IO181PB4F17	AM27
IO182NB4F17	AF24
IO182PB4F17	AE24
IO183NB4F17	AH24
IO183PB4F17	AH25
IO184NB4F17	AG23
IO184PB4F17	AG24
IO185NB4F17	AL25
IO185PB4F17	AL26
IO186NB4F17	AP25
IO186PB4F17	AP26
IO187NB4F17	AK24
IO187PB4F17	AK25
IO188NB4F17	AF23
IO188PB4F17	AE23
IO189NB4F17	AN24
IO189PB4F17	AM24

<b>FG1152</b>	
<b>AX2000 Function</b>	<b>Pin Number</b>
IO190NB4F17	AH22
IO190PB4F17	AH23
IO191NB4F17	AJ23
IO191PB4F17	AJ24
IO192NB4F17	AG21
IO192PB4F17	AG22
IO193NB4F18	AP23
IO193PB4F18	AP24
IO194NB4F18	AN22
IO194PB4F18	AN23
IO195NB4F18	AM23
IO195PB4F18	AL23
IO196NB4F18	AF21
IO196PB4F18	AF22
IO197NB4F18	AL22
IO197PB4F18	AM22
IO198NB4F18	AE21
IO198PB4F18	AE22
IO199NB4F18	AJ21
IO199PB4F18	AJ22
IO200NB4F18	AK21
IO200PB4F18	AK22
IO201NB4F18	AM21
IO201PB4F18	AL21
IO202NB4F18	AE20
IO202PB4F18	AD20
IO203NB4F19	AN21
IO203PB4F19	AP21
IO204NB4F19	AP20
IO204PB4F19	AN20
IO205NB4F19	AN19
IO205PB4F19	AP19
IO206NB4F19	AG20
IO206PB4F19	AF20
IO207NB4F19	AL19

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
<b>Dedicated I/O</b>	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ208	
AX500 Function	Pin Number
<b>Bank 0</b>	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
<b>Bank 1</b>	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
<b>Bank 2</b>	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132

CQ208	
AX500 Function	Pin Number
<b>Bank 3</b>	
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
<b>Bank 4</b>	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
<b>Bank 5</b>	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
<b>Bank 6</b>	
IO105NB5F10/CLKGN	76

CQ208	
AX500 Function	Pin Number
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
<b>Bank 6</b>	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
<b>Bank 7</b>	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18

CQ352	
AX250 Function	Pin Number
<b>Bank 0</b>	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
<b>Bank 1</b>	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282

CQ352	
AX250 Function	Pin Number
<b>Bank 2</b>	
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
<b>Bank 3</b>	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
<b>Bank 4</b>	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

CQ352	
AX250 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO131PB4F12	171	IO187PB5F17	99	IO224NB6F20	46
IO132NB4F12	166	IO188NB5F17	100	IO224PB6F20	47
IO132PB4F12	167	IO188PB5F17	101	<b>Bank 7</b>	
IO133NB4F12	164	IO190NB5F17	94	IO225NB7F21	40
IO133PB4F12	165	IO190PB5F17	95	IO225PB7F21	41
IO134NB4F12	160	IO192NB5F17	92	IO226NB7F21	42
IO134PB4F12	161	IO192PB5F17	93	IO226PB7F21	43
IO136NB4F12	158	<b>Bank 6</b>		IO237NB7F22	34
IO136PB4F12	159	IO193PB6F18	86	IO237PB7F22	35
IO137NB4F12	154	IO194NB6F18	84	IO238NB7F22	36
IO137PB4F12	155	IO194PB6F18	85	IO238PB7F22	37
IO138NB4F12	152	IO196NB6F18	78	IO240NB7F22	30
IO138PB4F12	153	IO196PB6F18	79	IO240PB7F22	31
IO153NB4F14	146	IO197NB6F18	82	IO241NB7F22	28
IO153PB4F14	147	IO197PB6F18	83	IO241PB7F22	29
IO159NB4F14/CLKEN	142	IO198NB6F18	76	IO242NB7F22	24
IO159PB4F14/CLKEP	143	IO198PB6F18	77	IO242PB7F22	25
IO160NB4F14/CLKFN	136	IO203NB6F19	72	IO244NB7F22	22
IO160PB4F14/CLKFP	137	IO203PB6F19	73	IO244PB7F22	23
<b>Bank 5</b>		IO204NB6F19	70	IO245NB7F22	18
IO161NB5F15/CLKGN	128	IO204PB6F19	71	IO245PB7F22	19
IO161PB5F15/CLKGP	129	IO205NB6F19	66	IO246NB7F22	16
IO162NB5F15/CLKHN	122	IO205PB6F19	67	IO246PB7F22	17
IO162PB5F15/CLKHP	123	IO206NB6F19	64	IO249NB7F23	12
IO167NB5F15	118	IO206PB6F19	65	IO249PB7F23	13
IO167PB5F15	119	IO207NB6F19	60	IO250NB7F23	10
IO183NB5F17	110	IO207PB6F19	61	IO250PB7F23	11
IO183PB5F17	111	IO208NB6F19	58	IO256NB7F23	4
IO184NB5F17	112	IO208PB6F19	59	IO256PB7F23	5
IO184PB5F17	113	IO211NB6F19	54	IO257NB7F23	6
IO185NB5F17	104	IO211PB6F19	55	IO257PB7F23	7
IO185PB5F17	105	IO212NB6F19	52	<b>Dedicated I/O</b>	
IO186NB5F17	106	IO212PB6F19	53	GND	1
IO186PB5F17	107	IO223NB6F20	48	GND	9
IO187NB5F17	98	IO223PB6F20	49	GND	15

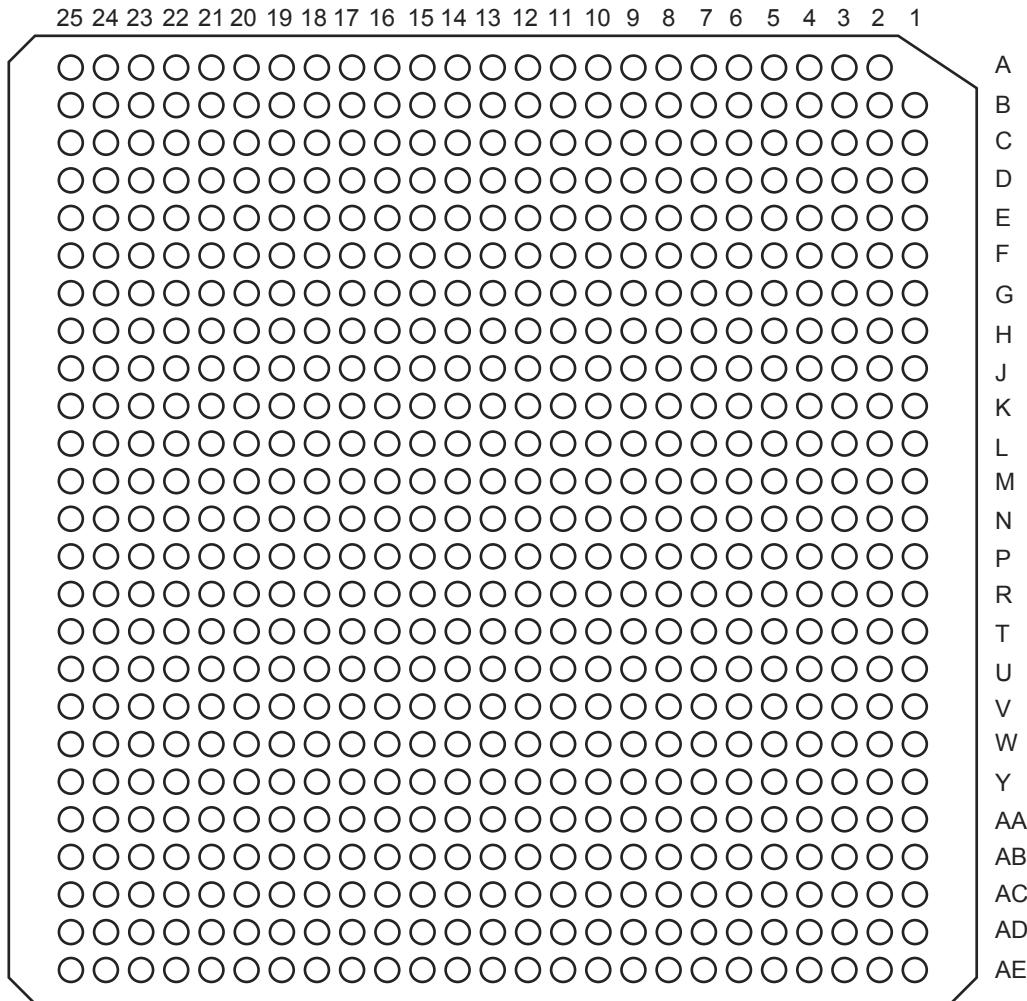
CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15

## CG624

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### Note

For Package Manufacturing and Environmental information, visit Resource center at  
<http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO194NB6F18	Y3	IO215PB6F20	V4	IO237NB7F22	N8
IO194PB6F18	AA3	IO216NB6F20	P8	IO237PB7F22	N7
IO195NB6F18	V6	IO216PB6F20	R3	IO238NB7F22	M5
IO195PB6F18	W4	IO217NB6F20	P7	IO239NB7F22	L6
IO197NB6F18	R5	IO217PB6F20	R7	IO239PB7F22	L5
IO197PB6F18	U3	IO219NB6F20	R4	IO240NB7F22	M4
IO198NB6F18	P6	IO219PB6F20	T4	IO241NB7F22	L7
IO199NB6F18	Y5	IO220NB6F20	P2	IO241PB7F22	M7
IO199PB6F18	W5	IO220PB6F20	R2	IO242NB7F22	J3
IO200NB6F18	V3	IO221NB6F20	N4	IO243NB7F22	M9
IO200PB6F18	W3	IO221PB6F20	P4	IO243PB7F22	M8
IO201NB6F18	T7	IO223NB6F20	M2	IO244NB7F22	P9
IO201PB6F18	U7	IO223PB6F20	N2	IO244PB7F22	N6
IO202NB6F18	V2	IO224NB6F20	N3	IO245NB7F22	K8
IO203NB6F19	W2	IO224PB6F20	P3	IO245PB7F22	L8
<b>Bank 7</b>					
IO203PB6F19	Y2	IO225NB7F21	J2	IO246NB7F22	F3
IO204NB6F19	AA1	IO225PB7F21	J1	IO246PB7F22	E3
IO204PB6F19	AB1	IO226PB7F21	G2	IO247NB7F23	K7
IO205NB6F19	R6	IO227NB7F21	H3	IO247PB7F23	K6
IO205PB6F19	T6	IO227PB7F21	H2	IO248NB7F23	D2
IO206NB6F19	W1	IO229NB7F21	K2	IO249NB7F23	G4
IO206PB6F19	Y1	IO229PB7F21	L2	IO249PB7F23	G3
IO207NB6F19	T2	IO230NB7F21	K1	IO251NB7F23	N10
IO207PB6F19	U2	IO230PB7F21	L1	IO251PB7F23	N9
IO208NB6F19	T1	IO231NB7F21	E2	IO253NB7F23	H4
IO208PB6F19	U1	IO231PB7F21	F2	IO253PB7F23	J4
IO209NB6F19	AA2	IO232NB7F21	F1	IO255NB7F23	J6
IO209PB6F19	AB2	IO232PB7F21	G1	IO255PB7F23	J5
IO210NB6F19	P5	IO233NB7F21	L3	IO257NB7F23	H5
IO211NB6F19	M1	IO233PB7F21	M3	IO257PB7F23	H6
IO211PB6F19	N1	IO234NB7F21	D1	<b>Dedicated I/O</b>	
IO212NB6F19	P1	IO234PB7F21	E1	GND	K5
IO212PB6F19	R1	IO235NB7F21	K4	GND	A18
IO213NB6F19	R8	IO235PB7F21	L4	GND	A2
IO213PB6F19	T8	IO236NB7F22	M6	GND	A24
IO215NB6F20	U4			GND	A25

Revision	Changes	Page
Revision 8 (continued)	The following changes were made in the "FG676"(AX500) section: AE2, AE25 Change from NC to GND. AF2, AF25 Changed from GND to NC AB4, AF24, C1, C26 Changed from V <sub>CCDA</sub> to V <sub>CCA</sub> AD15 Change from V <sub>CCDA</sub> to V <sub>COMPLE</sub> AD17 Changed from V <sub>COMPLE</sub> to V <sub>CCDA</sub>	3-37
	In the "FG896" (AX2000) section, the AK28 changed from VCCIB5 to VCCIB4.	3-52
	The "CQ352" and "CG624" sections are new.	3-98, 3-115
Revision 7 (Advance v1.6)	All I/O FIFO capability was removed.	n/a
	Table 1 was updated.	i
	Figure 1-9 was updated.	1-7
	Figure 2-5 was updated.	2-16
	The "Using an I/O Register" section was updated.	2-16
	The AX250 and AX1000 descriptions were added to the "FG484"section.	3-21
Revision 6 (Advance v1.5)	Table 2-3 was updated.	2-2
	Figure 2-1 was updated.	2-8
	Figure 2-48 was updated.	2-75
	Figure 2-52 was updated.	2-82
Revision 5 (Advance v1.4)	In the "PQ208" table, pin 196 was missing, but it has been added in this version with a function of GND.	3-84
	The following pins in the "FG484" table for AX500 were changed: Pin G7 is GND/LP Pins AB8, C10, C11, C14, AB16 are NC.	3-21
	The "FG676" table was updated.	3-37
	The "Device Resources" section was updated for the CS180.	ii
Revision 4 (Advance v1.3)	The "Programmable Interconnect Element" and Figure 1-2 are new.	1-1 and 1-2
	The "CS180" table is new.	3-1
	The "PQ208" tables for the AX500 were updated. The following pins were not defined in the previous version: GND 21 IO106PB5F10/CLKHP 71 GND 136	3-84
	Table 1, "Ordering Information", "Device Resources", and the Product Plan table were updated.	i, ii
Revision 3 (Advance v1.2)	The following figures and tables were updated: Figure 1-3 Figure 1-8 (new) Table 2-3 Figure 2-2 Table 2-8 Figure 2-11	1-2 1-6 2-2 2-9 2-12 2-23
	The "Design Environment" section was updated.	1-7
	The "Package Thermal Characteristics" was updated.	2-6