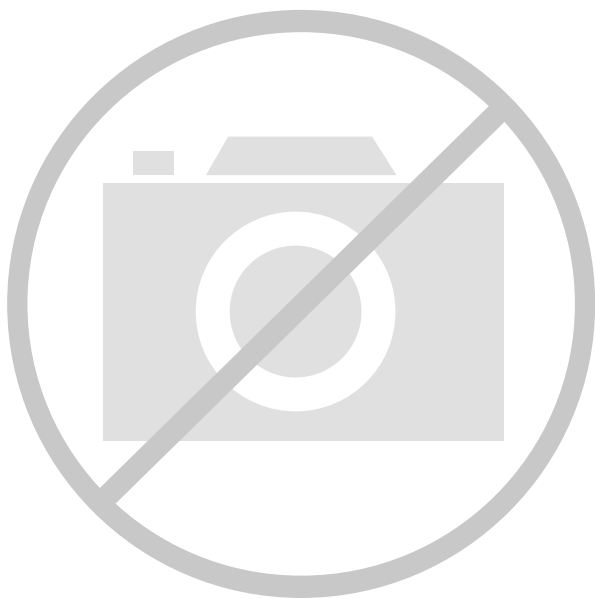




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	729-BBGA
Supplier Device Package	729-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1bg729m

1 – General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microsemi AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

Device Architecture

AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

The very nature of Microsemi's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-108).

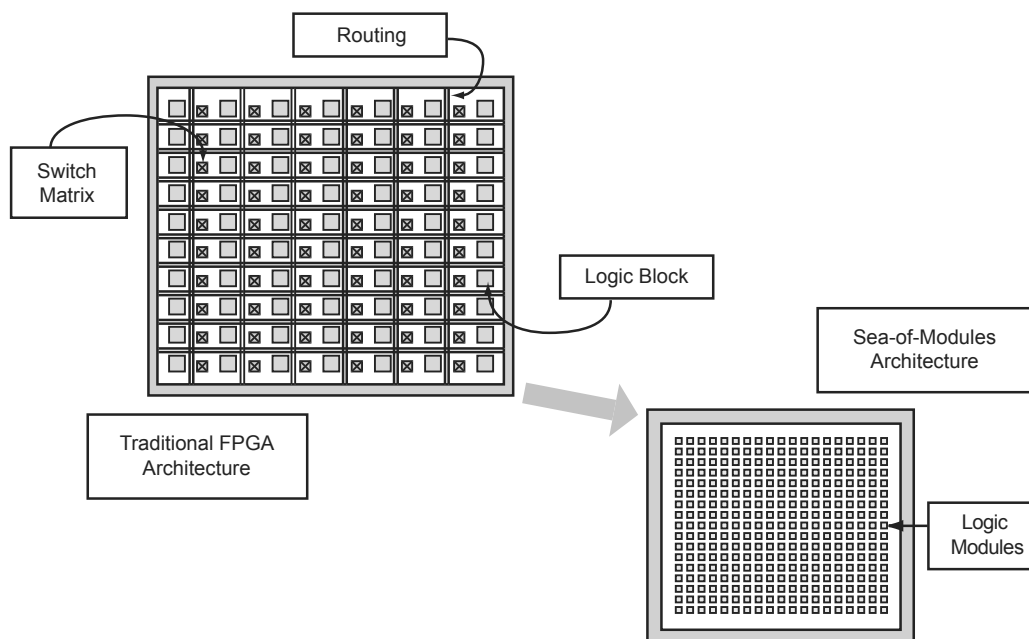


Figure 1-1 • Sea-of-Modules Comparison

User I/Os²

Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-8 on page 2-12 contains the I/O standards supported by the Axcelerator family, and Table 2-10 on page 2-12 compares the features of the different I/O standards.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (Figure 2-6 on page 2-18). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules:

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.
- Dedicated I/O pins such as GND and VCCI are counted as part of the 16.
- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.
- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3 V.

A user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.
- Use generic I/O macros and then use Designer's PinEditor to specify the desired I/O standards (please note that this is not applicable to differential standards).
- A combination of the first two methods.

Refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

2. Do not use an external resistor to pull the I/O above V_{CCI} for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above V_{CCI} .

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

Table 2-11 • Compatible I/O Standards for Different VREF Values

VREF	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5V and 3.3V Outputs)
0.75 V	HSTL (Class I)

Table 2-12 • Compatible I/O Standards for Different VCCI Values

VCCI ¹	Compatible Standards	VREF
3.3 V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVC MOS 2.5 V, GTL+ 2.5 V, LVDS ²	1.0
2.5 V	LVC MOS 2.5 V, SSTL 2 (Classes I and II), LVDS ²	1.25
1.8 V	LVC MOS 1.8 V	N/A
1.5 V	LVC MOS 1.5 V, HSTL Class I	0.75

Notes:

1. VCCI is used for both inputs and outputs
2. VCCI tolerance is $\pm 5\%$

User I/O Naming Conventions

Due to the complex and flexible nature of the Axcelerator family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (Figure 2-7).

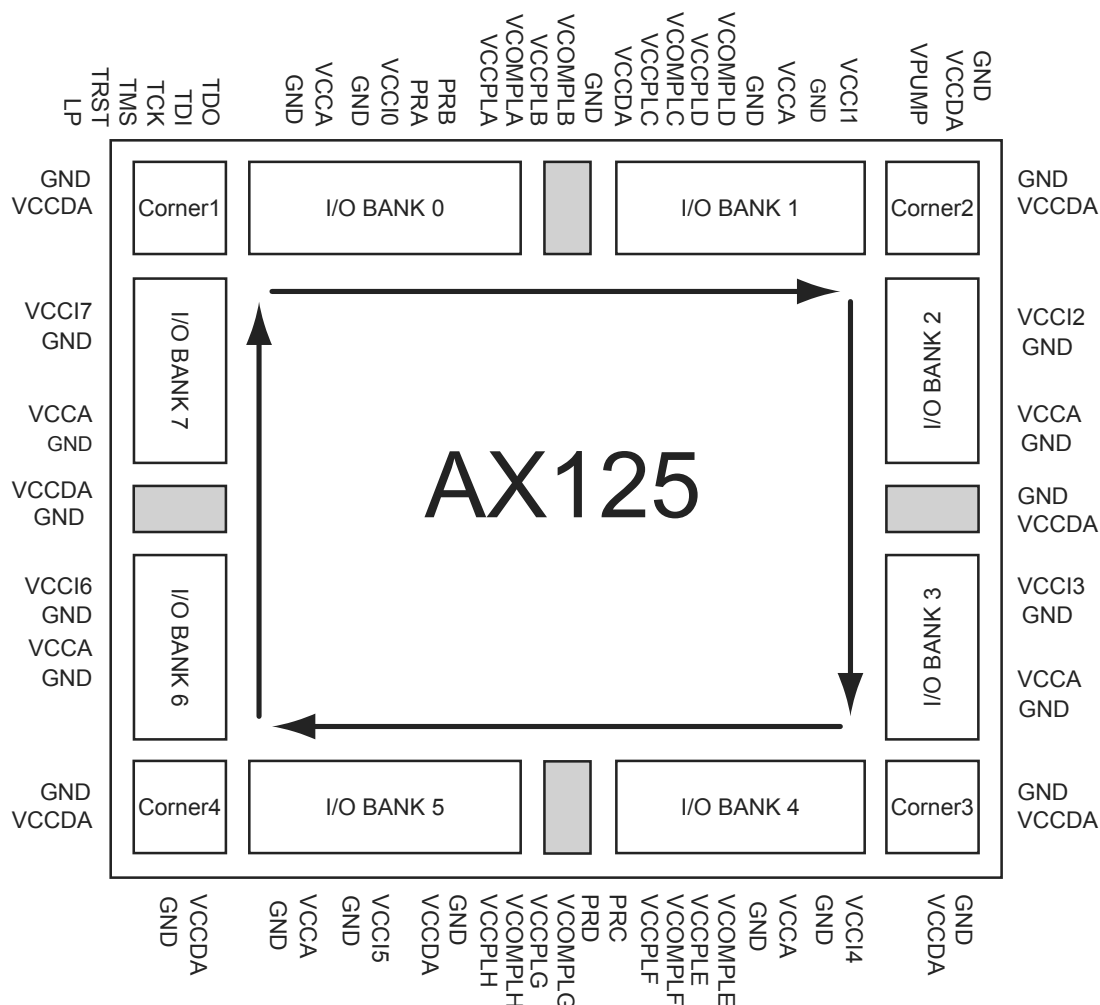
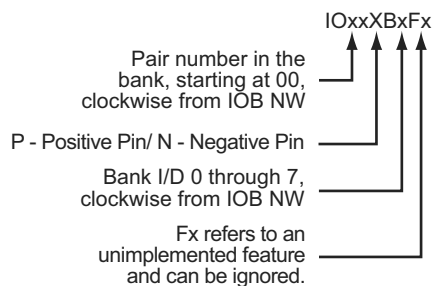


Figure 2-7 • I/O Bank and Dedicated Pin Layout



Examples:

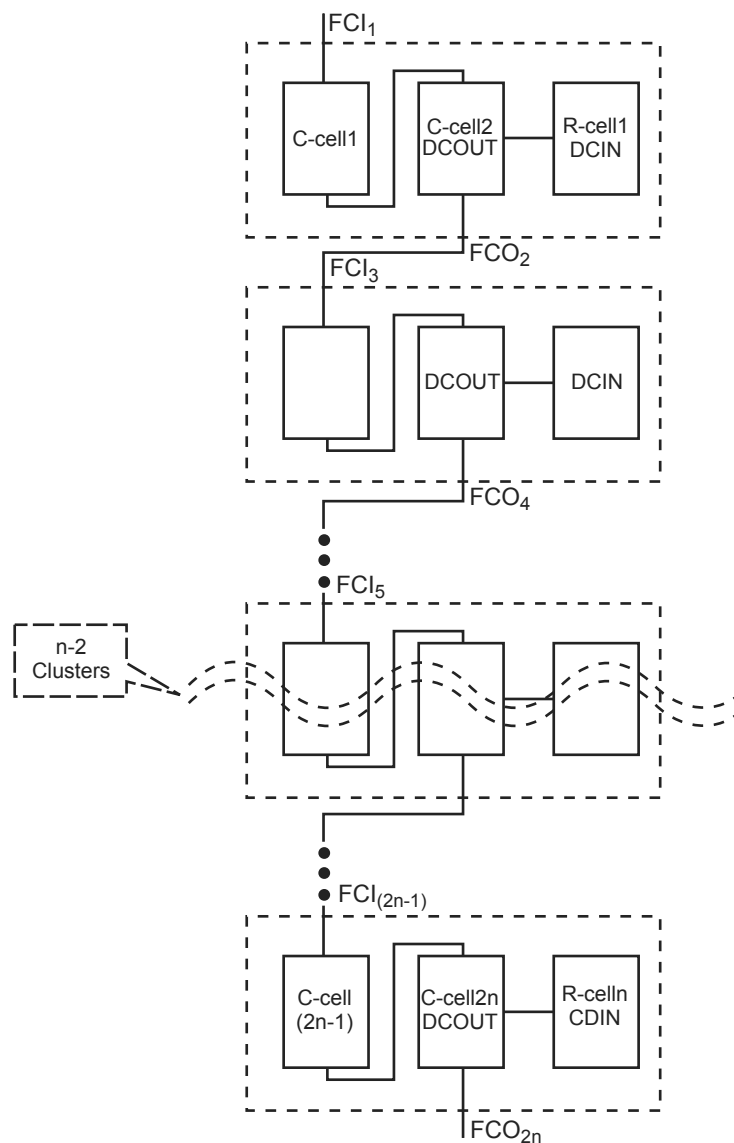
IO12PB1F1 is the positive pin of the thirteenth pair of the first I/O bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair.

For those I/Os that can be employed either as a user I/O or as a special function, the following nomenclature is used:

IOxxXBxFx/special_function_name

IOxxPB1Fx/xCLKx this pin can be configured as a clock input or as a user I/O.

Figure 2-8 • General Naming Schemes



Note: The carry-chain sequence can end on either C-cell.

Figure 2-30 • Carry-Chain Sequencing of C-Cells

Timing Characteristics

Refer to Table 2-62 on page 2-55 for more information on carry-chain timing.

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-70 • AX125 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-71 • AX250 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t _{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-72 • AX500 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.35		2.68		3.15	ns
t _{HCKH}	Input High to Low		2.44		2.79		3.27	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-73 • AX1000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-74 • AX2000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

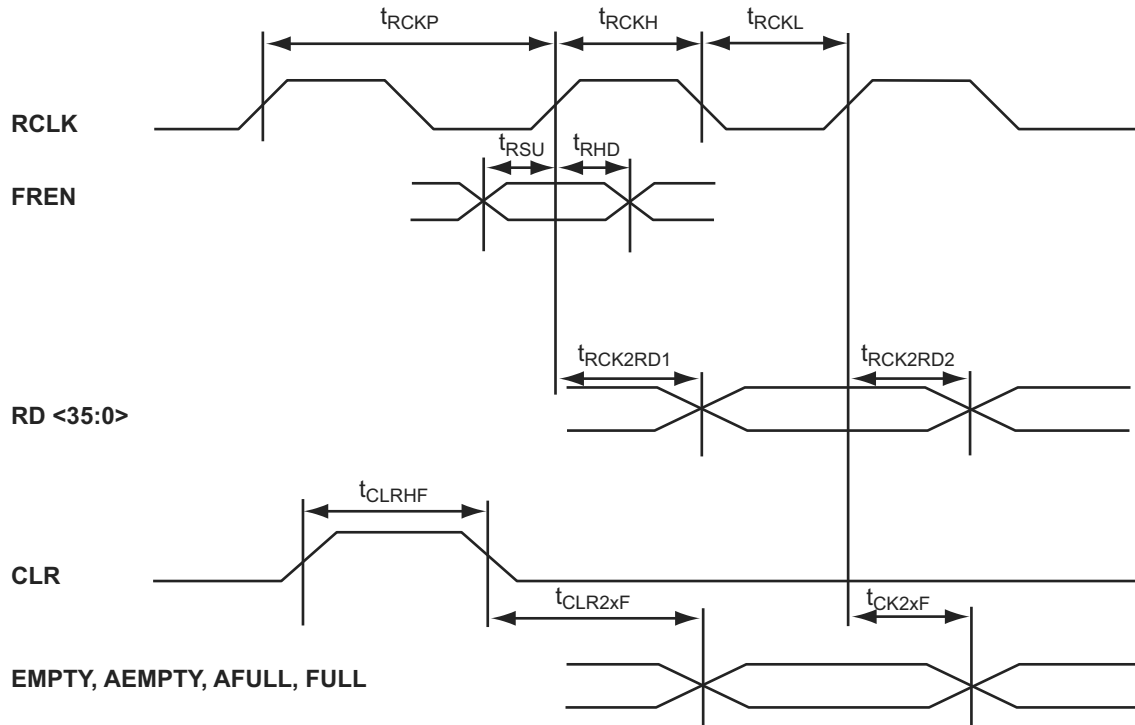
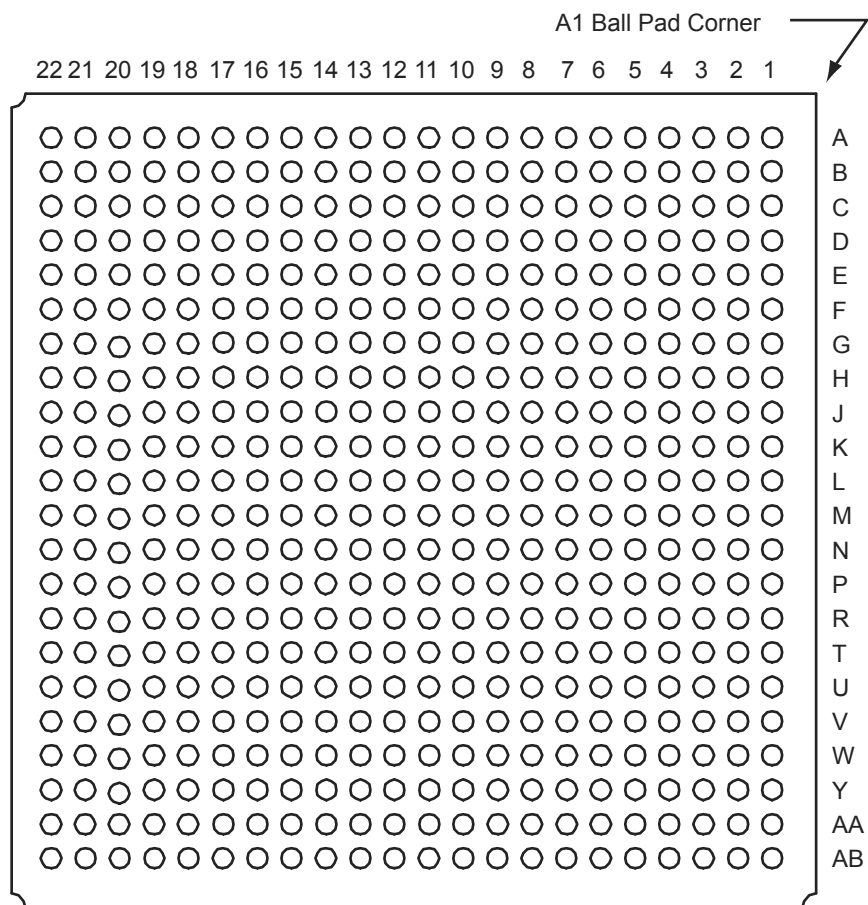


Figure 2-68 • FIFO Read Timing

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO163PB5F15	AA14	IO182NB5F17	AF7	IO200NB6F18	AA4
IO164NB5F15	AE13	IO182PB5F17	AG7	IO200PB6F18	AA5
IO164PB5F15	AF13	IO183NB5F17	AD7	IO201NB6F18	W5
IO165NB5F15	AF12	IO183PB5F17	AE7	IO201PB6F18	W6
IO165PB5F15	AG12	IO184NB5F17	AC7	IO202NB6F18	AB1
IO166NB5F15	AD12	IO184PB5F17	AC8	IO202PB6F18	AC1
IO166PB5F15	AE12	IO185NB5F17	AF6	IO203NB6F19	Y3
IO167NB5F15	Y13	IO185PB5F17	AG6	IO203PB6F19	AA3
IO167PB5F15	AA13	IO186NB5F17	AB7	IO204NB6F19	AA2
IO168NB5F15	AD11	IO186PB5F17	AB8	IO204PB6F19	AB2
IO168PB5F15	AE11	IO187NB5F17	Y9	IO205NB6F19	U8
IO169NB5F15	AG11	IO187PB5F17	AA9	IO205PB6F19	V8
IO169PB5F15	AF11	IO188NB5F17	AD6	IO206NB6F19	V5
IO170NB5F15	AB11	IO188PB5F17	AE6	IO206PB6F19	V6
IO170PB5F15	AC11	IO189NB5F17	AB6	IO207NB6F19	Y1
IO171NB5F16	AF10	IO189PB5F17	AC6	IO207PB6F19	AA1
IO171PB5F16	AG10	IO190NB5F17	AF5	IO208NB6F19	W4
IO172NB5F16	AD10	IO190PB5F17	AG5	IO208PB6F19	Y4
IO172PB5F16	AE10	IO191NB5F17	AA6	IO209NB6F19	T7
IO173NB5F16	Y12	IO191PB5F17	AA7	IO209PB6F19	U7
IO173PB5F16	AA12	IO192NB5F17	Y8	IO210NB6F19	W2
IO174NB5F16	AB10	IO192PB5F17	AA8	IO210PB6F19	Y2
IO174PB5F16	AC10	Bank 6		IO211NB6F19	U5
IO175NB5F16	AF9	IO193NB6F18	W8	IO211PB6F19	U6
IO175PB5F16	AG9	IO193PB6F18	Y7	IO212NB6F19	V3
IO176NB5F16	AD9	IO194NB6F18	AB5	IO212PB6F19	W3
IO176PB5F16	AE9	IO194PB6F18	AC5	IO213NB6F19	R9
IO177NB5F16	Y11	IO195NB6F18	AC2	IO213PB6F19	T8
IO177PB5F16	AA11	IO195PB6F18	AC3	IO214NB6F20	U4
IO178NB5F16	AF8	IO196NB6F18	AC4	IO214PB6F20	V4
IO178PB5F16	AG8	IO196PB6F18	AD4	IO215NB6F20	T5
IO179NB5F16	AD8	IO197NB6F18	Y5	IO215PB6F20	T6
IO179PB5F16	AE8	IO197PB6F18	Y6	IO216NB6F20	V1
IO180NB5F16	AB9	IO198NB6F18	AB3	IO216PB6F20	W1
IO180PB5F16	AC9	IO198PB6F18	AB4	IO217NB6F20	R7
IO181NB5F17	Y10	IO199NB6F18	V7	IO217PB6F20	R8
IO181PB5F17	AA10	IO199PB6F18	W7	IO218NB6F20	U2

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 0		IO20NB2F2	F15	IO41PB3F3	L14
IO01NB0F0	B4	IO20PB2F2	E15	Bank 4	
IO01PB0F0	B3	IO21NB2F2	C16	IO42NB4F4	N12
IO03NB0F0	A4	IO21PB2F2	B16	IO42PB4F4	N13
IO03PB0F0	A3	IO22NB2F2	H13	IO43NB4F4	T14
IO04NB0F0	B6	IO22PB2F2	G13	IO43PB4F4	R14
IO04PB0F0	B5	IO23NB2F2	E16	IO44PB4F4	T15
IO06NB0F0	A6	IO23PB2F2	D16	IO45NB4F4	R12
IO06PB0F0	A5	IO25NB2F2	H15	IO45PB4F4	R13
IO07NB0F0/HCLKAN	B8	IO25PB2F2	G15	IO46NB4F4	P11
IO07PB0F0/HCLKAP	B7	IO26NB2F2	H14	IO46PB4F4	P12
IO08NB0F0/HCLKBN	A9	IO26PB2F2	G14	IO47PB4F4	T11
IO08PB0F0/HCLKBP	A8	IO27NB2F2	G16	IO48NB4F4	T12
Bank 1		IO27PB2F2	F16	IO48PB4F4	T13
IO09NB1F1/HCLKCN	C10	IO28NB2F2	K15	IO49NB4F4/CLKEN	R9
IO09PB1F1/HCLKCP	C9	IO28PB2F2	K16	IO49PB4F4/CLKEP	R10
IO10NB1F1/HCLKDN	B11	IO29NB2F2	J16	IO50NB4F4/CLKFN	T8
IO10PB1F1/HCLKDP	B10	IO29PB2F2	H16	IO50PB4F4/CLKFP	T9
IO12NB1F1	A13	Bank 3		Bank 5	
IO12PB1F1	A12	IO30NB3F3	K13	IO51NB5F5/CLKGN	P7
IO13NB1F1	B13	IO30PB3F3	J13	IO51PB5F5/CLKGP	P8
IO13PB1F1	B12	IO31NB3F3	K14	IO52NB5F5/CLKHN	R6
IO14NB1F1	C12	IO31PB3F3	J14	IO52PB5F5/CLKHP	R7
IO14PB1F1	C11	IO33NB3F3	L15	IO54NB5F5	T5
IO15NB1F1	A15	IO33PB3F3	L16	IO54PB5F5	T6
IO15PB1F1	B14	IO35NB3F3	P16	IO55NB5F5	P5
IO16NB1F1	C15	IO35PB3F3	N16	IO55PB5F5	P6
IO16PB1F1	C14	IO36PB3F3	M16	IO56NB5F5	T3
IO17NB1F1	D13	IO37NB3F3	P15	IO56PB5F5	T4
IO17PB1F1	D12	IO37PB3F3	R16	IO57NB5F5	R3
Bank 2		IO39NB3F3	N15	IO57PB5F5	R4
IO18NB2F2	F13	IO39PB3F3	M15	IO58NB5F5	R1
IO18PB2F2	E13	IO40NB3F3	M13	IO58PB5F5	T2
IO19NB2F2	F14	IO40PB3F3	L13	IO59NB5F5	N4
IO19PB2F2	E14	IO41NB3F3	M14	IO59PB5F5	N5

FG484



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
IO104PB6F6	N4	IO122NB7F7	G5	GND	J9
IO105NB6F6	M5	IO122PB7F7	G6	GND	K10
IO105PB6F6	N5	IO123NB7F7	F5	GND	K11
IO106NB6F6	M3	IO123PB7F7	E4	GND	K12
IO106PB6F6	N3	Dedicated I/O		GND	K13
Bank 7		VCCDA	H7	GND	L1
IO107NB7F7	M2	GND	A1	GND	L10
IO107PB7F7	N1	GND	A11	GND	L11
IO108NB7F7	L3	GND	A12	GND	L12
IO108PB7F7	L2	GND	A2	GND	L13
IO109NB7F7	K2	GND	A21	GND	L22
IO109PB7F7	K1	GND	A22	GND	M1
IO110NB7F7	K5	GND	AA1	GND	M10
IO110PB7F7	L5	GND	AA2	GND	M11
IO111NB7F7	K6	GND	AA21	GND	M12
IO111PB7F7	L6	GND	AA22	GND	M13
IO112NB7F7	K4	GND	AB1	GND	M22
IO112PB7F7	K3	GND	AB11	GND	N10
IO113NB7F7	K7	GND	AB12	GND	N11
IO113PB7F7	L7	GND	AB2	GND	N12
IO114NB7F7	H1	GND	AB21	GND	N13
IO114PB7F7	J1	GND	AB22	GND	P14
IO115NB7F7	H2	GND	B1	GND	P9
IO115PB7F7	J2	GND	B2	GND	R15
IO116NB7F7	H4	GND	B21	GND	R8
IO116PB7F7	J4	GND	B22	GND	U16
IO117NB7F7	H5	GND	C20	GND	U6
IO117PB7F7	J5	GND	C3	GND	V18
IO118NB7F7	F2	GND	D19	GND	V5
IO118PB7F7	G2	GND	D4	GND	W19
IO119NB7F7	H6	GND	E18	GND	W4
IO119PB7F7	J6	GND	E5	GND	Y20
IO120NB7F7	F1	GND	G18	GND	Y3
IO120PB7F7	G1	GND	H15	GND/LP	G7
IO121NB7F7	F4	GND	H8	NC	A17
IO121PB7F7	G4	GND	J14	NC	A18

FG484	
AX1000 Function	Pin Number
IO167PB5F15	AA12
IO169NB5F15	AA9
IO169PB5F15	AA10
IO170NB5F15	AB9
IO170PB5F15	AB10
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	Y8
IO172PB5F16	Y9
IO173NB5F16	U8
IO173PB5F16	U9
IO174NB5F16	AA7
IO174PB5F16	AA8
IO175NB5F16	AB5
IO175PB5F16	AB6
IO176NB5F16	AA5
IO176PB5F16	AA6
IO177NB5F16	AA4
IO177PB5F16	AB4
IO178NB5F16	Y6
IO178PB5F16	Y7
IO179NB5F16	T7
IO179PB5F16	T8
IO180NB5F16	W6
IO180PB5F16	W7
IO181NB5F17	Y4
IO181PB5F17	Y5
IO184NB5F17	AB7
IO187NB5F17	V3
IO187PB5F17	W3
IO188NB5F17	V4
IO188PB5F17	W5
IO192NB5F17	V6
IO192PB5F17	V7
Bank 6	

FG484	
AX1000 Function	Pin Number
IO194NB6F18	V2
IO194PB6F18	W2
IO195NB6F18	U5
IO195PB6F18	T5
IO200NB6F18	T4
IO200PB6F18	U4
IO201NB6F18	P6
IO201PB6F18	R6
IO203NB6F19	U2
IO204NB6F19	T3
IO204PB6F19	U3
IO205NB6F19	P5
IO205PB6F19	R5
IO208NB6F19	V1
IO208PB6F19	W1
IO209NB6F19	P7
IO209PB6F19	R7
IO212NB6F19	P4
IO212PB6F19	R4
IO214NB6F20	P3
IO214PB6F20	R3
IO215NB6F20	M6
IO215PB6F20	N6
IO216NB6F20	R2
IO216PB6F20	T2
IO217NB6F20	T1
IO217PB6F20	U1
IO219NB6F20	M5
IO219PB6F20	N5
IO220NB6F20	P1
IO220PB6F20	R1
IO221NB6F20	N2
IO221PB6F20	P2
IO222NB6F20	M3
IO222PB6F20	N3

FG484	
AX1000 Function	Pin Number
IO223NB6F20	M7
IO223PB6F20	N7
IO224NB6F20	M4
IO224PB6F20	N4
Bank 7	
IO225NB7F21	M2
IO225PB7F21	N1
IO226NB7F21	K2
IO226PB7F21	K1
IO228NB7F21	L3
IO228PB7F21	L2
IO229NB7F21	K5
IO229PB7F21	L5
IO230NB7F21	H1
IO230PB7F21	J1
IO231NB7F21	H2
IO231PB7F21	J2
IO232NB7F21	K4
IO232PB7F21	K3
IO233NB7F21	K6
IO233PB7F21	L6
IO234NB7F21	F1
IO234PB7F21	G1
IO235NB7F21	F2
IO235PB7F21	G2
IO236NB7F22	H3
IO236PB7F22	J3
IO237NB7F22	K7
IO237PB7F22	L7
IO241NB7F22	H6
IO241PB7F22	J6
IO242NB7F22	H4
IO242PB7F22	J4
IO243NB7F22	H5
IO243PB7F22	J5

FG676	
AX1000 Function	Pin Number
NC	D13
NC	D14
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18

FG676	
AX1000 Function	Pin Number
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14
VCCA	V15
VCCA	V16
VCCA	V17
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCCDA	A11
VCCDA	A3
VCCDA	AB22
VCCDA	AB5
VCCDA	AD10
VCCDA	AD11
VCCDA	AD13
VCCDA	AD16
VCCDA	AD17
VCCDA	B1
VCCDA	B11
VCCDA	B17
VCCDA	C16
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23

FG676	
AX1000 Function	Pin Number
VCCIB0	G10
VCCIB0	G8
VCCIB0	G9
VCCIB0	H10
VCCIB0	H11
VCCIB0	H12
VCCIB0	H13
VCCIB0	H9
VCCIB1	G17
VCCIB1	G18
VCCIB1	G19
VCCIB1	H14
VCCIB1	H15
VCCIB1	H16
VCCIB1	H17
VCCIB1	H18
VCCIB2	H20
VCCIB2	J19
VCCIB2	J20
VCCIB2	K19
VCCIB2	K20
VCCIB2	L19
VCCIB2	M19
VCCIB2	N19
VCCIB3	P19
VCCIB3	R19
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0		IO17NB0F1	B11	IO34NB1F3	A17
IO00NB0F0	D6	IO17PB0F1	B10	IO34PB1F3	B17
IO00PB0F0	E6	IO18NB0F1	D11	IO35NB1F3	D18
IO01NB0F0	A5	IO18PB0F1	E11	IO35PB1F3	C18
IO01PB0F0	B5	IO19NB0F1	C12	IO36NB1F3	H17
IO02NB0F0	G9	IO19PB0F1	C11	IO36PB1F3	J17
IO02PB0F0	G8	IO20NB0F1	F12	IO37NB1F3	B19
IO03NB0F0	F8	IO20PB0F1	G12	IO37PB1F3	A19
IO03PB0F0	F7	IO21NB0F1	D12	IO38NB1F3	H18
IO04NB0F0	D7	IO21PB0F1	E12	IO38PB1F3	J18
IO04PB0F0	E7	IO22NB0F2	H13	IO39NB1F3	B20
IO05NB0F0	C7	IO22PB0F2	J13	IO39PB1F3	A20
IO05PB0F0	C6	IO23NB0F2	A12	IO40NB1F3	C20
IO06NB0F0	H9	IO23PB0F2	A11	IO40PB1F3	C19
IO06PB0F0	H8	IO24NB0F2	F13	IO41NB1F4	E20
IO07NB0F0	D8	IO24PB0F2	G13	IO41PB1F4	E19
IO07PB0F0	E8	IO25NB0F2	B13	IO42NB1F4	F18
IO08NB0F0	E9	IO25PB0F2	B12	IO42PB1F4	G18
IO08PB0F0	F9	IO26NB0F2	E14	IO43NB1F4	A22
IO09NB0F0	A7	IO26PB0F2	E13	IO43PB1F4	A21
IO09PB0F0	B7	IO27NB0F2	B14	IO44NB1F4	F20
IO10NB0F0	H10	IO27PB0F2	A14	IO44PB1F4	F19
IO10PB0F0	G10	IO28NB0F2	H14	IO45NB1F4	D21
IO11NB0F0	C9	IO28PB0F2	J14	IO45PB1F4	D20
IO11PB0F0	C8	IO29NB0F2	B15	IO46NB1F4	D22
IO12NB0F1	E10	IO29PB0F2	A15	IO46PB1F4	C22
IO12PB0F1	F10	IO30NB0F2/HCLKAN	C14	IO47NB1F4	A25
IO13NB0F1	D10	IO30PB0F2/HCLKAP	D14	IO47PB1F4	A24
IO13PB0F1	D9	IO31NB0F2/HCLKBN	E15	IO48NB1F4	H19
IO14NB0F1	F11	IO31PB0F2/HCLKBP	D15	IO48PB1F4	G19
IO14PB0F1	G11	Bank 1		IO49NB1F4	C24
IO15NB0F1	A10	IO32NB1F3/HCLKCN	E17	IO49PB1F4	C23
IO15PB0F1	A9	IO32PB1F3/HCLKCP	E16	IO50NB1F4	G20
IO16NB0F1	H12	IO33NB1F3/HCLKDN	C17	IO50PB1F4	H20
IO16PB0F1	H11	IO33PB1F3/HCLKDP	D17	IO51NB1F4	F21

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO155PB3F14	AC29	IO172PB4F16	AH27	IO190NB4F17	AH22
IO156NB3F14	AE30	IO173NB4F16	AJ27	IO190PB4F17	AH23
IO156PB3F14	AD30	IO173PB4F16	AJ28	IO191NB4F17	AJ23
IO157NB3F14	AC26	IO174NB4F16	AL27	IO191PB4F17	AJ24
IO157PB3F14	AB26	IO174PB4F16	AL28	IO192NB4F17	AG21
IO158NB3F14	AH33	IO175NB4F16	AM28	IO192PB4F17	AG22
IO158PB3F14	AG33	IO175PB4F16	AM29	IO193NB4F18	AP23
IO159NB3F14	AD27	IO176NB4F16	AG25	IO193PB4F18	AP24
IO159PB3F14	AC27	IO176PB4F16	AG26	IO194NB4F18	AN22
IO160NB3F14	AG32	IO177NB4F16	AK26	IO194PB4F18	AN23
IO160PB3F14	AF32	IO177PB4F16	AK27	IO195NB4F18	AM23
IO161NB3F15	AG31	IO178NB4F16	AF25	IO195PB4F18	AL23
IO161PB3F15	AF31	IO178PB4F16	AE25	IO196NB4F18	AF21
IO162NB3F15	AF29	IO179NB4F16	AP28	IO196PB4F18	AF22
IO162PB3F15	AE29	IO179PB4F16	AN28	IO197NB4F18	AL22
IO163NB3F15	AE28	IO180NB4F16	AJ25	IO197PB4F18	AM22
IO163PB3F15	AD28	IO180PB4F16	AJ26	IO198NB4F18	AE21
IO164NB3F15	AG30	IO181NB4F17	AM26	IO198PB4F18	AE22
IO164PB3F15	AF30	IO181PB4F17	AM27	IO199NB4F18	AJ21
IO165NB3F15	AE26	IO182NB4F17	AF24	IO199PB4F18	AJ22
IO165PB3F15	AD26	IO182PB4F17	AE24	IO200NB4F18	AK21
IO166NB3F15	AJ30	IO183NB4F17	AH24	IO200PB4F18	AK22
IO166PB3F15	AH30	IO183PB4F17	AH25	IO201NB4F18	AM21
IO167NB3F15	AG28	IO184NB4F17	AG23	IO201PB4F18	AL21
IO167PB3F15	AF28	IO184PB4F17	AG24	IO202NB4F18	AE20
IO168NB3F15	AF27	IO185NB4F17	AL25	IO202PB4F18	AD20
IO168PB3F15	AE27	IO185PB4F17	AL26	IO203NB4F19	AN21
IO169NB3F15	AH29	IO186NB4F17	AP25	IO203PB4F19	AP21
IO169PB3F15	AG29	IO186PB4F17	AP26	IO204NB4F19	AP20
IO170NB3F15	AD25	IO187NB4F17	AK24	IO204PB4F19	AN20
IO170PB3F15	AC25	IO187PB4F17	AK25	IO205NB4F19	AN19
Bank 4		IO188NB4F17	AF23	IO205PB4F19	AP19
IO171NB4F16	AP29	IO188PB4F17	AE23	IO206NB4F19	AG20
IO171PB4F16	AN29	IO189NB4F17	AN24	IO206PB4F19	AF20
IO172NB4F16	AH26	IO189PB4F17	AM24	IO207NB4F19	AL19

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	AK12	GND	AN34	GND	D1
GND	AK17	GND	AN4	GND	D11
GND	AK18	GND	AN9	GND	D2
GND	AK23	GND	AP13	GND	D24
GND	AK30	GND	AP2	GND	D3
GND	AK5	GND	AP22	GND	D31
GND	AL1	GND	AP27	GND	D32
GND	AL11	GND	AP3	GND	D33
GND	AL2	GND	AP31	GND	D34
GND	AL24	GND	AP32	GND	D4
GND	AL3	GND	AP33	GND	E12
GND	AL31	GND	AP4	GND	E17
GND	AL32	GND	AP8	GND	E18
GND	AL33	GND	B1	GND	E23
GND	AL34	GND	B2	GND	E30
GND	AL4	GND	B26	GND	E5
GND	AM1	GND	B3	GND	F29
GND	AM10	GND	B31	GND	F30
GND	AM15	GND	B32	GND	F6
GND	AM2	GND	B33	GND	G28
GND	AM20	GND	B34	GND	G7
GND	AM25	GND	B4	GND	H1
GND	AM3	GND	B9	GND	H34
GND	AM31	GND	C1	GND	J2
GND	AM32	GND	C10	GND	J33
GND	AM33	GND	C15	GND	K3
GND	AM34	GND	C2	GND	K32
GND	AM4	GND	C20	GND	L11
GND	AN1	GND	C25	GND	L24
GND	AN2	GND	C3	GND	L31
GND	AN26	GND	C31	GND	L4
GND	AN3	GND	C32	GND	M12
GND	AN31	GND	C33	GND	M23
GND	AN32	GND	C34	GND	M30
GND	AN33	GND	C4	GND	M5

CQ256	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	248
IO01PB0F0	249
IO04NB0F0	246
IO04PB0F0	247
IO05NB0F0	242
IO05PB0F0	243
IO08NB0F0	240
IO08PB0F0	241
Bank 0	
IO37NB0F3	234
IO37PB0F3	235
IO41NB0F3/HCLKAN	232
IO41PB0F3/HCLKAP	233
IO42NB0F3/HCLKBN	228
IO42PB0F3/HCLKBP	229
Bank 1 -	
IO43NB1F4/HCLKCN	220
IO43PB1F4/HCLKCP	221
IO44NB1F4/HCLKDN	216
IO44PB1F4/HCLKDP	217
Bank 1	
IO65NB1F6	210
IO65PB1F6	211
IO69NB1F6	208
IO69PB1F6	209
IO70NB1F6	199
IO71NB1F6	204
IO71PB1F6	205
IO73NB1F6	202
IO73PB1F6	203
IO74NB1F6	197
IO74PB1F6	198
Bank 2	
IO87NB2F8	187

CQ256	
AX2000 Function	Pin Number
IO87PB2F8	188
IO89PB2F8	186
Bank 2	
IO107NB2F10	184
IO107PB2F10	185
IO110NB2F10	180
IO110PB2F10	181
IO111NB2F10	178
IO111PB2F10	179
IO112NB2F10	174
IO112PB2F10	175
IO113NB2F10	172
IO113PB2F10	173
IO114NB2F10	168
IO114PB2F10	169
IO115NB2F10	166
IO115PB2F10	167
IO117NB2F10	162
IO117PB2F10	163
Bank 3	
IO139NB3F13	158
IO139PB3F13	159
IO141NB3F13	154
IO141PB3F13	155
IO142NB3F13	152
IO142PB3F13	153
IO145NB3F13	148
IO145PB3F13	149
IO146NB3F13	146
IO146PB3F13	147
IO147NB3F13	140
IO147PB3F13	141
IO148NB3F13	142
IO148PB3F13	143
IO149NB3F13	136

CQ256	
AX2000 Function	Pin Number
IO149PB3F13	137
Bank 3	
IO165NB3F15	135
IO167NB3F15	133
IO167PB3F15	134
Bank 4	
IO181NB4F17	124
IO181PB4F17	125
IO182NB4F17	122
IO182PB4F17	123
IO183NB4F17	118
IO183PB4F17	119
IO184NB4F17	116
IO184PB4F17	117
IO190NB4F17	112
IO190PB4F17	113
IO192NB4F17	110
IO192PB4F17	111
Bank 4	
IO212NB4F19/CLKEN	104
IO212PB4F19/CLKEP	105
IO213NB4F19/CLKFN	100
IO213PB4F19/CLKFP	101
Bank 5	
IO214NB5F20/CLKGN	92
IO214PB5F20/CLKGP	93
IO215NB5F20/CLKHN	88
IO215PB5F20/CLKHP	89
Bank 5	
IO236NB5F22	82
IO236PB5F22	83
IO238NB5F22	80
IO238PB5F22	81
IO240NB5F22	76
IO240PB5F22	77

CG624	
AX2000 Function	Pin Number
IO229PB5F21	AD10
IO230NB5F21	V11
IO233NB5F21	AD7
IO233PB5F21	AD8
IO234NB5F21	V9
IO234PB5F21	V10
IO236NB5F22	AC9
IO238NB5F22	W8
IO238PB5F22	W9
IO239NB5F22	AE4
IO239PB5F22	AE5
IO240NB5F22	AB9
IO242NB5F22	AA9
IO242PB5F22	Y9
IO243NB5F22	AD5
IO243PB5F22	AD6
IO244NB5F22	U8
IO246NB5F23	AB8
IO246PB5F23	AC8
IO247NB5F23	AB7
IO247PB5F23	AC7
IO250NB5F23	AA8
IO250PB5F23	Y8
IO251NB5F23	V8
IO251PB5F23	V7
IO252NB5F23	Y7
IO252PB5F23	W7
IO253NB5F23	AC5
IO253PB5F23	AC6
IO254NB5F23	Y6
IO254PB5F23	W6
IO256NB5F23	AB6*

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO256PB5F23	AA6*
Bank 6	
IO257NB6F24	Y3
IO257PB6F24	AA3
IO258NB6F24	V3
IO258PB6F24	W3
IO259NB6F24	AA2
IO259PB6F24	AB2
IO260NB6F24	V6*
IO260PB6F24	W4*
IO262NB6F24	U4
IO262PB6F24	V4
IO263NB6F24	Y5
IO263PB6F24	W5
IO268NB6F25	U6
IO268PB6F25	U5
IO269PB6F25	U3
IO272NB6F25	T2
IO272PB6F25	U2
IO273NB6F25	W2
IO273PB6F25	Y2
IO274NB6F25	R6
IO274PB6F25	T6
IO275NB6F25	T7
IO275PB6F25	U7
IO277NB6F25	V2
IO278NB6F26	R4
IO278PB6F26	T4
IO279PB6F26	R3
IO280NB6F26	R5
IO281NB6F26	AA1
IO281PB6F26	AB1

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO284NB6F26	R8
IO284PB6F26	T8
IO285NB6F26	W1
IO285PB6F26	Y1
IO286NB6F26	P2
IO286PB6F26	R2
IO287NB6F26	T1
IO287PB6F26	U1
IO288NB6F26	P5
IO290NB6F27	P6
IO291NB6F27	P1
IO291PB6F27	R1
IO292NB6F27	P7
IO292PB6F27	R7
IO293NB6F27	M1
IO293PB6F27	N1
IO294NB6F27	P8
IO296NB6F27	N3
IO296PB6F27	P3
IO298NB6F27	N4
IO298PB6F27	P4
IO299NB6F27	M2
IO299PB6F27	N2
Bank 7	
IO300NB7F28	P9*
IO300PB7F28	N6*
IO302NB7F28	M6
IO304NB7F28	N8
IO304PB7F28	N7
IO308NB7F28	M4
IO309NB7F28	L3
IO309PB7F28	M3

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.