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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	729-BBGA
Supplier Device Package	729-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1bgg729

I/O Clusters

Each I/O cluster incorporates two I/O modules, four RX modules, two TX modules, and a buffer module. In turn, each I/O module contains one Input Register (InReg), one Output Register (OutReg), and one Enable Register (EnReg) (Figure 2-5).

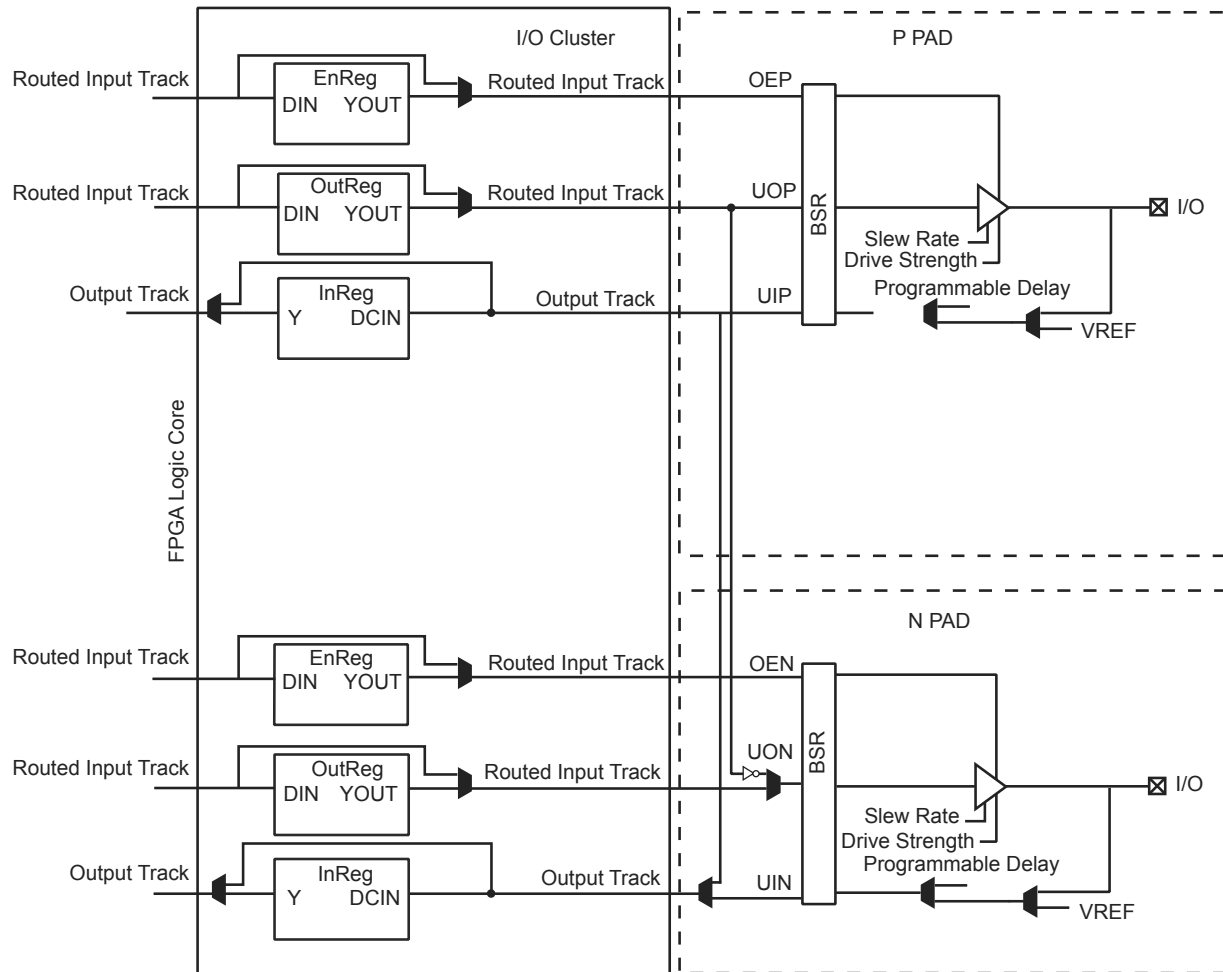


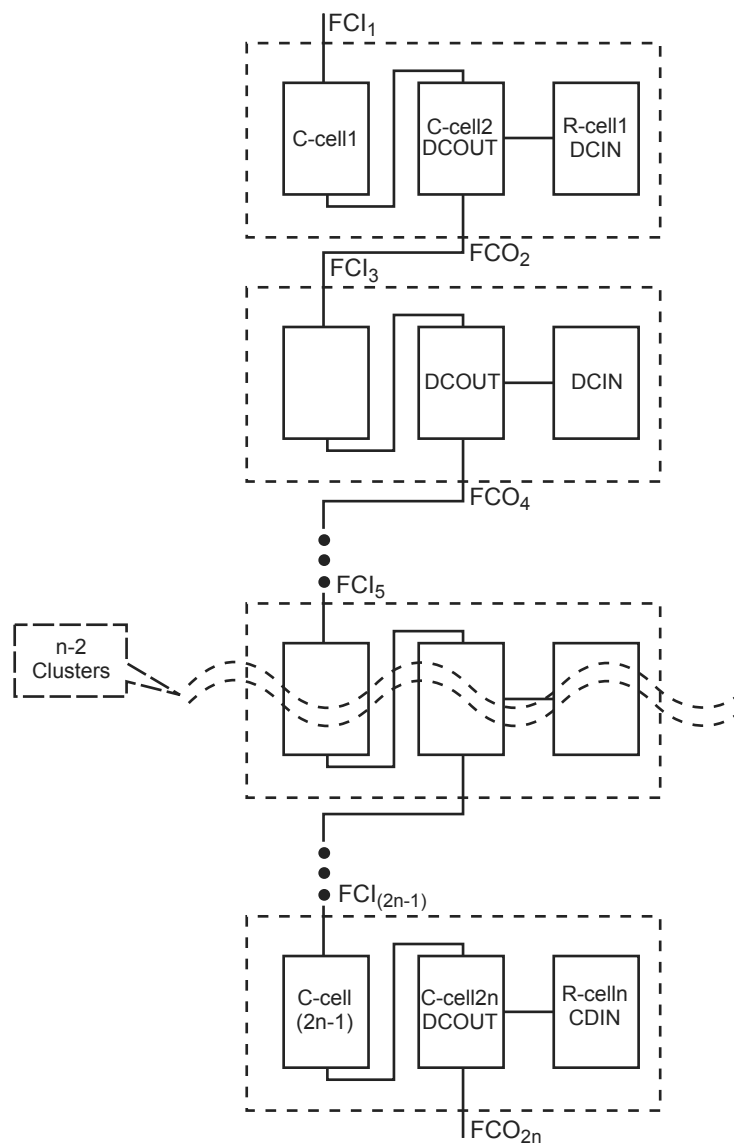
Figure 2-5 • I/O Cluster Interface

Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. Usage of each I/O register (register combining) is individually controlled and can be selected/deselected using the PinEditor tool in the Designer software. I/O register combining can also be controlled at the device level, affecting all I/Os. Please note, the I/O register option is deselected by default in any given design.⁴

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design-specific. The setting for each individual I/O overrides this global option. Furthermore, the *global set fuse* option in the Designer software, when checked, causes all I/O registers to output logic High at device power-up.

4. Please note that register combining for multi fanout nets is not supported.



Note: The carry-chain sequence can end on either C-cell.

Figure 2-30 • Carry-Chain Sequencing of C-Cells

Timing Characteristics

Refer to Table 2-62 on page 2-55 for more information on carry-chain timing.

R-Cell

Introduction

The R-cell, the sequential logic resource of the Axcelerator devices, is the second logic module type in the AX family architecture. It includes clock inputs for all eight global resources of the Axcelerator architecture as well as global presets and clears (Figure 2-31).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-Cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).
- Independent active-low asynchronous clear (CLR).
- Independent active-low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
 - One of the four high performance hardwired fast clocks (HCLKs)
 - One of the four routed clocks (CLKs)
 - User signals
- Global power-on clear (GCLR) and preset (GPSET), which drive each flip-flop on a chip-wide basis.
 - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET = 1 at device power-up. When the option is checked, GCLR = 1 and GPSET = 0. Both pins are pulled High when the device is in user mode. Refer to the "Simulation Support for GCLR/GPSET in Axcelerator" section of the *Antifuse Macro Library Guide* for information on simulation support for GCLR and GPSET.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Microsemi's extensive macro library (see the *Antifuse Macro Library Guide* for a complete listing of available AX macros).

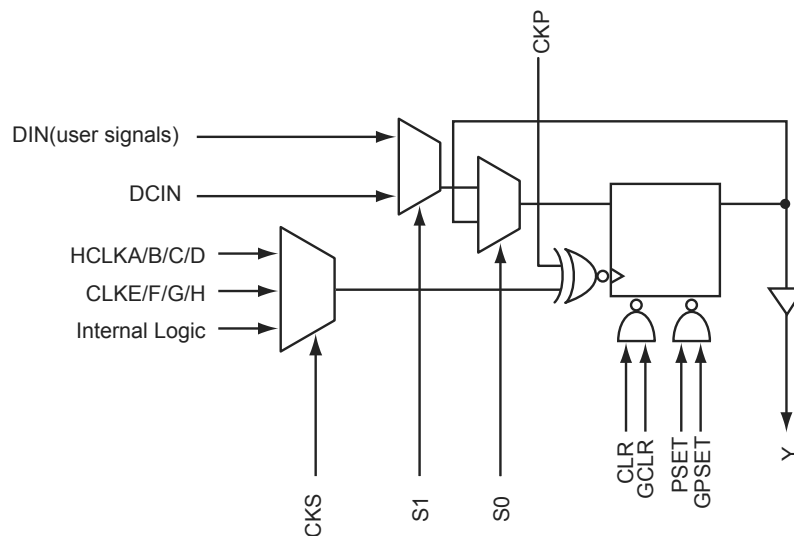


Figure 2-31 • R-Cell

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-37 on page 2-62). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 2-37). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

Figure 2-36 • FastConnect Routing

Figure 2-37 • Horizontal and Vertical Tracks

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-70 • AX125 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-71 • AX250 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t _{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Special PLL Macros

Table 2-84 shows the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

Table 2-84 • PLL Special Macros

Macro Name	Usage
PLLINT	Connects RefCLK to a regular routed net or a pad.
PLLCLK	Connects CLK1 or CLK2 to the CLK network.
PLHCLK	Connects CLK1 or CLK2 to the HCLK network.
PLLOUT	Connects CLK1 or CLK2 to a regular routed net.

Table 2-85 • Electrical Specifications

Parameter	Value	Notes
Frequency Ranges		
Reference Frequency (min.)	14 MHz	Lowest input frequency
Reference Frequency (max.)	200 MHz	Highest input frequency
OSC Frequency (min.)	20 MHz	Lowest output frequency
OSC Frequency (max.)	1 GHz	Highest output frequency
Jitter		
Long-Term Jitter (max.)	1%	Percentage of period, low reference clock frequencies
Long-Term Jitter (max.)	100ps	High reference clock frequencies
Short-Term Jitter (max.)	50ps+1%	Percentage of output frequency
Acquisition Time (lock) from Cold Start		
Acquisition Time (max.)*	400 cycles	Period of low reference clock frequencies
Acquisition Time (max.)*	1.5 μ s	High reference clock frequencies
Power Consumption		
Analog Supply Current (low freq.)	200 μ A	Current at minimum oscillator frequency
Analog Supply Current (high freq.)	200 μ A	Frequency-dependent current
Digital Supply Current (low freq.)	0.5 μ A/MHz	Current at maximum oscillator frequency, unloaded
Digital Supply Current (high freq.)	1 μ A/MHz	Frequency-dependent current
Duty Cycle		
Minimum Output Duty Cycle	45%	
Maximum Output Duty Cycle	55%	

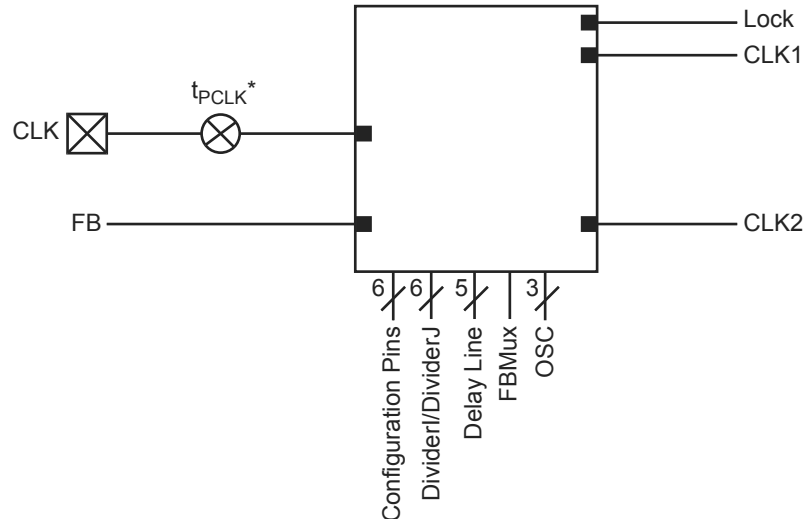
Note: *The lock bit remains Low until RefCLK reaches the minimum input frequency.

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model



Note: t_{PCLK} is the delay in the clock signal

Figure 2-52 • PLL Model

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 6		IO81NB7F7	C2	GND	M12
IO60NB6F6	L4	IO81PB7F7	B1	GND	M5
IO60PB6F6	M4	IO82NB7F7	D2	GND	P13
IO61NB6F6	L3	IO82PB7F7	D3	GND	P3
IO61PB6F6	M3	IO83NB7F7	E3	GND	R15
IO63NB6F6	P2	IO83PB7F7	F3	GND	R2
IO63PB6F6	N2	Dedicated I/O		GND	T1
IO64NB6F6	J4	VCCDA	E4	GND	T16
IO64PB6F6	K4	GND	A1	GND/LP	D4
IO65NB6F6	N1	GND	A16	NC	A11
IO65PB6F6	P1	GND	B15	NC	R11
IO67NB6F6	L2	GND	B2	NC	R5
IO67PB6F6	M2	GND	D15	PRA	D8
IO69NB6F6	L1	GND	E12	PRB	C8
IO69PB6F6	M1	GND	E5	PRC	N9
IO70NB6F6	J3	GND	F11	PRD	P9
IO70PB6F6	K3	GND	F6	TCK	D5
IO71NB6F6	J2	GND	G10	TDI	C6
IO71PB6F6	K2	GND	G7	TDO	C4
Bank 7		GND	G8	TMS	C3
IO72NB7F7	J1	GND	G9	TRST	C5
IO72PB7F7	K1	GND	H10	VCCA	D14
IO73NB7F7	G2	GND	H7	VCCA	F10
IO73PB7F7	H2	GND	H8	VCCA	F4
IO74NB7F7	G3	GND	H9	VCCA	F7
IO74PB7F7	H3	GND	J10	VCCA	F8
IO75NB7F7	E1	GND	J7	VCCA	F9
IO75PB7F7	F1	GND	J8	VCCA	G11
IO76NB7F7	G1	GND	J9	VCCA	G6
IO77NB7F7	E2	GND	K10	VCCA	H11
IO77PB7F7	F2	GND	K7	VCCA	H6
IO78NB7F7	G4	GND	K8	VCCA	J11
IO78PB7F7	H4	GND	K9	VCCA	J6
IO79NB7F7	C1	GND	L11	VCCA	K11
IO79PB7F7	D1	GND	L6	VCCA	K6

FG324	
AX125 Function	Pin Number
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO153PB7F14	M6	GND	A8	GND	L11
IO154NB7F14	K2	GND	AC23	GND	L12
IO154PB7F14	L2	GND	AC4	GND	L13
IO155NB7F14	K3	GND	AD24	GND	L14
IO155PB7F14	L3	GND	AD3	GND	L15
IO156NB7F14	L5	GND	AE2	GND	L16
IO156PB7F14	L4	GND	AE25	GND	L17
IO157NB7F14	L6	GND	AF1	GND	M10
IO157PB7F14	L7	GND	AF13	GND	M11
IO158NB7F15	J1	GND	AF14	GND	M12
IO158PB7F15	K1	GND	AF19	GND	M13
IO159NB7F15	J4	GND	AF26	GND	M14
IO159PB7F15	K4	GND	AF8	GND	M15
IO160NB7F15	H2	GND	B2	GND	M16
IO160PB7F15	J2	GND	B25	GND	M17
IO161NB7F15	K6	GND	B26	GND	N1
IO161PB7F15	K5	GND	C24	GND	N10
IO162NB7F15	H3	GND	C3	GND	N11
IO162PB7F15	J3	GND	G20	GND	N12
IO163NB7F15	G2	GND	G7	GND	N13
IO163PB7F15	G1	GND	H1	GND	N14
IO164NB7F15	G4	GND	H19	GND	N15
IO164PB7F15	H4	GND	H26	GND	N16
IO165NB7F15	F3	GND	H8	GND	N17
IO165PB7F15	G3	GND	J18	GND	N26
IO166NB7F15	E2	GND	J9	GND	P1
IO166PB7F15	F2	GND	K10	GND	P10
IO167NB7F15	F5	GND	K11	GND	P11
IO167PB7F15	G5	GND	K12	GND	P12
Dedicated I/O		GND	K13	GND	P13
GND	A1	GND	K14	GND	P14
GND	A13	GND	K15	GND	P15
GND	A14	GND	K16	GND	P16
GND	A19	GND	K17	GND	P17
GND	A26	GND	L10	GND	P26

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	N1	GND	U19	NC	A26
GND	N13	GND	U20	NC	AB2
GND	N22	GND	U21	NC	AB33
GND	N34	GND	U30	NC	AC34
GND	P14	GND	U5	NC	AD3
GND	P15	GND	V14	NC	AD34
GND	P16	GND	V15	NC	AE31
GND	P17	GND	V16	NC	AE33
GND	P18	GND	V17	NC	AE34
GND	P19	GND	V18	NC	AF1
GND	P20	GND	V19	NC	AF34
GND	P21	GND	V20	NC	AG2
GND	R14	GND	V21	NC	AG4
GND	R15	GND	V30	NC	AH1
GND	R16	GND	V5	NC	AH2
GND	R17	GND	W14	NC	AH31
GND	R18	GND	W15	NC	AH32
GND	R19	GND	W16	NC	AH34
GND	R20	GND	W17	NC	AJ1
GND	R21	GND	W18	NC	AJ2
GND	R3	GND	W19	NC	AJ3
GND	R32	GND	W20	NC	AJ31
GND	T14	GND	W21	NC	AJ32
GND	T15	GND	Y14	NC	AJ33
GND	T16	GND	Y15	NC	AJ34
GND	T17	GND	Y16	NC	AJ4
GND	T18	GND	Y17	NC	AL29
GND	T19	GND	Y18	NC	AM19
GND	T20	GND	Y19	NC	AM7
GND	T21	GND	Y20	NC	AN13
GND	U14	GND	Y21	NC	AN17
GND	U15	GND	Y3	NC	AN25
GND	U16	GND	Y32	NC	AN27
GND	U17	GND/LP	G6	NC	AN8
GND	U18	NC	A17	NC	AP17

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
NC	AP9	PRB	F18	VCCA	T22
NC	B17	PRC	AD18	VCCA	U13
NC	B22	PRD	AH18	VCCA	U22
NC	B27	TCK	J9	VCCA	V13
NC	B8	TDI	F7	VCCA	V22
NC	D10	TDO	L10	VCCA	W13
NC	D20	TMS	H8	VCCA	W22
NC	D23	TRST	E6	VCCA	Y13
NC	D25	VCCA	AA13	VCCA	Y22
NC	F3	VCCA	AA22	VCCDA	AF26
NC	F32	VCCA	AB14	VCCDA	AF9
NC	F33	VCCA	AB15	VCCDA	AG17
NC	F34	VCCA	AB16	VCCDA	AG18
NC	F4	VCCA	AB17	VCCDA	AH14
NC	G1	VCCA	AB18	VCCDA	AH15
NC	G32	VCCA	AB19	VCCDA	AH17
NC	G33	VCCA	AB20	VCCDA	AH20
NC	G34	VCCA	AB21	VCCDA	AH21
NC	H31	VCCA	AF8	VCCDA	AK29
NC	H33	VCCA	AK28	VCCDA	AK6
NC	J1	VCCA	G30	VCCDA	E15
NC	J3	VCCA	G5	VCCDA	E29
NC	J34	VCCA	N14	VCCDA	E7
NC	M1	VCCA	N15	VCCDA	F15
NC	M4	VCCA	N16	VCCDA	F21
NC	P1	VCCA	N17	VCCDA	F5
NC	P2	VCCA	N18	VCCDA	G20
NC	R31	VCCA	N19	VCCDA	H17
NC	T1	VCCA	N20	VCCDA	H18
NC	T2	VCCA	N21	VCCDA	H28
NC	V3	VCCA	P13	VCCDA	J18
NC	V34	VCCA	P22	VCCDA	V27
NC	W3	VCCA	R13	VCCDA	V6
NC	W34	VCCA	R22	VCCIB0	A5
PRA	J17	VCCA	T13	VCCIB0	B5

PQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	Pin Number
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

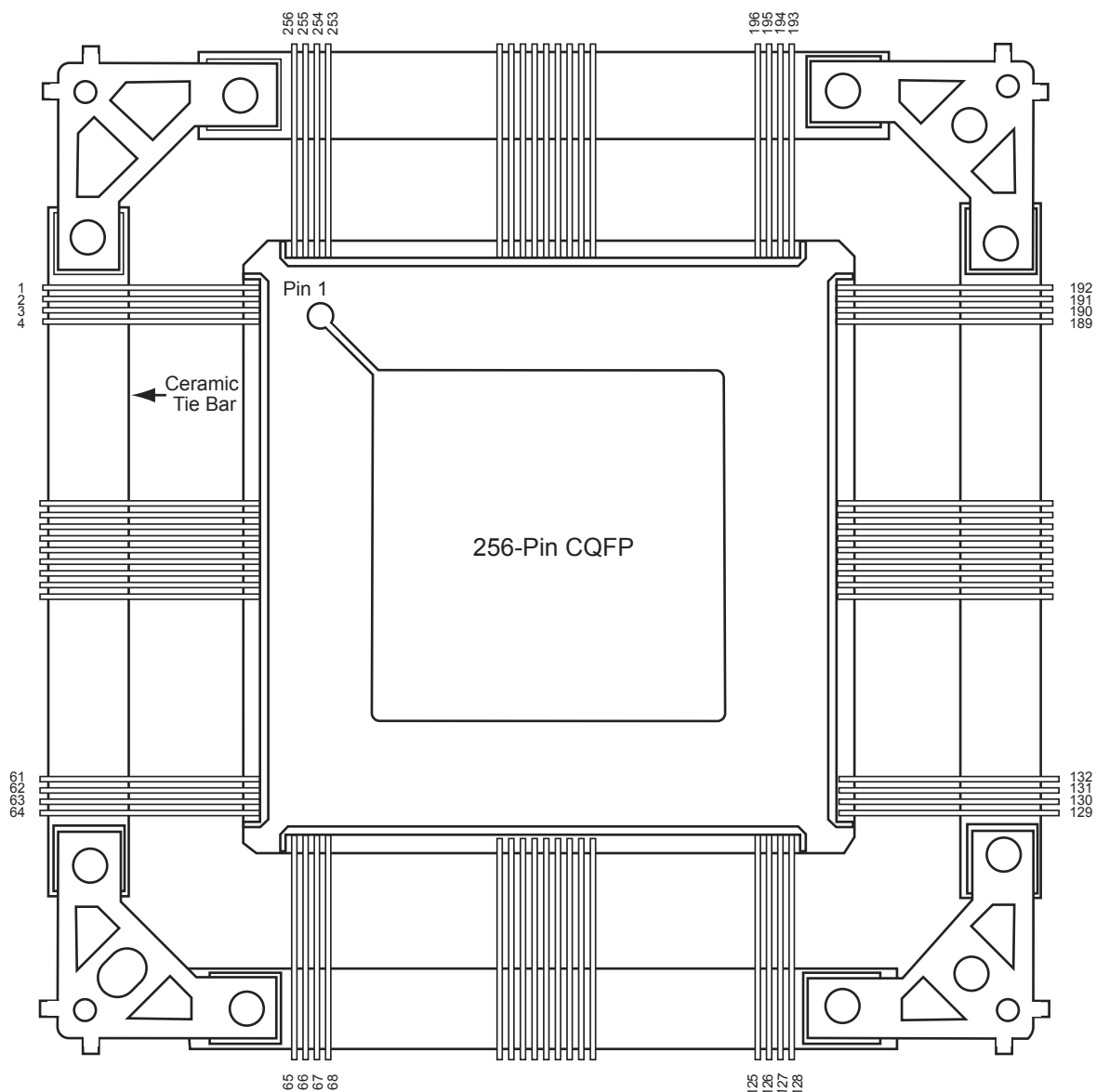
PQ208	
AX250 Function	Pin Number
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

PQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
V _{CCDA}	1
V _{CCDA}	26
V _{CCDA}	53
V _{CCDA}	63
V _{CCDA}	78
V _{CCDA}	95
V _{CCDA}	105
V _{CCDA}	130
V _{CCDA}	157
V _{CCDA}	167
V _{CCDA}	182
V _{CCDA}	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX500 Function	Pin Number
GND	94
GND	99
GND	113
GND	119
GND	125
GND	143
GND	136
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX500 Function	Pin Number
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	200
VCCIB0	193
VCCIB1	172
VCCIB1	163
VCCIB2	149
VCCIB2	135
VCCIB3	124
VCCIB3	112
VCCIB4	98
VCCIB4	89
VCCIB5	68
VCCIB5	58
VCCIB6	45
VCCIB6	31
VCCIB7	20
VCCIB7	8
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ256



Note

For Package Manufacturing and Environmental information, visit the Resource center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO194NB6F18	Y3	IO215PB6F20	V4	IO237NB7F22	N8
IO194PB6F18	AA3	IO216NB6F20	P8	IO237PB7F22	N7
IO195NB6F18	V6	IO216PB6F20	R3	IO238NB7F22	M5
IO195PB6F18	W4	IO217NB6F20	P7	IO239NB7F22	L6
IO197NB6F18	R5	IO217PB6F20	R7	IO239PB7F22	L5
IO197PB6F18	U3	IO219NB6F20	R4	IO240NB7F22	M4
IO198NB6F18	P6	IO219PB6F20	T4	IO241NB7F22	L7
IO199NB6F18	Y5	IO220NB6F20	P2	IO241PB7F22	M7
IO199PB6F18	W5	IO220PB6F20	R2	IO242NB7F22	J3
IO200NB6F18	V3	IO221NB6F20	N4	IO243NB7F22	M9
IO200PB6F18	W3	IO221PB6F20	P4	IO243PB7F22	M8
IO201NB6F18	T7	IO223NB6F20	M2	IO244NB7F22	P9
IO201PB6F18	U7	IO223PB6F20	N2	IO244PB7F22	N6
IO202NB6F18	V2	IO224NB6F20	N3	IO245NB7F22	K8
IO203NB6F19	W2	IO224PB6F20	P3	IO245PB7F22	L8
IO203PB6F19	Y2	Bank 7		IO246NB7F22	F3
IO204NB6F19	AA1	IO225NB7F21	J2	IO246PB7F22	E3
IO204PB6F19	AB1	IO225PB7F21	J1	IO247NB7F23	K7
IO205NB6F19	R6	IO226PB7F21	G2	IO247PB7F23	K6
IO205PB6F19	T6	IO227NB7F21	H3	IO248NB7F23	D2
IO206NB6F19	W1	IO227PB7F21	H2	IO249NB7F23	G4
IO206PB6F19	Y1	IO229NB7F21	K2	IO249PB7F23	G3
IO207NB6F19	T2	IO229PB7F21	L2	IO251NB7F23	N10
IO207PB6F19	U2	IO230NB7F21	K1	IO251PB7F23	N9
IO208NB6F19	T1	IO230PB7F21	L1	IO253NB7F23	H4
IO208PB6F19	U1	IO231NB7F21	E2	IO253PB7F23	J4
IO209NB6F19	AA2	IO231PB7F21	F2	IO255NB7F23	J6
IO209PB6F19	AB2	IO232NB7F21	F1	IO255PB7F23	J5
IO210NB6F19	P5	IO232PB7F21	G1	IO257NB7F23	H5
IO211NB6F19	M1	IO233NB7F21	L3	IO257PB7F23	H6
IO211PB6F19	N1	IO233PB7F21	M3	Dedicated I/O	
IO212NB6F19	P1	IO234NB7F21	D1	GND	K5
IO212PB6F19	R1	IO234PB7F21	E1	GND	A18
IO213NB6F19	R8	IO235NB7F21	K4	GND	A2
IO213PB6F19	T8	IO235PB7F21	L4	GND	A24
IO215NB6F20	U4	IO236NB7F22	M6	GND	A25

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
VCCA	U17	VCCIB2	D23	VCCIB7	E4
VCCA	U9	VCCIB2	E22	VCCIB7	K9
VCCA	Y4	VCCIB2	K17	VCCIB7	L9
VCCDA	A12	VCCIB2	L17	VCCIB7	M10
VCCDA	AA13	VCCIB2	M16	VCCPLA	E12
VCCDA	AA15	VCCIB3	AA22	VCCPLB	J12
VCCDA	AA7	VCCIB3	AB23	VCCPLC	E14
VCCDA	AC11	VCCIB3	AC24	VCCPLD	H14
VCCDA	AD11	VCCIB3	AC25	VCCPLE	Y14
VCCDA	AE17	VCCIB3	P16	VCCPLF	U14
VCCDA	B15	VCCIB3	R17	VCCPLG	Y12
VCCDA	C15	VCCIB3	T17	VCCPLH	U12
VCCDA	C6	VCCIB4	AB21	VCOMPLA	F12
VCCDA	D13	VCCIB4	AC22	VCOMPLB	H12
VCCDA	E13	VCCIB4	AD23	VCOMPLC	F14
VCCDA	E19	VCCIB4	AE23	VCOMPLD	J14
VCCDA	G5	VCCIB4	T14	VCOMPLE	AA14
VCCDA	N21	VCCIB4	U15	VCOMPLF	V14
VCCDA	N5	VCCIB4	U16	VCOMPLG	AA12
VCCDA	W21	VCCIB5	AB5	VCOMPLH	V12
VCCIB0	A3	VCCIB5	AC4	VPUMP	E20
VCCIB0	B3	VCCIB5	AD3		
VCCIB0	C4	VCCIB5	AE3		
VCCIB0	D5	VCCIB5	T12		
VCCIB0	J10	VCCIB5	U10		
VCCIB0	J11	VCCIB5	U11		
VCCIB0	K12	VCCIB6	AA4		
VCCIB1	A23	VCCIB6	AB3		
VCCIB1	B23	VCCIB6	AC1		
VCCIB1	C22	VCCIB6	AC2		
VCCIB1	D21	VCCIB6	P10		
VCCIB1	J15	VCCIB6	R9		
VCCIB1	J16	VCCIB6	T9		
VCCIB1	K14	VCCIB7	C1		
VCCIB2	C24	VCCIB7	C2		
VCCIB2	C25	VCCIB7	D3		

CG624	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	D7*
IO00PB0F0	E7*
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9*
IO13PB0F1	D8*
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11*
IO26PB0F2	B8*

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9

Note: **Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	Pin Number
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

Note: **Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*