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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1fg484i

Table 2-4 • Default CLOAD/VCCI

	C _{LOAD} (pF)	VCCI (V)	PLOAD (mw/MHz)	P10 (mw/MHz)	PI/O (mW/MHz)*
Single-Ended without VREF					
LVTTTL 24 mA High Slew	35	3.3	381.2	267.5	648.7
LVTTTL 16 mA High Slew	35	3.3	381.2	225.1	606.3
LVTTTL 12 mA High Slew	35	3.3	381.2	165.9	547.1
LVTTTL 8 mA High Slew	35	3.3	381.2	130.3	511.5
LVTTTL 24 mA Low Slew	35	3.3	381.2	169.2	550.4
LVTTTL 16 mA Low Slew	35	3.3	381.2	150.8	532.0
LVTTTL 12 mA Low Slew	35	3.3	381.2	138.6	519.8
LVTTTL 8 mA Low Slew	35	3.3	381.2	118.7	499.9
LVC MOS – 25	35	2.5	218.8	148.0	366.8
LVC MOS – 18	35	1.8	113.4	73.4	186.8
LVC MOS – 15 (JESD8-11)	35	1.5	78.8	49.5	128.3
PCI	10	3.3	108.9	218.5	327.4
PCI-X	10	3.3	108.9	162.9	271.8
Single-Ended with VREF					
HSTL-I	20	1.5	–	40.9	40.9
SSTL2-I	30	2.5	–	171.2	171.2
SSTL2-II	30	2.5	–	147.8	147.8
SSTL3-I	30	3.3	–	327.2	327.2
SSTL3-II	30	3.3	–	288.4	288.4
GTLP – 25	10	2.5	–	61.5	61.5
GTLP – 33	10	3.3	–	68.5	68.5
Differential					
LVPECL – 33	N/A	3.3	–	260.6	260.6
LVDS – 25	N/A	2.5	–	145.8	145.8

Note: $*P_{I/O} = P10 + C_{LOAD} * VCC_I^2$

I/O Clusters

Each I/O cluster incorporates two I/O modules, four RX modules, two TX modules, and a buffer module. In turn, each I/O module contains one Input Register (InReg), one Output Register (OutReg), and one Enable Register (EnReg) (Figure 2-5).

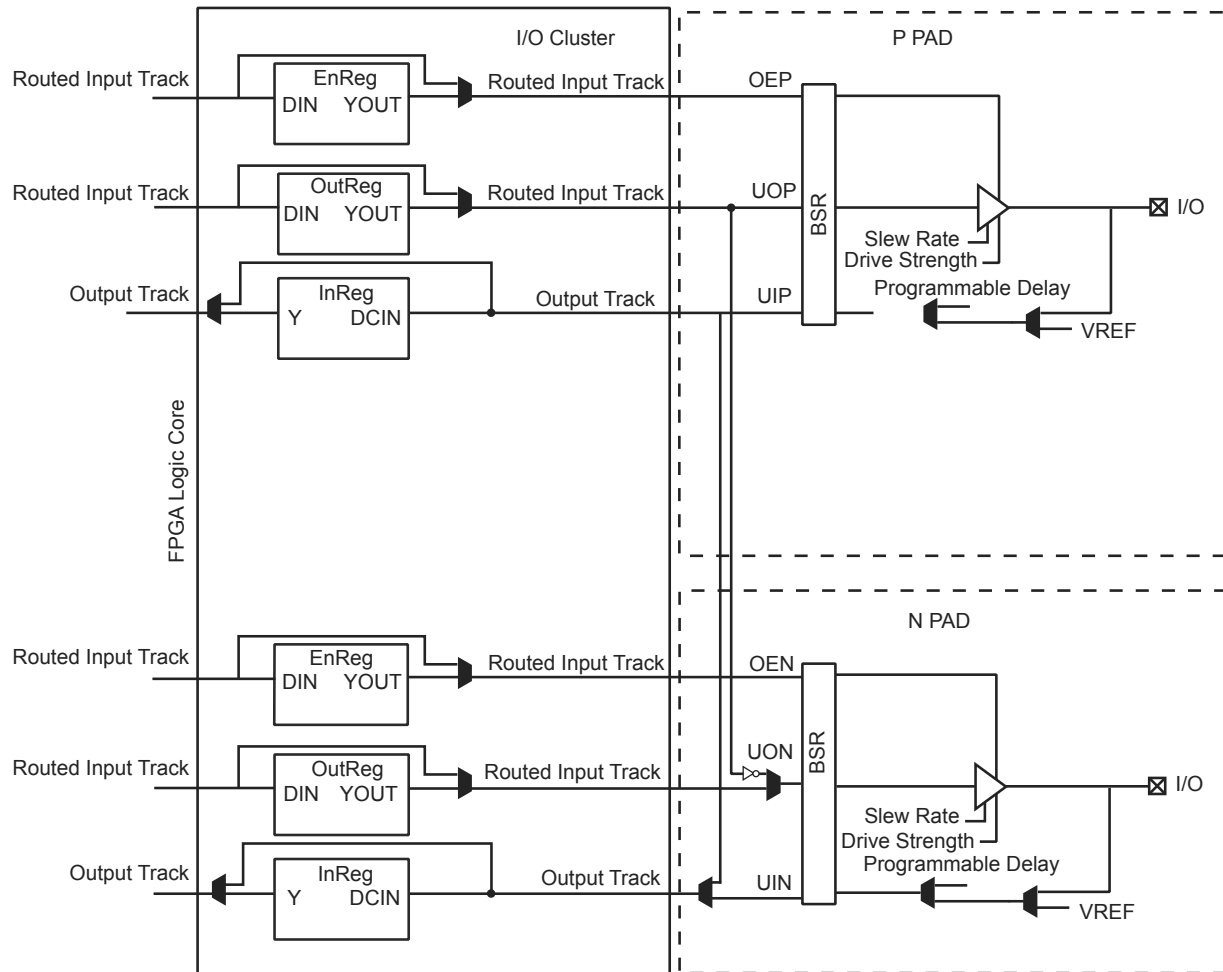


Figure 2-5 • I/O Cluster Interface

Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. Usage of each I/O register (register combining) is individually controlled and can be selected/deselected using the PinEditor tool in the Designer software. I/O register combining can also be controlled at the device level, affecting all I/Os. Please note, the I/O register option is deselected by default in any given design.⁴

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design-specific. The setting for each individual I/O overrides this global option. Furthermore, the *global set fuse* option in the Designer software, when checked, causes all I/O registers to output logic High at device power-up.

4. Please note that register combining for multi fanout nets is not supported.

I/O Standard Electrical Specifications

Table 2-18 • Input Capacitance

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF

Table 2-19 • I/O Input Rise Time and Fall Time*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTTL	No Requirement	50 ns
LVC MOS 2.5V	No Requirement	50 ns
LVC MOS 1.8V	No Requirement	50 ns
LVC MOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

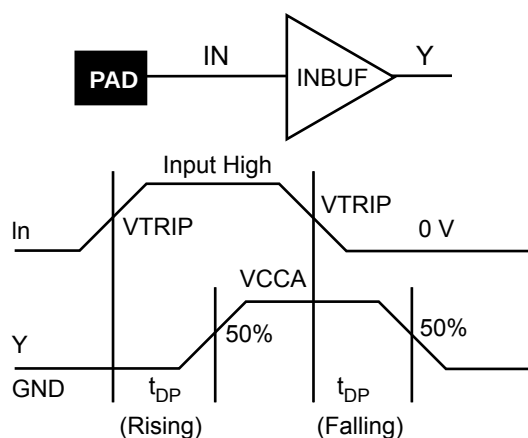


Figure 2-9 • Input Buffer Delays

3.3 V LVTTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-20 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.8	2.0	3.6	0.4	2.4	24	-24

AC Loadings

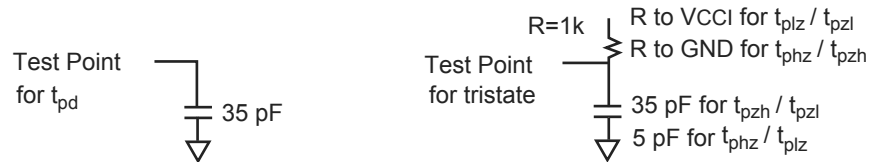


Figure 2-15 • AC Test Loads

Table 2-21 • AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	3.0	1.40	N/A	35

Note: * Measuring Point = VTRIP

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		12.14		13.83		16.26	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

Table 2-41 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCC – 0.4	8	-8

AC Loadings

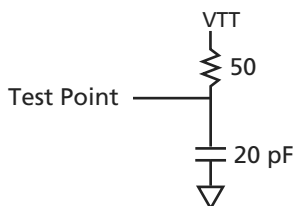


Figure 2-20 • AC Test Loads

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 0.5	VREF + 0.5	VREF	0.75	20

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-43 • 1.5 V HSTL Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.425 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
1.5 V HSTL Class I I/O Module Timing								
t _{DP}	Input Buffer		1.80		2.05		2.41	ns
t _{PY}	Output Buffer		4.90		5.58		6.56	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-80 • PLL Interface Signals

Signal Name	Type	User Accessible	Allowable Values	Function
RefCLK	Input	Yes		Reference Clock for the PLL
FB	Input	Yes		Feedback port for the PLL
PowerDown	Input	Yes		PLL power down control
			0	PLL powered down
			1	PLL active
DIVI[5:0]	Input	Yes	1 to 64, in unsigned binary notation offset by -1	Sets value for feedback divider (multiplier)
DIVJ[5:0]	Input	Yes		Sets value for CLK1 divider
LowFreq	Input	Yes		Input frequency range selector
			0	50–200 MHz
			1	14–50 MHz
Osc[2:0]	Input	Yes		Output frequency range selector
			XX0	400–1000 MHZ
			001	200–400 MHZ
			011	100–200 MHZ
			101	50–100 MHZ
			111	20–50 MHZ
DelayLine[4:0]	Input	Yes	–15 to +15 (increments), in signed-and-magnitude binary representation	Clock Delay (positive/negative) in increments of 250 ps, with maximum value of ± 3.75 ns
FBMuxSel	Input	No		Selects the source for the feedback input
REFSEL	Input	No		Selects the source for the reference clock
OUTSEL	Input	No		Selects the source for the routed net output
PLLSEL	Input	No		ROOTSEL & PLLSEL are used to select the source of the global clock network
ROOTSEL	Input	No		
Lock	Output	Yes		High value indicates PLL has locked
CLK1	Output	Yes		PLL clock output
CLK2	Output	Yes		PLL clock output

Note: If the input RefClk is taken outside its operating range, the outputs Lock, CLK1 and CLK2 are indeterminate.

CLK1 and CLK2

Both PLL outputs, CLK1 and CLK2, can be used to drive a global resource, an adjacent PLL RefCLK input, or a net in the FPGA core. Not all drive combinations are possible (Table 2-81).

Table 2-81 • PLL General Connections Rules

CLK1	CLK2
HCLK	HCLK
CLK	CLK
HCLK	Routed net output
Routed net output	HCLK
HCLK	NONE
NONE	HCLK
CLK	NONE
NONE	CLK

Note: The PLL outputs remain Low when REFCLK is constant (either Low or High).

Restrictions on CLK1 and CLK2

- When both are driving global resources, they must be driving the same type of global resource (i.e. either HCLK or CLK).
- Only one can drive a routed net at any given time.

Table 2-82 and Table 2-83 specify all the possible CLK1 and CLK2 connections for the north and south PLLs. HCLK1 and HCLK2 are used to denote the different HCLK networks when two are being driven at the same time by a single PLL (Note that HCLK1 is the primary clock resource associated with the PLL, and HCLK2 is the clock resource associated with the adjacent PLL). Likewise, CLK1 and CLK2 are used to denote the different CLK networks when two are being driven at the same time by a single PLL (Figure 2-48 on page 2-75).

Table 2-82 • North PLL Connections

CLK1	CLK2
HCLK1	Routed net
HCLK1	Unused
HCLK2	HCLK1
HCLK2	Routed net
HCLK2	Both HCLK1 and routed net
HCLK2	Unused
Unused	HCLK1
Unused	Routed net
Unused	Both HCLK1 and routed net
Unused	Unused
Routed net	HCLK1
Routed net	Unused
Both HCLK1 and HCLK2	Routed net
Both HCLK1 and HCLK2	Unused
Both HCLK1 and routed net	Unusable
Both HCLK2 and routed net	HCLK1
Both HCLK2 and routed net	Unused
HCLK1, HCLK2, and routed net	Unusable

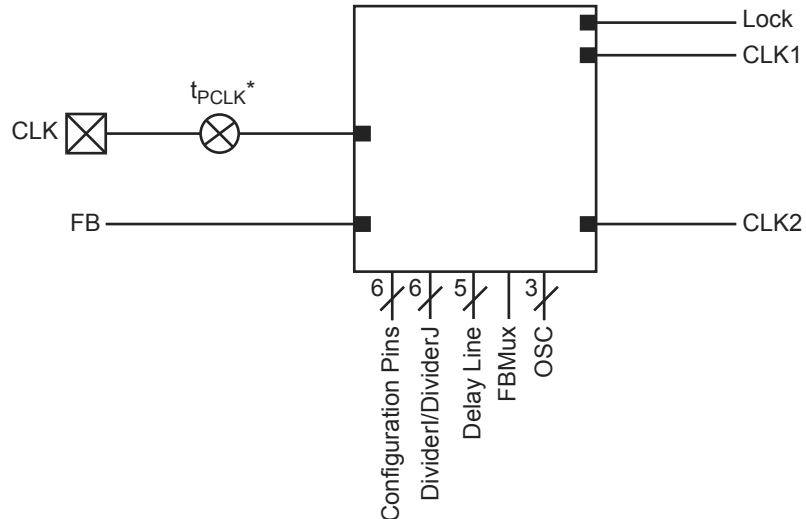
Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g. CLK1 driving HCLK1, and HCLK2 is not supported).

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model



Note: t_{PCLK} is the delay in the clock signal

Figure 2-52 • PLL Model

Table 2-99 • Two FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		13.75		15.66		18.41	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		1.76		1.76		1.76	ns
t _{WCKP}	Minimum WCLK Period	2.51		2.51		2.51		ns
t _{RSU}	Read Setup		14.33		16.32		19.19	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		1.89		1.89		1.89	ns
t _{RCKP}	Minimum RCLK period	2.62		2.62		2.62		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		1.43		1.63		1.92	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		2.26		2.58		3.03	ns

Note: Timing data for these two cascaded FIFO blocks uses a depth of 8,192. For all other combinations, use Microsemi's timing software.

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111". If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:

The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microsemi identity, part number, and version number in a specific JTAG format.

2. USERCODE:

The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.

3. Boundary-Scan Register (BSR):

Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.

4. Bypass Register (BYR):

This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

Special Fuses

Security

Microsemi antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 0		IO20NB2F2	F15	IO41PB3F3	L14
IO01NB0F0	B4	IO20PB2F2	E15	Bank 4	
IO01PB0F0	B3	IO21NB2F2	C16	IO42NB4F4	N12
IO03NB0F0	A4	IO21PB2F2	B16	IO42PB4F4	N13
IO03PB0F0	A3	IO22NB2F2	H13	IO43NB4F4	T14
IO04NB0F0	B6	IO22PB2F2	G13	IO43PB4F4	R14
IO04PB0F0	B5	IO23NB2F2	E16	IO44PB4F4	T15
IO06NB0F0	A6	IO23PB2F2	D16	IO45NB4F4	R12
IO06PB0F0	A5	IO25NB2F2	H15	IO45PB4F4	R13
IO07NB0F0/HCLKAN	B8	IO25PB2F2	G15	IO46NB4F4	P11
IO07PB0F0/HCLKAP	B7	IO26NB2F2	H14	IO46PB4F4	P12
IO08NB0F0/HCLKBN	A9	IO26PB2F2	G14	IO47PB4F4	T11
IO08PB0F0/HCLKBP	A8	IO27NB2F2	G16	IO48NB4F4	T12
Bank 1		IO27PB2F2	F16	IO48PB4F4	T13
IO09NB1F1/HCLKCN	C10	IO28NB2F2	K15	IO49NB4F4/CLKEN	R9
IO09PB1F1/HCLKCP	C9	IO28PB2F2	K16	IO49PB4F4/CLKEP	R10
IO10NB1F1/HCLKDN	B11	IO29NB2F2	J16	IO50NB4F4/CLKFN	T8
IO10PB1F1/HCLKDP	B10	IO29PB2F2	H16	IO50PB4F4/CLKFP	T9
IO12NB1F1	A13	Bank 3		Bank 5	
IO12PB1F1	A12	IO30NB3F3	K13	IO51NB5F5/CLKGN	P7
IO13NB1F1	B13	IO30PB3F3	J13	IO51PB5F5/CLKGP	P8
IO13PB1F1	B12	IO31NB3F3	K14	IO52NB5F5/CLKHN	R6
IO14NB1F1	C12	IO31PB3F3	J14	IO52PB5F5/CLKHP	R7
IO14PB1F1	C11	IO33NB3F3	L15	IO54NB5F5	T5
IO15NB1F1	A15	IO33PB3F3	L16	IO54PB5F5	T6
IO15PB1F1	B14	IO35NB3F3	P16	IO55NB5F5	P5
IO16NB1F1	C15	IO35PB3F3	N16	IO55PB5F5	P6
IO16PB1F1	C14	IO36PB3F3	M16	IO56NB5F5	T3
IO17NB1F1	D13	IO37NB3F3	P15	IO56PB5F5	T4
IO17PB1F1	D12	IO37PB3F3	R16	IO57NB5F5	R3
Bank 2		IO39NB3F3	N15	IO57PB5F5	R4
IO18NB2F2	F13	IO39PB3F3	M15	IO58NB5F5	R1
IO18PB2F2	E13	IO40NB3F3	M13	IO58PB5F5	T2
IO19NB2F2	F14	IO40PB3F3	L13	IO59NB5F5	N4
IO19PB2F2	E14	IO41NB3F3	M14	IO59PB5F5	N5

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
IO52NB3F3	P18	IO69PB4F4	AA17	IO87NB5F5	Y4
IO52PB3F3	P19	IO70NB4F4	AB14	IO87PB5F5	Y5
IO53NB3F3	R20	IO70PB4F4	AB15	IO88NB5F5	V6
IO53PB3F3	P20	IO71NB4F4	Y14	IO88PB5F5	V7
IO54NB3F3	T21	IO71PB4F4	W14	IO89NB5F5	T7
IO54PB3F3	R21	IO72NB4F4	AA14	IO89PB5F5	T8
IO55NB3F3	R17	IO72PB4F4	AA15	Bank 6	
IO55PB3F3	P17	IO73NB4F4	AA13	IO90NB6F6	V4
IO56NB3F3	U20	IO73PB4F4	AB13	IO90PB6F6	W5
IO56PB3F3	T20	IO74NB4F4/CLKEN	V12	IO91NB6F6	P7
IO57NB3F3	T18	IO74PB4F4/CLKEP	V13	IO91PB6F6	R7
IO57PB3F3	R18	IO75NB4F4/CLKFN	W11	IO92NB6F6	U5
IO58NB3F3	U19	IO75PB4F4/CLKFP	W12	IO92PB6F6	T5
IO58PB3F3	T19	Bank 5		IO93NB6F6	P6
IO59NB3F3	R16	IO76NB5F5/CLKGN	U10	IO93PB6F6	R6
IO59PB3F3	P16	IO76PB5F5/CLKGP	U11	IO94NB6F6	T4
IO60NB3F3	W20	IO77NB5F5/CLKHN	V9	IO94PB6F6	U4
IO60PB3F3	V20	IO77PB5F5/CLKHP	V10	IO95NB6F6	P5
IO61NB3F3	U18	IO78NB5F5	AA9	IO95PB6F6	R5
IO61PB3F3	V19	IO78PB5F5	AA10	IO96NB6F6	T3
Bank 4		IO79NB5F5	AB9	IO96PB6F6	U3
IO62NB4F4	T15	IO79PB5F5	AB10	IO97NB6F6	P3
IO62PB4F4	T16	IO80NB5F5	AA7	IO97PB6F6	R3
IO63NB4F4	W17	IO80PB5F5	AA8	IO98NB6F6	R2
IO63PB4F4	V17	IO81NB5F5	W8	IO98PB6F6	T2
IO64NB4F4	V15	IO81PB5F5	W9	IO99NB6F6	P4
IO64PB4F4	V16	IO82NB5F5	AB5	IO99PB6F6	R4
IO65NB4F4	Y19	IO82PB5F5	AB6	IO100NB6F6	P1
IO65PB4F4	W18	IO83NB5F5	AA5	IO100PB6F6	R1
IO66NB4F4	AB18	IO83PB5F5	AA6	IO101NB6F6	M7
IO66PB4F4	AB19	IO84NB5F5	U8	IO101PB6F6	N7
IO67NB4F4	W15	IO84PB5F5	U9	IO102NB6F6	N2
IO67PB4F4	W16	IO85NB5F5	Y6	IO102PB6F6	P2
IO68NB4F4	U14	IO85PB5F5	Y7	IO103NB6F6	M6
IO68PB4F4	U15	IO86NB5F5	W6	IO103PB6F6	N6
IO69NB4F4	AA16	IO86PB5F5	W7	IO104NB6F6	M4

FG484	
AX1000 Function	Pin Number
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	AB16
VCCDA	AB8
VCCDA	C10
VCCDA	C11
VCCDA	C14
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX1000 Function	Pin Number
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX1000 Function	Pin Number
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG676	
AX1000 Function	Pin Number
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26
IO73PB2F6	D26
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23

FG676	
AX1000 Function	Pin Number
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
Bank 3	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24
IO100NB3F9	R22
IO100PB3F9	P22
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25

FG676	
AX1000 Function	Pin Number
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
Bank 4	
IO129NB4F12	AB21

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG896	
AX1000 Function	Pin Number
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

FG896	
AX1000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX1000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO259NB6F24	AF7	IO276PB6F25	AD2	IO294NB6F27	V10
IO259PB6F24	AG7	IO277NB6F25	AC4	IO294PB6F27	V11
IO260NB6F24	AH3	IO277PB6F25	AC3	IO295NB6F27	Y1
IO260PB6F24	AH4	IO278NB6F26	AA8	IO295PB6F27	Y2
IO261NB6F24	AH5	IO278PB6F26	AA9	IO296NB6F27	W1
IO261PB6F24	AJ5	IO279NB6F26	AB5	IO296PB6F27	W2
IO262NB6F24	AE6	IO279PB6F26	AB6	IO297NB6F27	V1
IO262PB6F24	AF6	IO280NB6F26	Y10	IO297PB6F27	V2
IO263NB6F24	AF5	IO280PB6F26	Y11	IO298NB6F27	V9
IO263PB6F24	AG5	IO281NB6F26	AB3	IO298PB6F27	V8
IO264NB6F24	AD8	IO281PB6F26	AB4	IO299NB6F27	U4
IO264PB6F24	AE8	IO282NB6F26	Y7	IO299PB6F27	V4
IO265NB6F24	AF3	IO282PB6F26	AA7	Bank 7	
IO265PB6F24	AG3	IO283NB6F26	AC2	IO300NB7F28	U10
IO266NB6F24	AC10	IO283PB6F26	AC1	IO300PB7F28	U11
IO266PB6F24	AD10	IO284NB6F26	Y9	IO301NB7F28	U2
IO267NB6F25	AD7	IO284PB6F26	Y8	IO301PB7F28	U1
IO267PB6F25	AE7	IO285NB6F26	AA5	IO302NB7F28	U6
IO268NB6F25	AD5	IO285PB6F26	AA6	IO302PB7F28	U7
IO268PB6F25	AE5	IO286NB6F26	W10	IO303NB7F28	T3
IO269NB6F25	AE4	IO286PB6F26	W11	IO303PB7F28	U3
IO269PB6F25	AF4	IO287NB6F26	AA3	IO304NB7F28	U9
IO270NB6F25	AB9	IO287PB6F26	AA4	IO304PB7F28	U8
IO270PB6F25	AC9	IO288NB6F26	W9	IO305NB7F28	R2
IO271NB6F25	AC6	IO288PB6F26	W8	IO305PB7F28	R1
IO271PB6F25	AD6	IO289NB6F27	AA1	IO306NB7F28	R4
IO272NB6F25	AB8	IO289PB6F27	AA2	IO306PB7F28	T4
IO272PB6F25	AC8	IO290NB6F27	W6	IO307NB7F28	R5
IO273NB6F25	AE1	IO290PB6F27	Y6	IO307PB7F28	T5
IO273PB6F25	AE2	IO291NB6F27	W5	IO308NB7F28	T11
IO274NB6F25	AA10	IO291PB6F27	Y5	IO308PB7F28	T10
IO274PB6F25	AB10	IO292NB6F27	V7	IO309NB7F28	T6
IO275NB6F25	AB7	IO292PB6F27	W7	IO309PB7F28	T7
IO275PB6F25	AC7	IO293NB6F27	W4	IO310NB7F29	T9
IO276NB6F25	AD1	IO293PB6F27	Y4	IO310PB7F29	T8

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO131NB4F12	V19	IO153NB4F14	Y15	IO173PB5F16	Y11
IO131PB4F12	W19	IO153PB4F14	Y16	IO174NB5F16	AB10
IO133NB4F12	Y18	IO155NB4F14	V15	IO174PB5F16	AB11
IO133PB4F12	Y19	IO155PB4F14	V16	IO175NB5F16	AC9
IO135NB4F12	W18	IO156NB4F14	AB14	IO175PB5F16	AE9
IO135PB4F12	V18	IO156PB4F14	AB15	IO177NB5F16	AA8
IO137NB4F12	Y17	IO157NB4F14	AE14	IO177PB5F16	Y8
IO137PB4F12	AA17	IO157PB4F14	AC18	IO178NB5F16	Y6
IO138NB4F12	AB19	IO158NB4F14	AC15	IO178PB5F16	W6
IO138PB4F12	AB18	IO158PB4F14	AC19	IO179NB5F16	Y10
IO139NB4F13	AA19	IO159NB4F14/CLKEN	W14	IO179PB5F16	W10
IO139PB4F13	U18	IO159PB4F14/CLKEP	W15	IO180NB5F16	Y7
IO140NB4F13	AC20	IO160NB4F14/CLKFN	AC13	IO180PB5F16	W7
IO140PB4F13	AC21	IO160PB4F14/CLKFP	AD13	IO181NB5F17	AD9
IO141NB4F13	AD17	Bank 5		IO181PB5F17	AD10
IO141PB4F13	AD18	IO161NB5F15/CLKGN	W13	IO182NB5F17	AE10
IO142NB4F13	AD21	IO161PB5F15/CLKGP	Y13	IO182PB5F17	AE11
IO142PB4F13	AD22	IO162NB5F15/CLKHN	AC12	IO183NB5F17	AD7
IO143NB4F13	AB17	IO162PB5F15/CLKHP	AD12	IO183PB5F17	AD8
IO143PB4F13	AC17	IO163NB5F15	V9	IO184NB5F17	AB9
IO144PB4F13	AE22	IO163PB5F15	V10	IO185NB5F17	AE6
IO145NB4F13	AE15	IO164NB5F15	V11	IO185PB5F17	AE7
IO145PB4F13	AE16	IO164PB5F15	T13	IO186NB5F17	AE4
IO146NB4F13	AD19	IO165NB5F15	U13	IO186PB5F17	AE5
IO146PB4F13	AD20	IO165PB5F15	V13	IO187NB5F17	AA9
IO147NB4F13	AD15	IO167NB5F15	W11	IO187PB5F17	Y9
IO147PB4F13	AD16	IO167PB5F15	W12	IO188NB5F17	U8
IO148PB4F13	AE21	IO168NB5F15	AB6	IO189NB5F17	AD5
IO149NB4F13	AD14	IO168PB5F15	AA6	IO189PB5F17	AD6
IO149PB4F13	AC14	IO169NB5F15	V8	IO191NB5F17	AC5
IO150NB4F13	AE19	IO169PB5F15	V7	IO191PB5F17	AC6
IO150PB4F13	AE20	IO171NB5F16	W8	IO192NB5F17	AB7
IO151NB4F13	V17	IO171PB5F16	W9	IO192PB5F17	AC7
IO151PB4F13	W17	IO172NB5F16	AB8	Bank 6	
IO152NB4F14	AB16	IO172PB5F16	AC8	IO193NB6F18	U6
IO152PB4F14	W16	IO173NB5F16	AA11	IO193PB6F18	U5



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