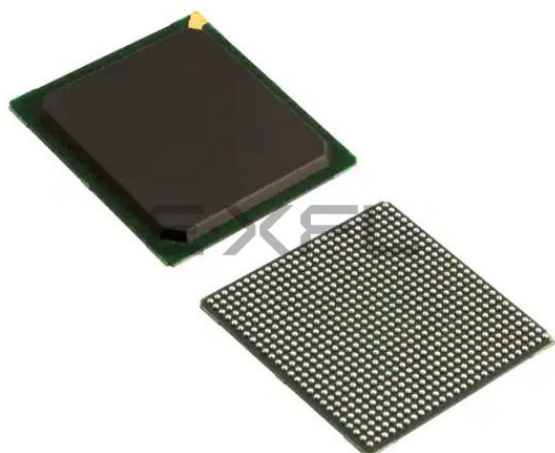




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	418
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1fg676

Packaging Data

Refer to the following documents located on the Microsemi SoC Products Group website for additional packaging information.

- Package Mechanical Drawings

- Package Thermal Characteristics and Weights

- Hermetic Package Mechanical Information

Contact your local Microsemi representative for device availability.

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Table 2-4 • Default CLOAD/VCCI

	C _{LOAD} (pF)	VCCI (V)	PLOAD (mw/MHz)	P10 (mw/MHz)	PI/O (mW/MHz)*
Single-Ended without VREF					
LVTTTL 24 mA High Slew	35	3.3	381.2	267.5	648.7
LVTTTL 16 mA High Slew	35	3.3	381.2	225.1	606.3
LVTTTL 12 mA High Slew	35	3.3	381.2	165.9	547.1
LVTTTL 8 mA High Slew	35	3.3	381.2	130.3	511.5
LVTTTL 24 mA Low Slew	35	3.3	381.2	169.2	550.4
LVTTTL 16 mA Low Slew	35	3.3	381.2	150.8	532.0
LVTTTL 12 mA Low Slew	35	3.3	381.2	138.6	519.8
LVTTTL 8 mA Low Slew	35	3.3	381.2	118.7	499.9
LVC MOS – 25	35	2.5	218.8	148.0	366.8
LVC MOS – 18	35	1.8	113.4	73.4	186.8
LVC MOS – 15 (JESD8-11)	35	1.5	78.8	49.5	128.3
PCI	10	3.3	108.9	218.5	327.4
PCI-X	10	3.3	108.9	162.9	271.8
Single-Ended with VREF					
HSTL-I	20	1.5	–	40.9	40.9
SSTL2-I	30	2.5	–	171.2	171.2
SSTL2-II	30	2.5	–	147.8	147.8
SSTL3-I	30	3.3	–	327.2	327.2
SSTL3-II	30	3.3	–	288.4	288.4
GTLP – 25	10	2.5	–	61.5	61.5
GTLP – 33	10	3.3	–	68.5	68.5
Differential					
LVPECL – 33	N/A	3.3	–	260.6	260.6
LVDS – 25	N/A	2.5	–	145.8	145.8

Note: $*P_{I/O} = P10 + C_{LOAD} * VCC_I^2$

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

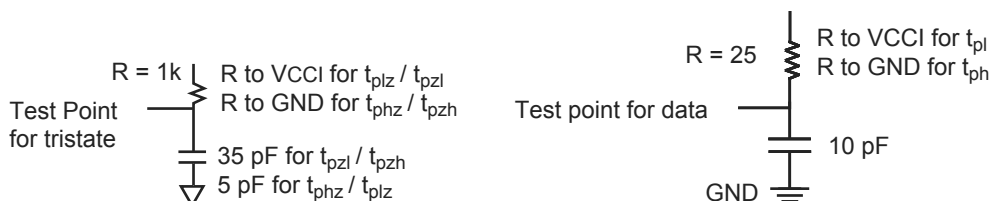


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

Class II

Table 2-53 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16

AC Loadings

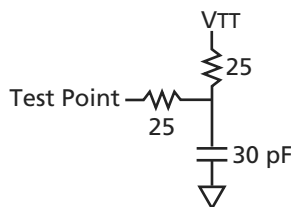


Figure 2-24 • AC Test Loads

Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-55 • 3.3 V SSTL3 Class II I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V SSTL3 Class II I/O Module Timing								
t _{DP}	Input Buffer		1.85		2.10		2.47	ns
t _{PY}	Output Buffer		2.17		2.47		2.91	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Models and Waveforms

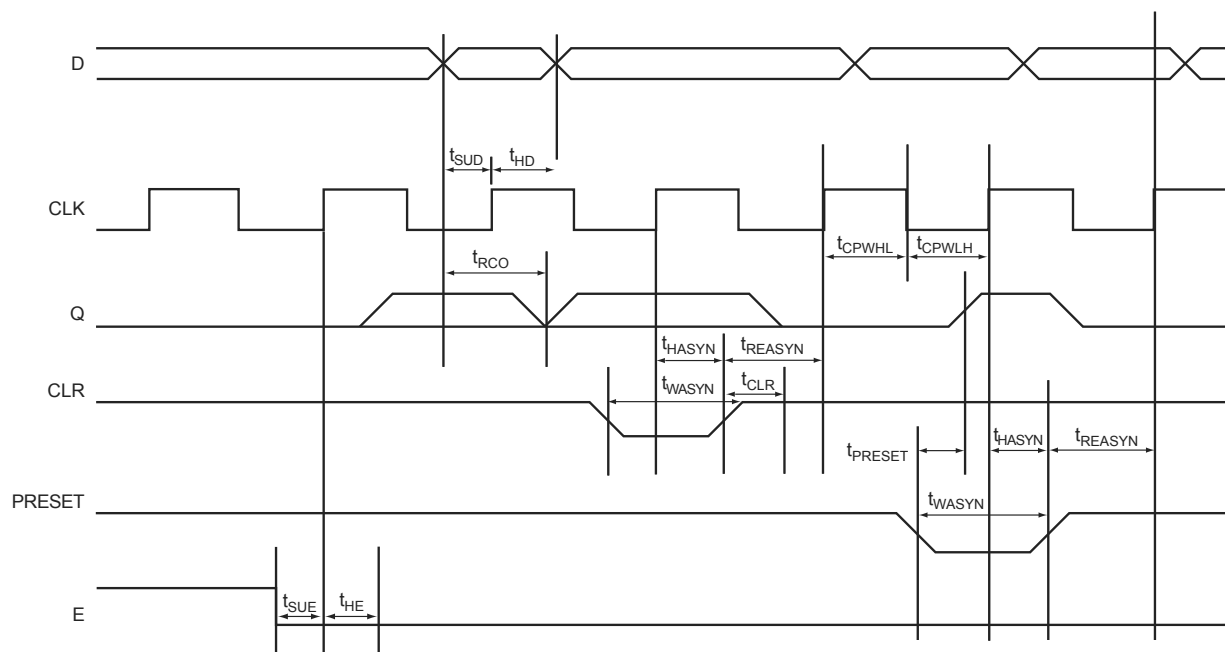


Figure 2-32 • R-Cell Delays

Timing Characteristics

Table 2-63 • R-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
R-Cell Propagation Delays								
t _{RCO}	Sequential Clock-to-Q		0.67		0.77		0.90	ns
t _{CLR}	Asynchronous Clear-to-Q		0.67		0.77		0.90	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.36		0.36		0.36	ns
t _{SUD}	Flip-Flop Data Input Set-Up		0.34		0.34		0.34	ns
t _{SUE}	Flip-Flop Enable Input Set-Up		0.00		0.00		0.00	ns
t _{HD}	Flip-Flop Data Input Hold		0.67		0.77		0.90	ns
t _{HE}	Flip-Flop Enable Input Hold		0.67		0.77		0.90	ns
t _{WASYN}	Asynchronous Pulse Width	0.48		0.48		0.48		ns
t _{REASYN}	Asynchronous Recovery Time		0.23		0.27		0.31	ns
t _{HASYN}	Asynchronous Removal Time		0.36		0.36		0.36	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.36		0.36		0.36		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.36		0.36		0.36		ns

Table 2-69 • AX2000 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.50	0.56	0.66	ns
t _{RD2}	Routing delay for FO2	0.59	0.67	0.79	ns
t _{RD3}	Routing delay for FO3	0.70	0.80	0.94	ns
t _{RD4}	Routing delay for FO4	0.76	0.87	1.02	ns
t _{RD5}	Routing delay for FO5	0.98	1.11	1.31	ns
t _{RD6}	Routing delay for FO6	1.48	1.68	1.97	ns
t _{RD7}	Routing delay for FO7	1.65	1.87	2.20	ns
t _{RD8}	Routing delay for FO8	1.73	1.96	2.31	ns
t _{RD16}	Routing delay for FO16	2.58	2.92	3.44	ns
t _{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Axcelerator Clock Management System

Introduction

Each member of the Axcelerator family⁶ contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20μs

Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 μF and 10 μF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

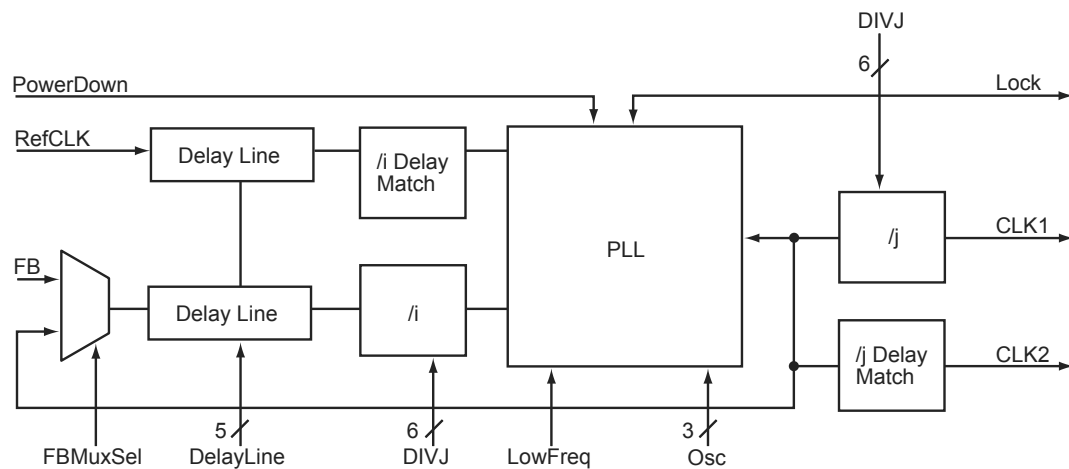


Figure 2-48 • PLL Block Diagram

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

6. AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.

Table 2-80 • PLL Interface Signals

Signal Name	Type	User Accessible	Allowable Values	Function
RefCLK	Input	Yes		Reference Clock for the PLL
FB	Input	Yes		Feedback port for the PLL
PowerDown	Input	Yes		PLL power down control
			0	PLL powered down
			1	PLL active
DIVI[5:0]	Input	Yes	1 to 64, in unsigned binary notation offset by -1	Sets value for feedback divider (multiplier)
DIVJ[5:0]	Input	Yes		Sets value for CLK1 divider
LowFreq	Input	Yes		Input frequency range selector
			0	50–200 MHz
			1	14–50 MHz
Osc[2:0]	Input	Yes		Output frequency range selector
			XX0	400–1000 MHZ
			001	200–400 MHZ
			011	100–200 MHZ
			101	50–100 MHZ
			111	20–50 MHZ
DelayLine[4:0]	Input	Yes	–15 to +15 (increments), in signed-and-magnitude binary representation	Clock Delay (positive/negative) in increments of 250 ps, with maximum value of ± 3.75 ns
FBMuxSel	Input	No		Selects the source for the feedback input
REFSEL	Input	No		Selects the source for the reference clock
OUTSEL	Input	No		Selects the source for the routed net output
PLLSEL	Input	No		ROOTSEL & PLLSEL are used to select the source of the global clock network
ROOTSEL	Input	No		
Lock	Output	Yes		High value indicates PLL has locked
CLK1	Output	Yes		PLL clock output
CLK2	Output	Yes		PLL clock output

Note: If the input RefClk is taken outside its operating range, the outputs Lock, CLK1 and CLK2 are indeterminate.

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-86). Each block has independent read and write ports which enable simultaneous read and write operations.

Table 2-86 • Memory Block WxD Options

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in Table 2-87.

Table 2-87 • Allowable RW and WW Values

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

mode if desired. Please note, if the I/O bank is not disabled, differential I/Os belonging to the I/O bank will still consume normal power, even when operating in the low power mode.

The Axcelerator device will resume normal operation 10 μ s after the LP pin is pulled Low.

To further reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e. high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

In addition, any PLL in use can be powered down to further reduce power consumption. This can be done with the PowerDown pin driven Low. Driving this pin High restarts the PLL with the output clock(s) being stable once lock is restored.

JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the Table 2-103.

Table 2-103 • JTAG Instruction Code

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload / Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
Reserved	All others
Bypass	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low, asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1 k Ω resistor.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a VCCA and/or VCCDA voltage drop.

throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is protected with highest level of security in the industry.



Figure 2-69 • FuseLock Logo

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to the *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (Figure 2-31 on page 2-58). Default setting is to clear all registers (GCLR = 0 and GPSET = 1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET = 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-108).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-7). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

FG676	
AX500 Function	Pin Number
IO51NB2F4	L20
IO51PB2F4	L21
IO52NB2F5	K26
IO52PB2F5	J26
IO53NB2F5	L23
IO53PB2F5	L22
IO54NB2F5	L24
IO54PB2F5	K24
IO55NB2F5	M20
IO55PB2F5	M21
IO56NB2F5	L26
IO56PB2F5	L25
IO57NB2F5	M23
IO57PB2F5	M22
IO58NB2F5	M26
IO58PB2F5	M25
IO59NB2F5	N22
IO59PB2F5	N23
IO60NB2F5	N24
IO60PB2F5	M24
IO61NB2F5	N20
IO61PB2F5	N21
IO62NB2F5	P25
IO62PB2F5	N25
Bank 3	
IO63NB3F6	T26
IO63PB3F6	R26
IO64NB3F6	R24
IO64PB3F6	P24
IO65NB3F6	P20
IO65PB3F6	P21
IO66NB3F6	T25
IO66PB3F6	R25
IO67NB3F6	T23
IO67PB3F6	R23

FG676	
AX500 Function	Pin Number
IO68NB3F6	V26
IO68PB3F6	U26
IO69NB3F6	V25
IO69PB3F6	U25
IO70NB3F6	Y25
IO70PB3F6	W25
IO71NB3F6	W24
IO71PB3F6	V24
IO72NB3F6	V23
IO72PB3F6	U23
IO73NB3F6	T21
IO73PB3F6	T20
IO74NB3F7	AA26
IO74PB3F7	Y26
IO75NB3F7	AA24
IO75PB3F7	Y24
IO76NB3F7	Y23
IO76PB3F7	W23
IO77NB3F7	V21
IO77PB3F7	U21
IO78NB3F7	AB25
IO78PB3F7	AA25
IO79NB3F7	AC26
IO79PB3F7	AB26
IO80NB3F7	AC24
IO80PB3F7	AB24
IO81NB3F7	AB23
IO81PB3F7	AA23
IO82NB3F7	AA22
IO82PB3F7	Y22
IO83NB3F7	AE26
IO83PB3F7	AD26
Bank 4	
IO84NB4F8	AB21
IO84PB4F8	AA21

FG676	
AX500 Function	Pin Number
IO85NB4F8	AE23
IO85PB4F8	AE24
IO86NB4F8	AC21
IO86PB4F8	AC22
IO87NB4F8	AF22
IO87PB4F8	AF23
IO88NB4F8	AD22
IO88PB4F8	AD23
IO89NB4F8	AC19
IO89PB4F8	AC20
IO90NB4F8	AE21
IO90PB4F8	AE22
IO91NB4F8	AA17
IO91PB4F8	AA18
IO92NB4F8	AD20
IO92PB4F8	AD21
IO93NB4F8	AF20
IO93PB4F8	AF21
IO94NB4F9	AE19
IO94PB4F9	AE20
IO95NB4F9	AC17
IO95PB4F9	AC18
IO96NB4F9	AD18
IO96PB4F9	AD19
IO97NB4F9	AA16
IO97PB4F9	Y16
IO98NB4F9	AE17
IO98PB4F9	AE18
IO99NB4F9	AC16
IO99PB4F9	AB16
IO100NB4F9	AF17
IO100PB4F9	AF18
IO101NB4F9	AA15
IO101PB4F9	Y15
IO102NB4F9	AC15

FG676	
AX1000 Function	Pin Number
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11

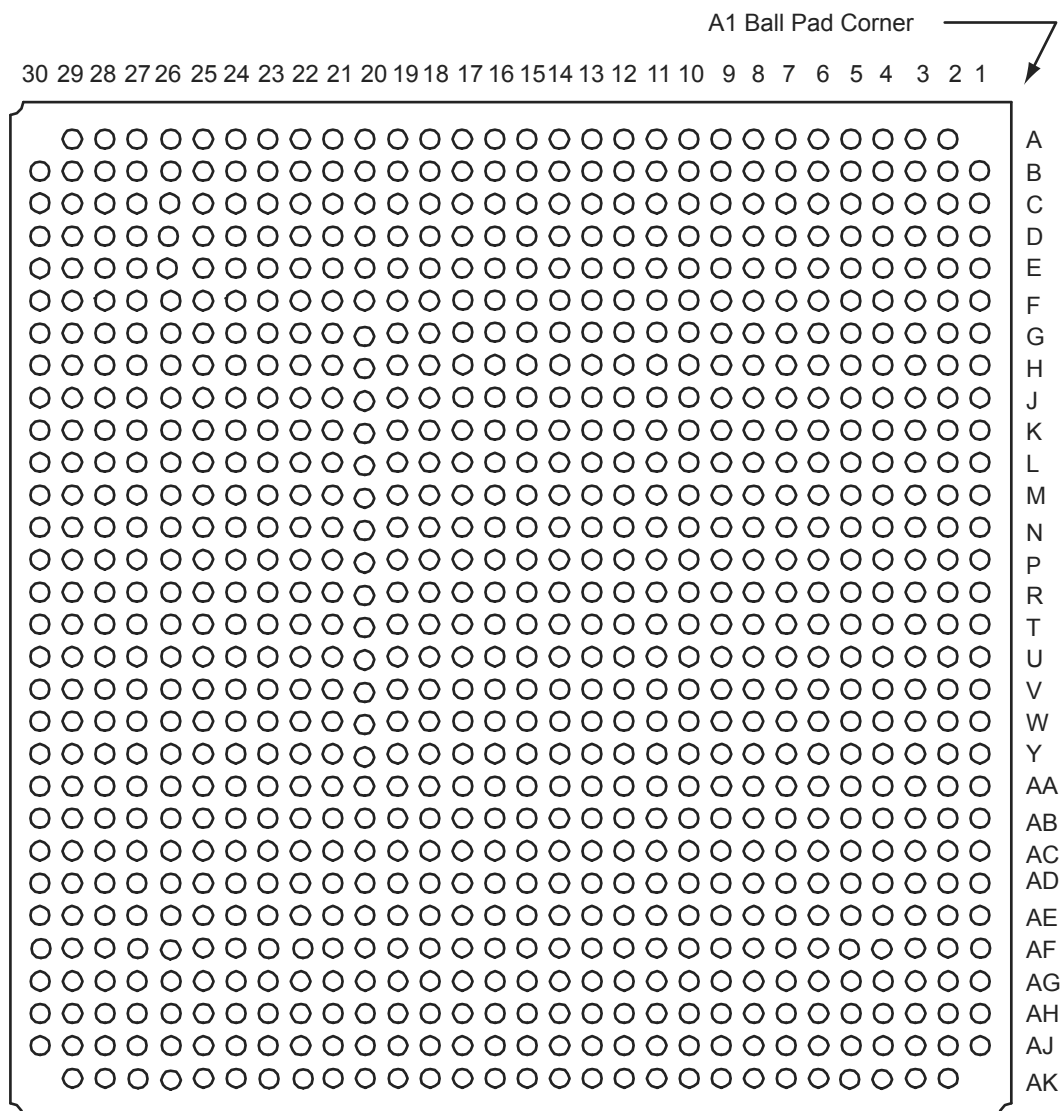
FG676	
AX1000 Function	Pin Number
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11

FG676	
AX1000 Function	Pin Number
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ256		CQ256	
AX2000 Function	Pin Number	AX2000 Function	Pin Number
VCCA	4	VCCDA	224
VCCA	22	VCCDA	236
VCCA	42	VCCDA	237
VCCA	61	VCCDA	251
VCCA	63	VCCIB0	230
VCCA	84	VCCIB0	244
VCCA	108	VCCIB1	200
VCCA	127	VCCIB1	206
VCCA	131	VCCIB1	218
VCCA	150	VCCIB2	164
VCCA	170	VCCIB2	176
VCCA	189	VCCIB2	182
VCCA	191	VCCIB3	138
VCCA	212	VCCIB3	144
VCCA	238	VCCIB3	156
VCCDA	2	VCCIB4	102
VCCDA	32	VCCIB4	114
VCCDA	66	VCCIB4	120
VCCDA	67	VCCIB5	72
VCCDA	86	VCCIB5	78
VCCDA	87	VCCIB5	90
VCCDA	94	VCCIB6	36
VCCDA	95	VCCIB6	48
VCCDA	96	VCCIB6	54
VCCDA	106	VCCIB7	10
VCCDA	107	VCCIB7	16
VCCDA	126	VCCIB7	28
VCCDA	130	VPUMP	195
VCCDA	160		
VCCDA	194		
VCCDA	196		
VCCDA	214		
VCCDA	215		
VCCDA	222		
VCCDA	223		

CQ352	
AX2000 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX2000 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO194NB6F18	Y3	IO215PB6F20	V4	IO237NB7F22	N8
IO194PB6F18	AA3	IO216NB6F20	P8	IO237PB7F22	N7
IO195NB6F18	V6	IO216PB6F20	R3	IO238NB7F22	M5
IO195PB6F18	W4	IO217NB6F20	P7	IO239NB7F22	L6
IO197NB6F18	R5	IO217PB6F20	R7	IO239PB7F22	L5
IO197PB6F18	U3	IO219NB6F20	R4	IO240NB7F22	M4
IO198NB6F18	P6	IO219PB6F20	T4	IO241NB7F22	L7
IO199NB6F18	Y5	IO220NB6F20	P2	IO241PB7F22	M7
IO199PB6F18	W5	IO220PB6F20	R2	IO242NB7F22	J3
IO200NB6F18	V3	IO221NB6F20	N4	IO243NB7F22	M9
IO200PB6F18	W3	IO221PB6F20	P4	IO243PB7F22	M8
IO201NB6F18	T7	IO223NB6F20	M2	IO244NB7F22	P9
IO201PB6F18	U7	IO223PB6F20	N2	IO244PB7F22	N6
IO202NB6F18	V2	IO224NB6F20	N3	IO245NB7F22	K8
IO203NB6F19	W2	IO224PB6F20	P3	IO245PB7F22	L8
IO203PB6F19	Y2	Bank 7		IO246NB7F22	F3
IO204NB6F19	AA1	IO225NB7F21	J2	IO246PB7F22	E3
IO204PB6F19	AB1	IO225PB7F21	J1	IO247NB7F23	K7
IO205NB6F19	R6	IO226PB7F21	G2	IO247PB7F23	K6
IO205PB6F19	T6	IO227NB7F21	H3	IO248NB7F23	D2
IO206NB6F19	W1	IO227PB7F21	H2	IO249NB7F23	G4
IO206PB6F19	Y1	IO229NB7F21	K2	IO249PB7F23	G3
IO207NB6F19	T2	IO229PB7F21	L2	IO251NB7F23	N10
IO207PB6F19	U2	IO230NB7F21	K1	IO251PB7F23	N9
IO208NB6F19	T1	IO230PB7F21	L1	IO253NB7F23	H4
IO208PB6F19	U1	IO231NB7F21	E2	IO253PB7F23	J4
IO209NB6F19	AA2	IO231PB7F21	F2	IO255NB7F23	J6
IO209PB6F19	AB2	IO232NB7F21	F1	IO255PB7F23	J5
IO210NB6F19	P5	IO232PB7F21	G1	IO257NB7F23	H5
IO211NB6F19	M1	IO233NB7F21	L3	IO257PB7F23	H6
IO211PB6F19	N1	IO233PB7F21	M3	Dedicated I/O	
IO212NB6F19	P1	IO234NB7F21	D1	GND	K5
IO212PB6F19	R1	IO234PB7F21	E1	GND	A18
IO213NB6F19	R8	IO235NB7F21	K4	GND	A2
IO213PB6F19	T8	IO235PB7F21	L4	GND	A24
IO215NB6F20	U4	IO236NB7F22	M6	GND	A25