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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1fgg484

I/O Specifications

Pin Descriptions

Supply Pins

GND **Ground**

Low supply voltage.

VCCA **Supply Voltage**

Supply voltage for array (1.5V). See "Operating Conditions" on page 2-1 for more information.

VCCIBx **Supply Voltage**

Supply voltage for I/Os. Bx is the I/O Bank ID – 0 to 7. See "Operating Conditions" on page 2-1 for more information.

VCCDA **Supply Voltage**

Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. See "Operating Conditions" on page 2-1 for more information. VCCDA should be tied to 3.3V.

VCCPLA/B/C/D/E/F/G/H **Supply Voltage**

PLL analog power supply (1.5V) for internal PLL. There are eight in each device. VCCPLA supports the PLL associated with global resource HCLKA, VCCPLB supports the PLL associated with global resource HCLKB, etc. The PLL analog power supply pins should be connected to 1.5V whether PLL is used or not.

VCOMPLA/B/C/D/E/F/G/H **Supply Voltage**

Compensation reference signals for internal PLL. There are eight in each device. **VCOMPLA** supports the PLL associated with global resource HCLKA, VCOMPLE supports the PLL associated with global resource CLKE, etc. (see Figure 2-2 on page 2-9 for correct external connection to the supply). The VCOMPLX pins should be left floating if PLL is not used.

VPUMP **Supply Voltage (External Pump)**

In the low power mode, VPUMP will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on VPUMP reaches VIH[1]. In normal device operation, when using the internal charge pump, VPUMP should be tied to GND.

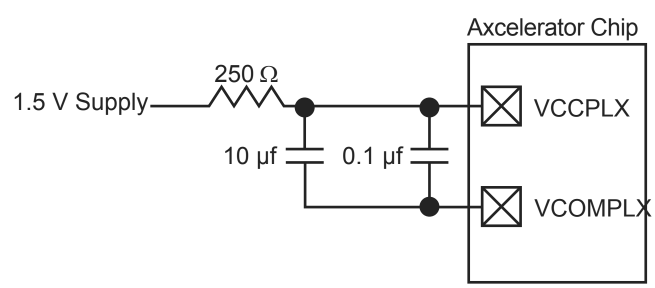


Figure 2-2 • **VCCPLX and VCOMPLX Power Supply Connect**

1. *When $V_{PUMP} = V_{IH}$, it shuts off the internal charge pump. See **"Low Power Mode" on page 2-106**.*

Table 2-8 • I/O Standards Supported by the Axcelerator Family

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVCMOS 2.5 V	2.5	N/A	N/A
LVCMOS 1.8 V	1.8	N/A	N/A
LVCMOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

*Note: *2.5 V GTL+ is not supported across the full military temperature range.*

Table 2-9 • Supply Voltages

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5 V	1.5 V	3.3 V	1.5 V
1.5 V	1.8 V	3.3 V	1.8 V
1.5 V	2.5 V	3.3 V	2.5 V
1.5 V	3.3 V	3.3 V	3.3 V

Table 2-10 • I/O Features Comparison

I/O Assignment	Clamp Diode	Hot Insertion	5 V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1, 2]	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled[3]
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled[4]

Notes:

1. *Can be implemented with an IDT bus switch.*
2. *Can be implemented with an external resistor.*
3. *The OE input of the output buffer must be deasserted permanently (handled by software).*
4. *The OE input of the output buffer must be asserted permanently (handled by software).*

5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

EQ 3

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

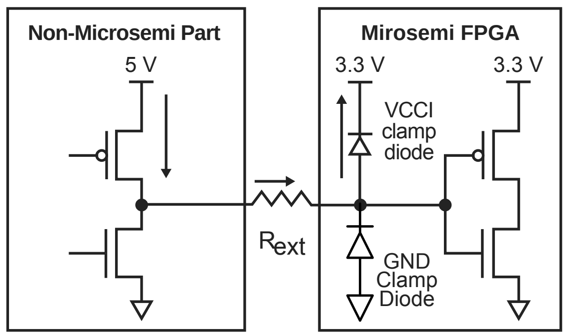


Figure 2-3 • **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

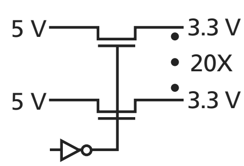


Figure 2-4 • **Bus Switch IDTQS32X2384**

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

3. *The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.*

Timing Characteristics

Table 2-22 • 3.3 V LVTTL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 1 (8 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		14.28		16.27		19.13	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		15.25		17.37		20.42	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		14.26		16.24		19.09	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.56		1.57		1.58	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		1.95		1.96		1.97	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		039		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-61 • LVPECL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVPECL Output Module Timing								
t_{DP}	Input Buffer		1.66		1.89		2.22	ns
t_{PY}	Output Buffer		2.24		2.55		3.00	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-67 • AX500 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-68 • AX1000 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.45	0.51	0.60	ns
t_{RD2}	Routing delay for FO2	0.53	0.60	0.71	ns
t_{RD3}	Routing delay for FO3	0.56	0.63	0.74	ns
t_{RD4}	Routing delay for FO4	0.63	0.71	0.84	ns
t_{RD5}	Routing delay for FO5	0.73	0.82	0.97	ns
t_{RD6}	Routing delay for FO6	0.99	1.13	1.32	ns
t_{RD7}	Routing delay for FO7	1.02	1.15	1.36	ns
t_{RD8}	Routing delay for FO8	1.48	1.68	1.97	ns
t_{RD16}	Routing delay for FO16	2.57	2.91	3.42	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

***Table 2-75* • AX125 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-76* • AX250 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t_{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-38).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-39).

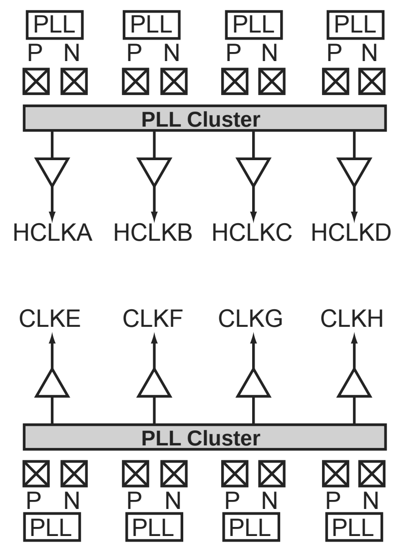


Figure 2-38 **• PLL Group**

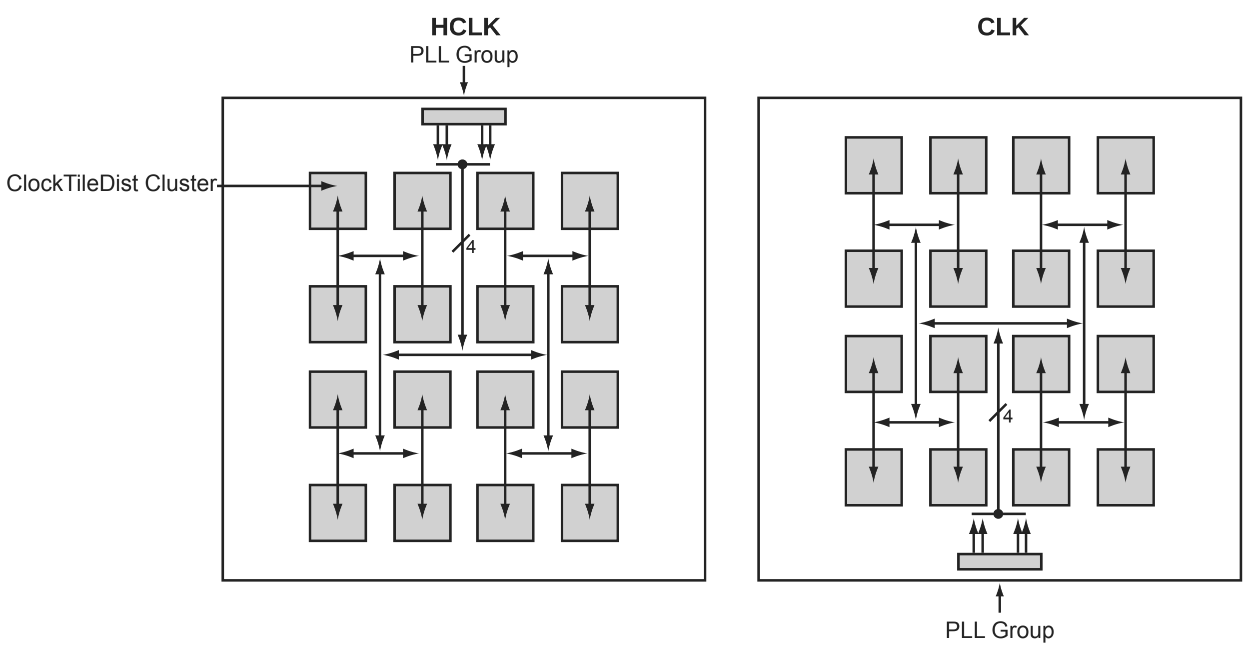


Figure 2-39 **• Example of HCLK and CLK Distributions on the AX2000**

Table 2-80 • PLL Interface Signals

Signal Name	Type	User Accessible	Allowable Values	Function
RefCLK	Input	Yes		Reference Clock for the PLL
FB	Input	Yes		Feedback port for the PLL
PowerDown	Input	Yes		PLL power down control
			0	PLL powered down
			1	PLL active
DIVI[5:0]	Input	Yes	1 to 64, in unsigned binary notation offset by -1	Sets value for feedback divider (multiplier)
DIVJ[5:0]	Input	Yes		Sets value for CLK1 divider
LowFreq	Input	Yes		Input frequency range selector
			0	50–200 MHz
			1	14–50 MHz
Osc[2:0]	Input	Yes		Output frequency range selector
			XX0	400–1000 MHZ
			001	200–400 MHZ
			011	100–200 MHZ
			101	50–100 MHZ
			111	20–50 MHZ
DelayLine[4:0]	Input	Yes	–15 to +15 (increments), in signed-and-magnitude binary representation	Clock Delay (positive/negative) in increments of 250 ps, with maximum value of ± 3.75 ns
FBMuxSel	Input	No		Selects the source for the feedback input
REFSEL	Input	No		Selects the source for the reference clock
OUTSEL	Input	No		Selects the source for the routed net output
PLLSEL	Input	No		ROOTSEL & PLLSEL are used to select the source of the global clock network
ROOTSEL	Input	No		
Lock	Output	Yes		High value indicates PLL has locked
CLK1	Output	Yes		PLL clock output
CLK2	Output	Yes		PLL clock output

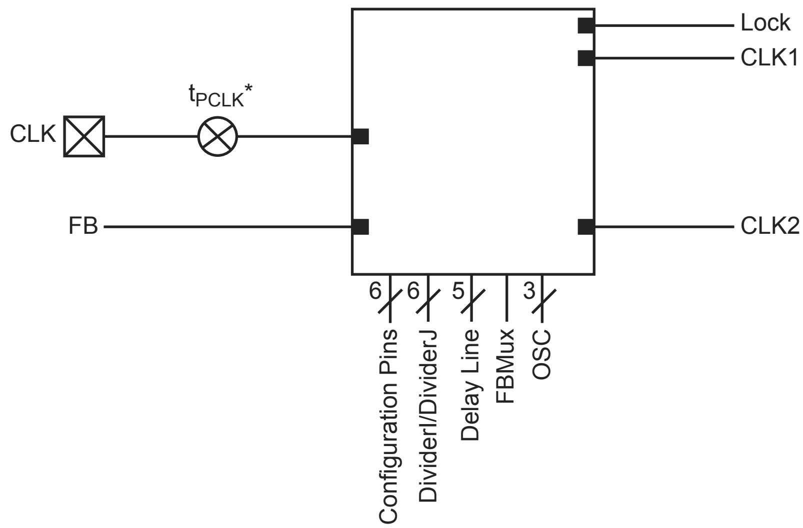
Note: *If the input RefClk is taken outside its operating range, the outputs Lock, CLK1 and CLK2 are indeterminate.*

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model



Note: t_{PCLK} is the delay in the clock signal

Figure 2-52 • **PLL Model**

Table 2-89 • One RAM Block
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		1.08		1.23		1.45	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.22		0.25		0.30	ns
t_{WADSU}	Write Address Setup vs. WCLK		1.08		1.23		1.45	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		1.08		1.23		1.45	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.22		0.25		0.30	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	0.88		0.88		0.88		ns
t_{WCKP}	WCLK Minimum Period	1.63		1.63		1.63		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		0.81		0.92		1.08	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		0.81		0.92		1.08	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)		1.32		1.51		1.77	ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)		2.16		2.46		2.90	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.77		0.77		0.77		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	0.93		0.93		0.93		ns
t_{RCKP}	RCLK Minimum Period	1.70		1.70		1.70		ns

Note: Timing data for this single block RAM has a depth of 4,096. For all other combinations, use Microsemi's timing software.

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111". If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:

   The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microsemi identity, part number, and version number in a specific JTAG format.

2. USERCODE:

   The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.

3. Boundary-Scan Register (BSR):

   Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.

4. Bypass Register (BYR):

   This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

Special Fuses

Security

Microsemi antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden

FG256-Pin FBGA	
AX125 Function	Pin Number
Bank 6	
IO60NB6F6	L4
IO60PB6F6	M4
IO61NB6F6	L3
IO61PB6F6	M3
IO63NB6F6	P2
IO63PB6F6	N2
IO64NB6F6	J4
IO64PB6F6	K4
IO65NB6F6	N1
IO65PB6F6	P1
IO67NB6F6	L2
IO67PB6F6	M2
IO69NB6F6	L1
IO69PB6F6	M1
IO70NB6F6	J3
IO70PB6F6	K3
IO71NB6F6	J2
IO71PB6F6	K2
Bank 7	
IO72NB7F7	J1
IO72PB7F7	K1
IO73NB7F7	G2
IO73PB7F7	H2
IO74NB7F7	G3
IO74PB7F7	H3
IO75NB7F7	E1
IO75PB7F7	F1
IO76NB7F7	G1
IO77NB7F7	E2
IO77PB7F7	F2
IO78NB7F7	G4
IO78PB7F7	H4
IO79NB7F7	C1
IO79PB7F7	D1

FG256-Pin FBGA	
AX125 Function	Pin Number
IO81NB7F7	C2
IO81PB7F7	B1
IO82NB7F7	D2
IO82PB7F7	D3
IO83NB7F7	E3
IO83PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6

FG256-Pin FBGA	
AX125 Function	Pin Number
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
NC	A11
NC	R11
NC	R5
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6

FG484	
AX1000 Function	Pin Number
IO246NB7F22	F3
IO246PB7F22	G3
IO250NB7F23	F4
IO250PB7F23	G4
IO253NB7F23	G5
IO253PB7F23	G6
IO254NB7F23	D1
IO254PB7F23	E1
IO257NB7F23	F5
IO257PB7F23	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX1000 Function	Pin Number
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX1000 Function	Pin Number
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17

FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9

FG676	
AX500 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21

FG676	
AX500 Function	Pin Number
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

FG1152	
AX2000 Function	Pin Number
IO103PB2F9	M28
IO104NB2F9	M34
IO104PB2F9	L34
IO105NB2F9	P27
IO105PB2F9	N27
IO106NB2F9	M32
IO106PB2F9	M31
IO107NB2F10	P25
IO107PB2F10	P26
IO108NB2F10	N33
IO108PB2F10	M33
IO109NB2F10	P29
IO109PB2F10	N29
IO110NB2F10	P30
IO110PB2F10	N30
IO111NB2F10	R24
IO111PB2F10	R25
IO112NB2F10	P31
IO112PB2F10	N31
IO113NB2F10	R28
IO113PB2F10	P28
IO114NB2F10	P32
IO114PB2F10	N32
IO115NB2F10	R30
IO115PB2F10	R29
IO116NB2F10	P34
IO116PB2F10	P33
IO117NB2F10	R27
IO117PB2F10	R26
IO118NB2F11	R34
IO118PB2F11	R33
IO119NB2F11	T24
IO119PB2F11	T25
IO120NB2F11	T33
IO120PB2F11	T34

FG1152	
AX2000 Function	Pin Number
IO121NB2F11	T27
IO121PB2F11	T26
IO122NB2F11	T30
IO122PB2F11	T29
IO123NB2F11	U28
IO123PB2F11	T28
IO124NB2F11	T31
IO124PB2F11	T32
IO125NB2F11	U24
IO125PB2F11	U25
IO126NB2F11	U33
IO126PB2F11	U34
IO127NB2F11	U26
IO127PB2F11	U27
IO128NB2F11	U31
IO128PB2F11	U32
Bank 3	
IO129NB3F12	V29
IO129PB3F12	U29
IO130NB3F12	V31
IO130PB3F12	V32
IO131NB3F12	V24
IO131PB3F12	V25
IO132NB3F12	W28
IO132PB3F12	V28
IO133NB3F12	W26
IO133PB3F12	V26
IO134NB3F12	W33
IO134PB3F12	V33
IO135NB3F12	W25
IO135PB3F12	W24
IO136NB3F12	W31
IO136PB3F12	W32
IO137NB3F12	Y30
IO137PB3F12	W30

FG1152	
AX2000 Function	Pin Number
IO138NB3F12	Y29
IO138PB3F12	W29
IO139NB3F13	Y27
IO139PB3F13	W27
IO140NB3F13	AA33
IO140PB3F13	Y33
IO141NB3F13	Y25
IO141PB3F13	Y24
IO142NB3F13	AA31
IO142PB3F13	Y31
IO143NB3F13	AA28
IO143PB3F13	Y28
IO144NB3F13	AA34
IO144PB3F13	Y34
IO145NB3F13	AA26
IO145PB3F13	Y26
IO146NB3F13	AA29
IO146PB3F13	AA30
IO147NB3F13	AB30
IO147PB3F13	AB29
IO148NB3F13	AB32
IO148PB3F13	AA32
IO149NB3F13	AB27
IO149PB3F13	AA27
IO150NB3F14	AC31
IO150PB3F14	AB31
IO151NB3F14	AD33
IO151PB3F14	AC33
IO152NB3F14	AC28
IO152PB3F14	AB28
IO153NB3F14	AB25
IO153PB3F14	AA25
IO154NB3F14	AD32
IO154PB3F14	AC32
IO155NB3F14	AD29

CQ256	
AX2000 Function	Pin Number
VCCA	4
VCCA	22
VCCA	42
VCCA	61
VCCA	63
VCCA	84
VCCA	108
VCCA	127
VCCA	131
VCCA	150
VCCA	170
VCCA	189
VCCA	191
VCCA	212
VCCA	238
VCCDA	2
VCCDA	32
VCCDA	66
VCCDA	67
VCCDA	86
VCCDA	87
VCCDA	94
VCCDA	95
VCCDA	96
VCCDA	106
VCCDA	107
VCCDA	126
VCCDA	130
VCCDA	160
VCCDA	194
VCCDA	196
VCCDA	214
VCCDA	215
VCCDA	222
VCCDA	223

CQ256	
AX2000 Function	Pin Number
VCCDA	224
VCCDA	236
VCCDA	237
VCCDA	251
VCCIB0	230
VCCIB0	244
VCCIB1	200
VCCIB1	206
VCCIB1	218
VCCIB2	164
VCCIB2	176
VCCIB2	182
VCCIB3	138
VCCIB3	144
VCCIB3	156
VCCIB4	102
VCCIB4	114
VCCIB4	120
VCCIB5	72
VCCIB5	78
VCCIB5	90
VCCIB6	36
VCCIB6	48
VCCIB6	54
VCCIB7	10
VCCIB7	16
VCCIB7	28
VPUMP	195

CQ352	
AX250 Function	**Pin Number**
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282

CQ352	
AX250 Function	**Pin Number**
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224

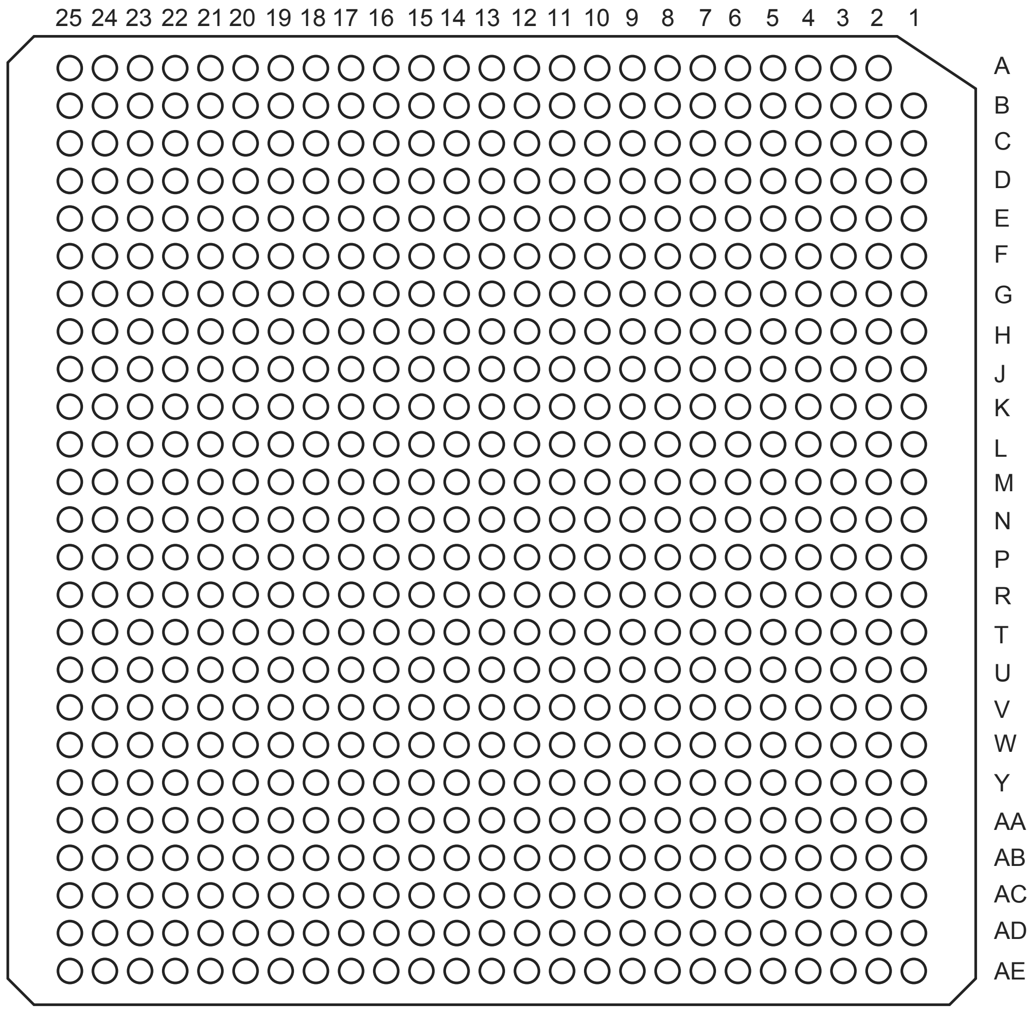
CQ352	
AX250 Function	**Pin Number**
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

CQ352	
AX500 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX500 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND/LP	352
NC	91
NC	117
NC	130
NC	131
NC	148
NC	174
NC	268
NC	294
NC	307
NC	308
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349

CQ352	
AX500 Function	Pin Number
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	132
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	309

CG624



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.