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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax1000-1fgg896

Axcelerator Family Device Status

Axcelerator® Devices	Status
AX125	Production
AX250	Production
AX500	Production
AX1000	Production
AX2000	Production

Temperature Grade Offerings

Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	C, I, M	C, I, M	–	–
CQ208	–	M	M	–	–
CQ256	–	–	–	–	M
FG256	C, I	C, I, M	–	–	–
FG324	C, I	–	–	–	–
CQ352	–	M	M	M	M
FG484	–	C, I, M	C, I, M	C, I, M	–
CG624	–	–	–	M	M
FG676	–	–	C, I, M	C, I, M	–
BG729	–	–	–	C, I, M	–
FG896	–	–	–	C, I, M	C, I, M
FG1152	–	–	–	–	C, I, M

C = Commercial

I = Industrial

M = Military

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std	–1	–2
C	✓	✓	✓
I	✓	✓	✓
M	✓	✓	–

C = Commercial

I = Industrial

M = Military

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

The maximum power dissipation allowed for Military temperature and Mil-Std 883B devices is specified as a function of θ_{jc}.

Table 2-6 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0m/s	θ_{ja} 2.5m/s	Units
Chip Scale Package (CSP)	180	N/A	57.8	51.0	50	°C/W
Plastic Quad Flat Pack (PQFP)	208	8.0	26	23.5	20.9	°C/W
Plastic Ball Grid Array (PBGA)	729	2.2	13.7	10.6	9.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.0	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	324	3.0	25.8	22.1	20.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	208	2.0	22	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA)[2]	624	6.5	8.9	8.5	8	°C/W

Notes:

1. *θ_{jc} for the 208-pin and 352-pin CQFP refers to the thermal resistance between the junction and the bottom of the package.*
2. *θ_{jc} for the 624-pin CCGA refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board (θ_{jb}) for CCGA 624 package is 3.4°C/W.*

Timing Characteristics

Axcelerator devices are manufactured in a CMOS process, therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-7 should be applied to all timing data contained within this datasheet.

Table 2-7 • **Temperature and Voltage Timing Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, VCCA = 1.425V)**

VCCA	Junction Temperature						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
1.4 V	0.83	0.86	0.91	0.96	1.02	1.05	1.15
1.425 V	0.82	0.84	0.90	0.94	1.00	1.04	1.13
1.5 V	0.78	0.80	0.85	0.89	0.95	0.98	1.07
1.575 V	0.74	0.76	0.81	0.85	0.90	0.94	1.02
1.6 V	0.73	0.75	0.80	0.84	0.89	0.92	1.01

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 175°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4V and 1.6V.*

All timing numbers listed in this datasheet represent sample timing characteristics of Axcelerator devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Microsemi's Designer software after place-and-route.

Timing Characteristics

Table 2-22 • 3.3 V LVTTL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 1 (8 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		14.28		16.27		19.13	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		15.25		17.37		20.42	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		14.26		16.24		19.09	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.56		1.57		1.58	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		1.95		1.96		1.97	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		039		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-22 • 3.3 V LVTTL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 1 (8 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		4.23		4.81		5.66	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		4.64		5.28		6.21	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.23		4.81		5.66	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.01		2.02		2.03	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-22 **• 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		3.30		3.76		4.42	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.74		4.26		5.00	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.06		3.49		4.10	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.29		2.30		2.31	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

1.5 V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-29 **• DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
–0.3	0.35 VCCI	0.65 VCCI	3.6	0.4	VCCI – 0.4	8 mA	–8 mA

AC Loadings

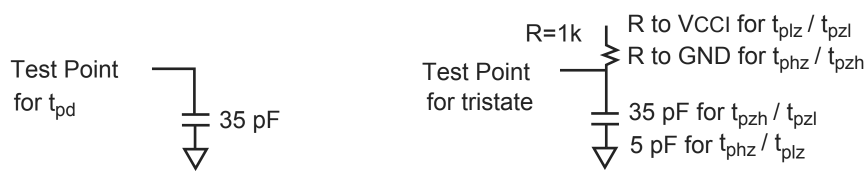


Table 2-30 **• AC Test Loads**

Table 2-31 **• AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
0	1.5	$0.5V_{CCI}$	N/A	35

*Note: * Measuring Point = VTRIP*

Module Specifications

C-Cell

Introduction

The C-cell is one of the two logic module types in the AX architecture. It is the combinatorial logic resource in the Axcelerator device. The AX architecture implements a new combinatorial cell that is an extension of the C-cell implemented in the SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The C-cell features the following (Figure 2-27):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns.
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns.

This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with Microsemi's extensive macro library (please see the *Antifuse Macro Library Guide* for a complete listing of available Axcelerator macros).

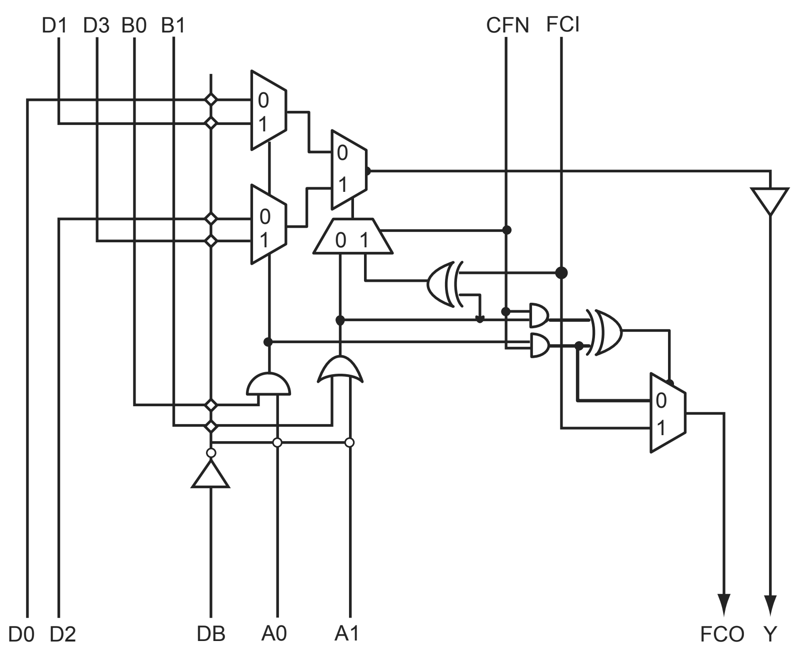


Figure 2-27 • **C-Cell**

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

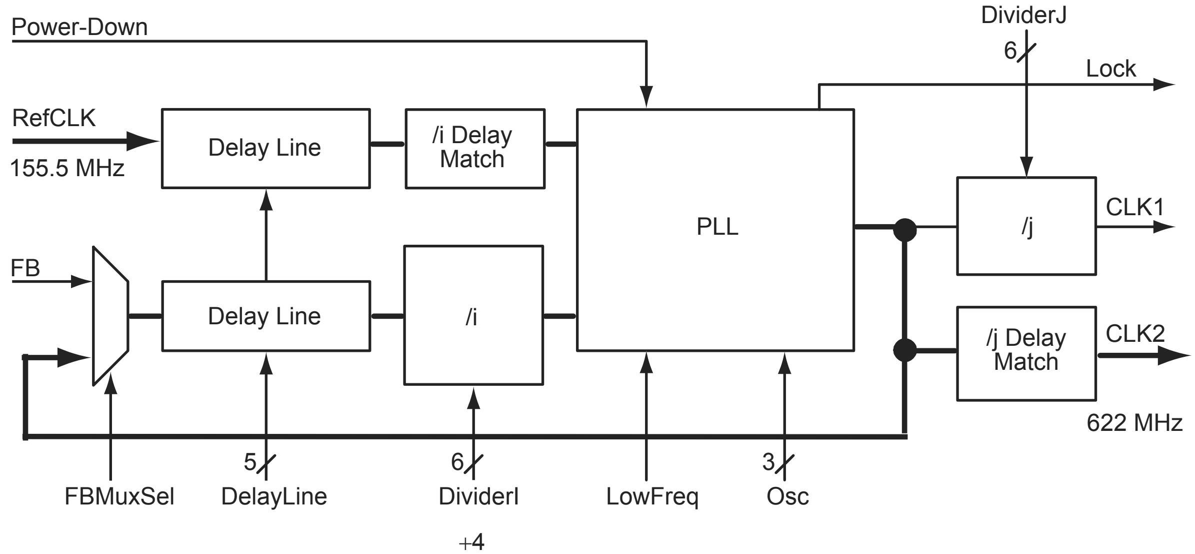


***Figure 2-53* • Using the PLL 155.5 MHz In, 622 MHz Out**

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

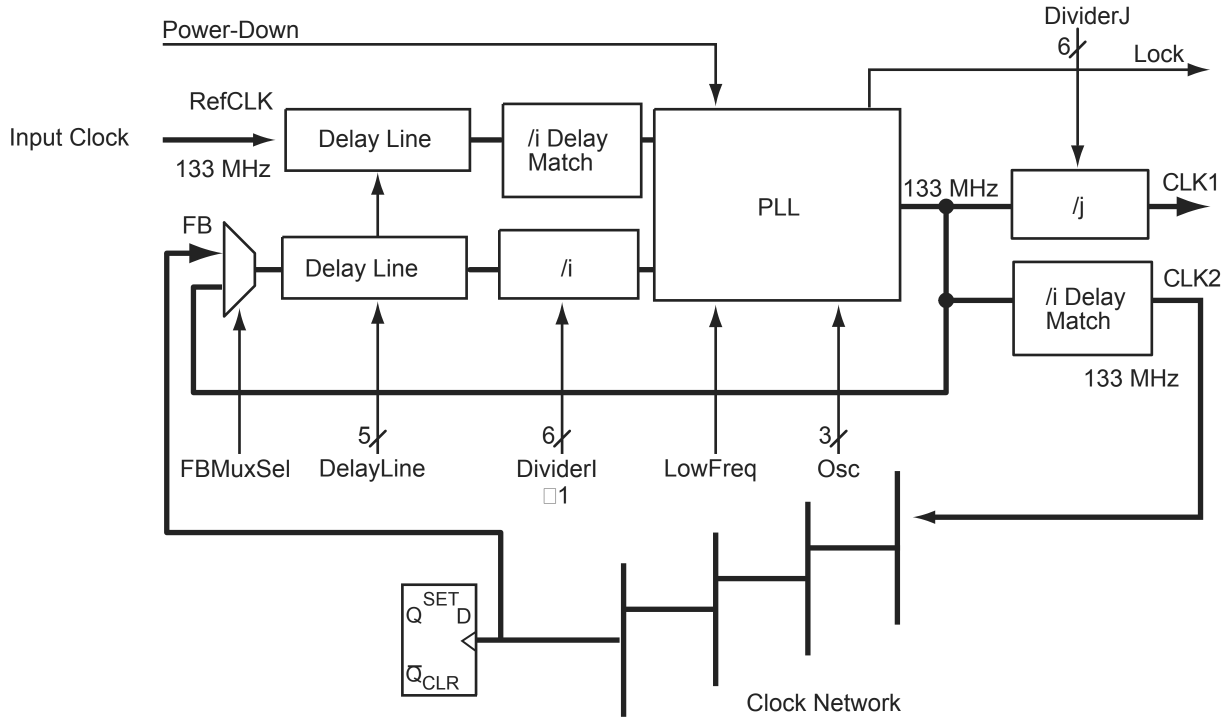


Figure 2-56 • **Using the PLL for Clock Deskewing**

Embedded Memory

The AX architecture provides extensive, high-speed memory resources to the user. Each 4,608 bit block of RAM contains its own embedded FIFO controller, allowing the user to configure each block as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate in synchronous mode for both read and write operations. However, the read and write clocks are completely independent, and each may operate up to and above 500 MHz.

No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The AX memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in Figure 2-57.

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

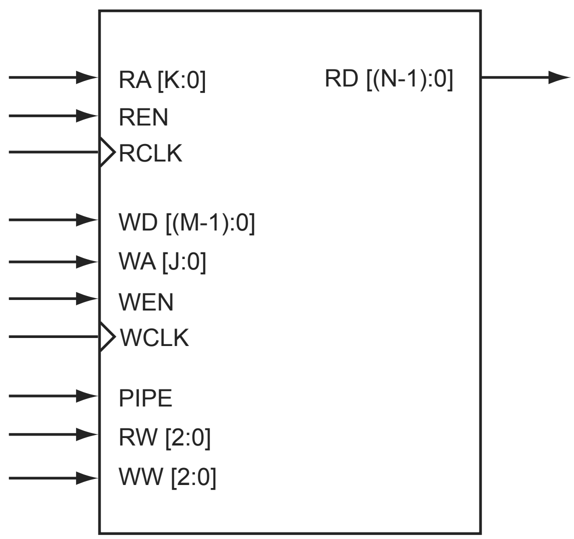


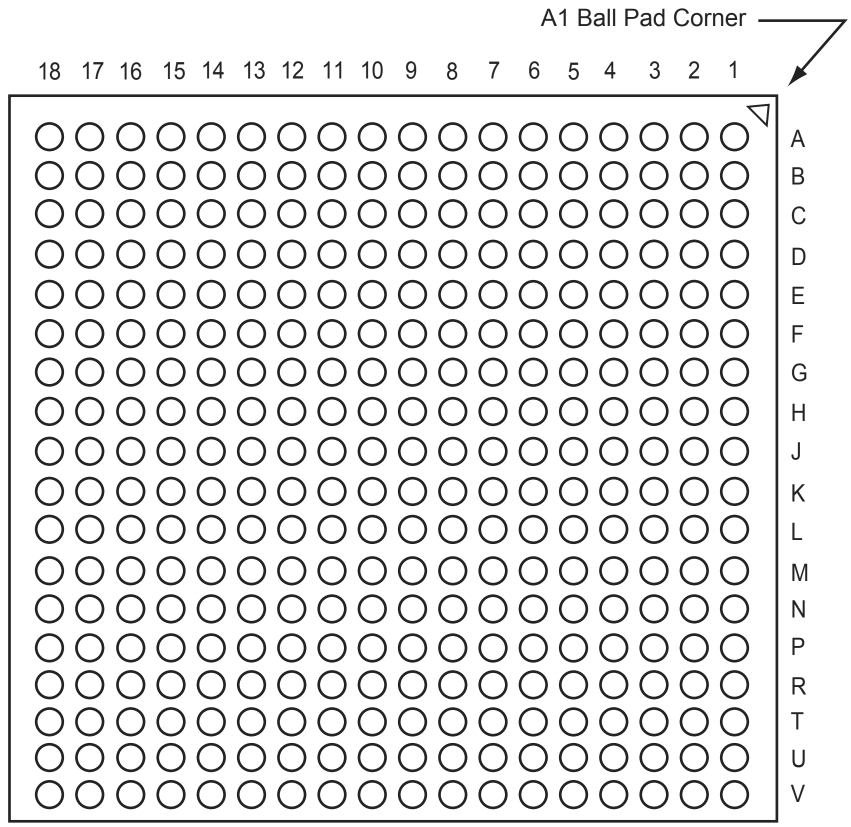
Figure 2-57 • **Axcelerator Memory Module**

Table 2-99 • Two FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
FIFO Module Timing								
t_{WSU}	Write Setup		13.75		15.66		18.41	ns
t_{WHD}	Write Hold		0.00		0.00		0.00	ns
t_{WCKH}	WCLK High		0.75		0.75		0.75	ns
t_{WCKL}	WCLK Low		1.76		1.76		1.76	ns
t_{WCKP}	Minimum WCLK Period	2.51		2.51		2.51		ns
t_{RSU}	Read Setup		14.33		16.32		19.19	ns
t_{RHD}	Read Hold		0.00		0.00		0.00	ns
t_{RCKH}	RCLK High		0.73		0.73		0.73	ns
t_{RCKL}	RCLK Low		1.89		1.89		1.89	ns
t_{RCKP}	Minimum RCLK period	2.62		2.62		2.62		ns
t_{CLRHF}	Clear High		0.00		0.00		0.00	ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.43		1.63		1.92	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Nonpipelined)		2.26		2.58		3.03	ns

Note: Timing data for these two cascaded FIFO blocks uses a depth of 8,192. For all other combinations, use Microsemi's timing software.

FG324



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG484	
AX500 Function	Pin Number
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
Bank 6	
IO126NB6F12	V2
IO126PB6F12	W2

FG484	
AX500 Function	Pin Number
IO127NB6F12	P7
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7

FG484	
AX500 Function	Pin Number
IO146NB6F13	M3
IO146PB6F13	N3
Bank 7	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3

FG484	
AX500 Function	Pin Number
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX500 Function	Pin Number
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX500 Function	Pin Number
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG484	
AX1000 Function	Pin Number
IO87PB2F8	H20
IO88NB2F8	L18
IO88PB2F8	K18
IO89NB2F8	K19
IO89PB2F8	J19
IO90NB2F8	J21
IO90PB2F8	H21
IO91NB2F8	J22
IO91PB2F8	H22
IO93NB2F8	K21
IO93PB2F8	K22
IO94NB2F8	L20
IO94PB2F8	K20
IO95NB2F8	M21
IO95PB2F8	L21
Bank 3	
IO96NB3F9	N16
IO96PB3F9	M16
IO97NB3F9	M19
IO97PB3F9	L19
IO98NB3F9	P22
IO98PB3F9	N22
IO99NB3F9	N20
IO99PB3F9	M20
IO100NB3F9	N17
IO100PB3F9	M17
IO101NB3F9	P21
IO101PB3F9	N21
IO103NB3F9	R20
IO103PB3F9	P20
IO104NB3F9	N18
IO104PB3F9	N19
IO105NB3F9	T22
IO105PB3F9	R22
IO106NB3F9	R17

FG484	
AX1000 Function	Pin Number
IO106PB3F9	P17
IO107NB3F10	T21
IO107PB3F10	R21
IO110NB3F10	V22
IO110PB3F10	U22
IO113NB3F10	V21
IO113PB3F10	U21
IO114NB3F10	P18
IO114PB3F10	P19
IO116PB3F10	R19
IO117NB3F10	U20
IO117PB3F10	T20
IO118NB3F11	T18
IO118PB3F11	R18
IO121NB3F11	U19
IO121PB3F11	T19
IO124NB3F11	R16
IO124PB3F11	P16
IO127NB3F11	W21
IO127PB3F11	W22
Bank 4	
IO129PB4F12	AB17
IO132NB4F12	Y19
IO132PB4F12	W18
IO133NB4F12	W17
IO133PB4F12	V17
IO135NB4F12	T15
IO135PB4F12	T16
IO138NB4F12	Y17
IO138PB4F12	Y18
IO139NB4F13	V15
IO139PB4F13	V16
IO140NB4F13	U18
IO140PB4F13	V19
IO142NB4F13	W20

FG484	
AX1000 Function	Pin Number
IO142PB4F13	V20
IO143NB4F13	W15
IO143PB4F13	W16
IO144NB4F13	AA18
IO144PB4F13	AA19
IO145NB4F13	U14
IO145PB4F13	U15
IO146NB4F13	Y15
IO146PB4F13	Y16
IO147NB4F13	AB18
IO147PB4F13	AB19
IO149NB4F13	Y14
IO149PB4F13	W14
IO150NB4F13	AA16
IO150PB4F13	AA17
IO152NB4F14	AA14
IO152PB4F14	AA15
IO154NB4F14	AB14
IO154PB4F14	AB15
IO155NB4F14	AA13
IO155PB4F14	AB13
IO158NB4F14	Y12
IO158PB4F14	Y13
IO159NB4F14/CLKEN	V12
IO159PB4F14/CLKEP	V13
IO160NB4F14/CLKFN	W11
IO160PB4F14/CLKFP	W12
Bank 5	
IO161NB5F15/CLKGN	U10
IO161PB5F15/CLKGP	U11
IO162NB5F15/CLKHN	V9
IO162PB5F15/CLKHP	V10
IO163NB5F15	Y10
IO163PB5F15	Y11
IO167NB5F15	AA11

CQ352	
AX250 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	F7
IO02NB0F0	G7
IO02PB0F0	G6
IO04NB0F0	E9
IO04PB0F0	D8
IO06NB0F0	G9
IO06PB0F0	G8
IO07PB0F0	B6
IO08NB0F0	F10
IO08PB0F0	F9
IO09PB0F0	C7
IO10NB0F0	H8
IO10PB0F0	H7
IO11NB0F0	D10
IO11PB0F0	D9
IO12NB0F1	B5
IO12PB0F1	B4
IO13NB0F1	A7
IO13PB0F1	A6
IO14NB0F1	C9
IO14PB0F1	C8
IO15PB0F1	B7
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	A9
IO17PB0F1	B9
IO18NB0F1	D12
IO18PB0F1	D11
IO20NB0F1	B11
IO20PB0F1	B10
IO21NB0F1	A11
IO21PB0F1	A10
IO22NB0F2	H10
IO22PB0F2	H9

CG624	
AX1000 Function	Pin Number
IO23NB0F2	E11
IO23PB0F2	F11
IO24NB0F2	D7
IO24PB0F2	E7
IO25PB0F2	B12
IO26NB0F2	H11
IO26PB0F2	G11
IO27NB0F2	C11
IO27PB0F2	B8
IO28NB0F2	J13
IO28PB0F2	K13
IO29NB0F2	J8
IO29PB0F2	J7
IO30NB0F2/HCLKAN	G13
IO30PB0F2/HCLKAP	G12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	C12
Bank 1	
IO32NB1F3/HCLKCN	G15
IO32PB1F3/HCLKCP	G14
IO33NB1F3/HCLKDN	B14
IO33PB1F3/HCLKDP	B13
IO34NB1F3	G16
IO34PB1F3	H16
IO35NB1F3	C17
IO35PB1F3	B18
IO36NB1F3	H18
IO36PB1F3	H15
IO37NB1F3	H13
IO38NB1F3	E15
IO38PB1F3	F15
IO39NB1F3	D14
IO39PB1F3	C14
IO40NB1F3	D16
IO40PB1F3	D15
IO41NB1F4	F16

CG624	
AX1000 Function	Pin Number
IO42NB1F4	G21
IO42PB1F4	G20
IO43NB1F4	A16
IO43PB1F4	A15
IO44NB1F4	A20
IO44PB1F4	A19
IO45NB1F4	B17
IO45PB1F4	B16
IO46NB1F4	G17
IO46PB1F4	H17
IO47NB1F4	A17
IO48NB1F4	C19
IO48PB1F4	C18
IO49NB1F4	B20
IO49PB1F4	B19
IO50NB1F4	H20
IO50PB1F4	H19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	C21
IO52PB1F4	C20
IO53NB1F4	B22
IO53PB1F4	B21
IO54NB1F5	J18
IO54PB1F5	J19
IO55NB1F5	D18
IO55PB1F5	D17
IO56NB1F5	F20
IO56PB1F5	F19
IO58NB1F5	E17
IO58PB1F5	F17
IO60NB1F5	D20
IO60PB1F5	D19
IO62NB1F5	E18
IO62PB1F5	F18
IO63NB1F5	G19

CG624	
AX2000 Function	Pin Number
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22*
IO169PB3F15	W23*
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20*
IO171PB4F16	AC21*
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

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5172160-18/3.12