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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-1fgg896m

2 – Detailed Specifications

Operating Conditions

Table 2-1 lists the absolute maximum ratings of Axcelerator devices. Stresses beyond the ratings may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommendations in Table 2-2.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCA	DC Core Supply Voltage	–0.3 to 1.7	V
VCCI	DC I/O Supply Voltage	–0.3 to 3.75	V
VREF	DC I/O Reference Voltage	–0.3 to 3.75	V
VI	Input Voltage	–0.5 to 4.1	V
VO	Output Voltage	–0.5 to 3.75	V
TSTG	Storage Temperature	–60 to +150	°C
VCCDA*	Supply Voltage for Differential I/Os	–0.3 to 3.75	V

Note: * Should be the maximum of all VCCI.

Table 2-2 • Recommended Operating Conditions

Parameter Range	Commercial	Industrial	Military	Units
Ambient Temperature (T_A) ¹	0 to +70	–40 to +85	–55 to +125	°C
1.5 V Core Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.5 V I/O Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.8 V I/O Supply Voltage	1.71 to 1.89	1.71 to 1.89	1.71 to 1.89	V
2.5 V I/O Supply Voltage	2.375 to 2.625	2.375 to 2.625	2.375 to 2.625	V
3.3 V I/O Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCDA Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VPUMP Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Notes:

1. Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.
2. $T_J \text{ max} = 125^\circ\text{C}$

Power-Up/Down Sequence

All Axcelerator I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. VCCDA should be powered up before (or coincidentally with) VCCA and VCCI to ensure the behavior of user I/Os at system start-up. Conversely, VCCDA should be powered down after (or coincidentally with) VCCA and VCCI. Note that VCCI and VCCA can be powered up in any sequence with respect to each other, provided the requirement with respect to VCCDA is satisfied.

Calculating Power Dissipation

Table 2-3 • Standby Current

Device	Temperature	ICCA	ICCD A	ICCBANK		ICCP LL	ICCCP ¹		IIH, IIL, IOZ ²	Units
		Standby Current (Core)	Standby Current, Differential I/O	Standby Current per I/O Bank		Standby Current per PLL	Standby Current, Charge Pump			
				2.5 V VCCI	3.3 V VCCI		Active	Bypassed Mode		
AX125	Typical at 25°C	1.5	1.5	0.2	0.3	0.2	0.3	0.01	±0.01	mA
	70°C	15	6	0.5	0.75	1	0.4	0.01	±0.01	mA
	85°C	25	6	0.6	0.8	1	0.4	0.2	±0.01	mA
	125°C	50	8	1	1.5	2	0.4	0.5	±0.01	mA
AX250	Typical at 25°C	1.5	1.4	0.25	0.4	0.2	0.3	0.01	±0.01	mA
	70°C	30	7	0.8	0.9	1	0.4	0.01	±0.01	mA
	85°C	40	7	0.8	1	1	0.4	0.2	±0.01	mA
	125°C	70	9	1.3	1.8	2	0.4	0.5	±0.01	mA
AX500	Typical at 25°C	5	1.4	0.4	0.75	0.2	0.3	0.01	±0.01	mA
	70°C	60	7	1	1.5	1	0.4	0.01	±0.01	mA
	85°C	80	7	1	1.9	1	0.4	0.2	±0.01	mA
	125°C	180	9	1.75	2.5	1.5	0.4	0.5	±0.01	mA
AX1000	Typical at 25°C	7.5	1.5	0.5	1.25	0.2	0.3	0.01	±0.01	mA
	70°C	80	8	1.5	3	1	0.4	0.01	±0.01	mA
	85°C	120	8	1.5	3.4	1	0.4	0.2	±0.01	mA
	125°C	200	10	3	4	1.5	0.4	0.5	±0.01	mA
AX2000	Typical at 25°C	20	1.6	0.7	1.5	0.2	0.3	0.01	±0.01	mA
	70°C	160	10	2	7	1	0.4	0.01	±0.01	mA
	85°C	200	10	3	8	1	0.4	0.2	±0.01	mA
	125°C	500	15	4	10	1.5	0.4	0.5	±0.01	mA

Notes:

1. ICCCP Active is the ICCDA or the Internal Charge Pump current. ICCCP Bypassed mode is the External Charge Pump current IIH (VPUMP pin).
2. IIH, IIL, or IOZ values are measured with inputs at the same level as VCCI for IIH and GND for IIL and IOZ.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

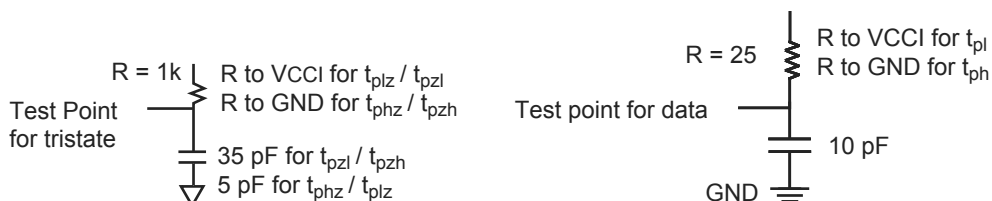


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-35 • 3.3 V PCI I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_j = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Output Module Timing								
t _{DP}	Input Buffer		1.57		1.79		2.10	ns
t _{PY}	Output Buffer		1.91		2.18		2.56	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-36 • 3.3 V PCI-X I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI-X Output Module Timing								
t _{DP}	Input Buffer	1.57		1.79		2.10		ns
t _{PY}	Output Buffer	2.10		2.40		2.82		ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low	1.61		1.62		1.63		ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High	1.59		1.60		1.61		ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z	2.65		3.02		3.55		ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z	3.11		3.55		4.17		ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register	0.67		0.77		0.90		ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

SSTL2

Stub Series Terminated Logic for 2.5 V is a general-purpose 2.5 V memory bus standard (JESD8-9). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-44 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF - 0.2	VREF + 0.2	3.6	VREF - 0.57	VREF + 0.57	7.6	-7.6

AC Loadings

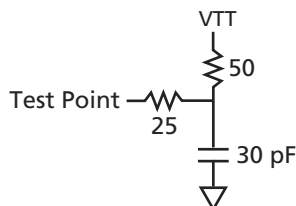


Figure 2-21 • AC Test Loads

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF - 0.75	VREF + 0.75	VREF	1.25	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-46 • 2.5 V SSTL2 Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

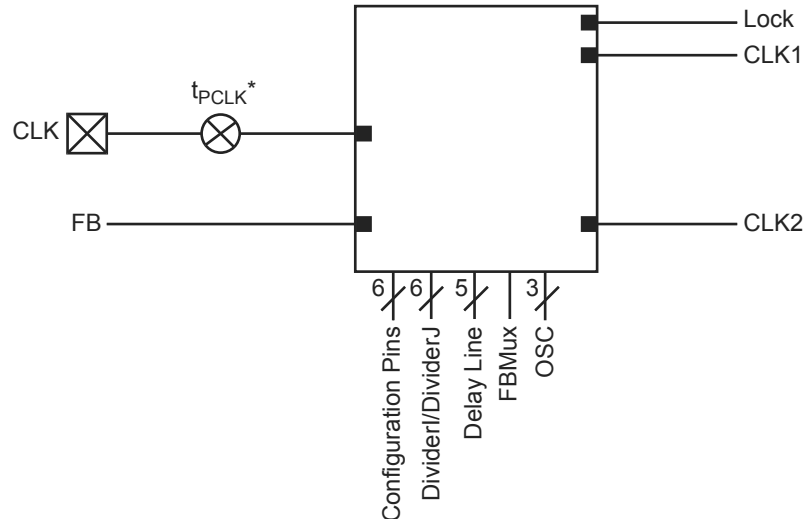
		-2 Speed		-1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V SSTL2 Class I I/O Module Timing								
t _{DP}	Input Buffer		1.83		2.08		2.45	ns
t _{PY}	Output Buffer		2.39		2.72		3.20	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model

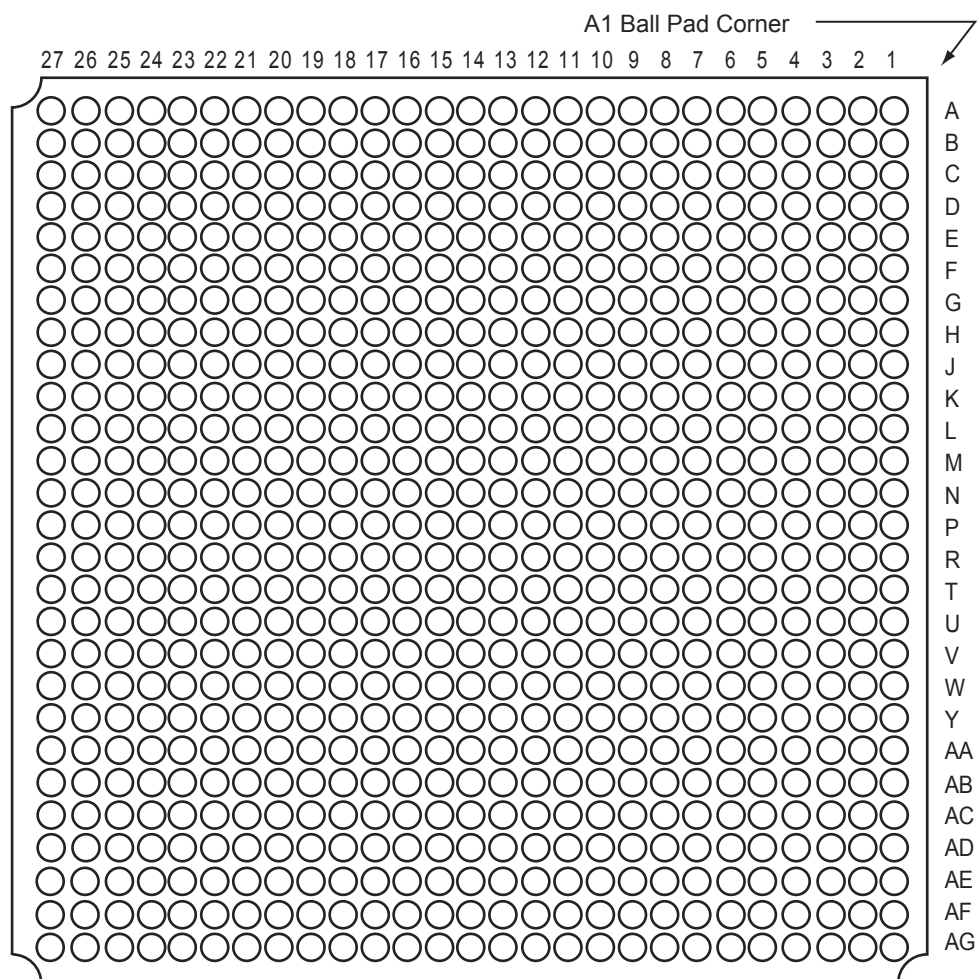


Note: t_{PCLK} is the delay in the clock signal

Figure 2-52 • PLL Model

3 – Package Pin Assignments

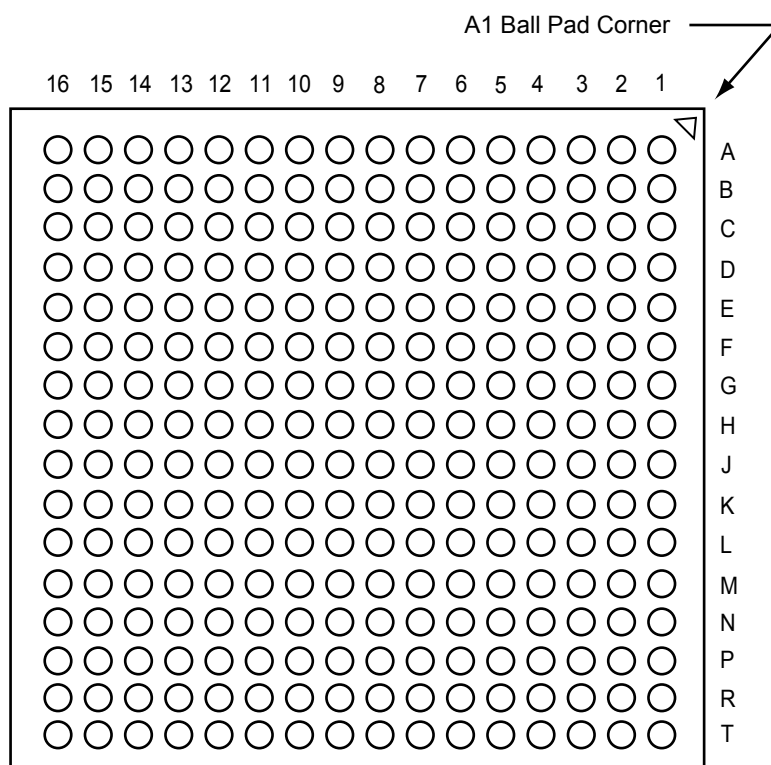
BG729



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG256



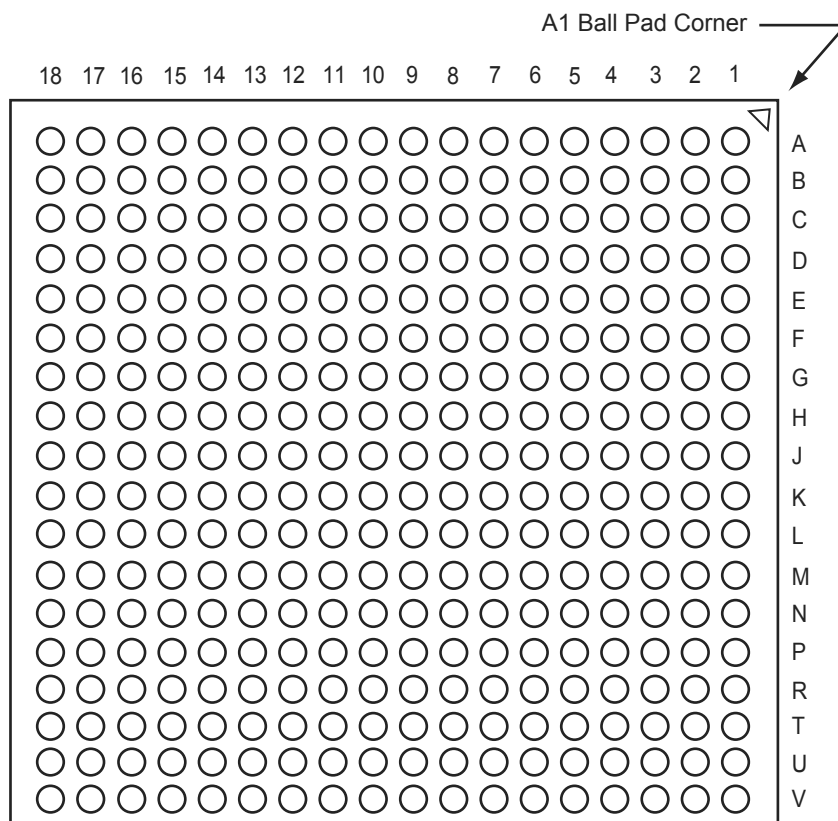
Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG256		FG256		FG256	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
Bank 0		IO32NB2F2	C16	IO61PB3F3	L14
IO01NB0F0	B4	IO32PB2F2	B16	Bank 4	
IO01PB0F0	B3	IO33NB2F2	F15	IO62NB4F4	N12
IO03NB0F0	A4	IO33PB2F2	E15	IO62PB4F4	N13
IO03PB0F0	A3	IO35NB2F2	H13	IO63NB4F4	T14
IO05NB0F0	B6	IO35PB2F2	G13	IO63PB4F4	R14
IO05PB0F0	B5	IO36NB2F2	E16	IO66PB4F4	T15
IO07NB0F0	A6	IO36PB2F2	D16	IO67NB4F4	R12
IO07PB0F0	A5	IO38NB2F2	H15	IO67PB4F4	R13
IO12NB0F0/HCLKAN	B8	IO38PB2F2	G15	IO69NB4F4	P11
IO12PB0F0/HCLKAP	B7	IO39NB2F2	H14	IO69PB4F4	P12
IO13NB0F0/HCLKBN	A9	IO39PB2F2	G14	IO70PB4F4	T11
IO13PB0F0/HCLKBP	A8	IO40NB2F2	G16	IO73NB4F4	T12
Bank 1		IO40PB2F2	F16	IO73PB4F4	T13
IO14NB1F1/HCLKCN	C10	IO43NB2F2	K15	IO74NB4F4/CLKEN	R9
IO14PB1F1/HCLKCP	C9	IO43PB2F2	K16	IO74PB4F4/CLKEP	R10
IO15NB1F1/HCLKDN	B11	IO44NB2F2	J16	IO75NB4F4/CLKFN	T8
IO15PB1F1/HCLKDP	B10	IO44PB2F2	H16	IO75PB4F4/CLKFP	T9
IO17NB1F1	A13	Bank 3		Bank 5	
IO17PB1F1	A12	IO45NB3F3	K13	IO76NB5F5/CLKGN	P7
IO19NB1F1	B13	IO45PB3F3	J13	IO76PB5F5/CLKGP	P8
IO19PB1F1	B12	IO46NB3F3	K14	IO77NB5F5/CLKHN	R6
IO21NB1F1	C12	IO46PB3F3	J14	IO77PB5F5/CLKHP	R7
IO21PB1F1	C11	IO52NB3F3	L15	IO79NB5F5	T5
IO23NB1F1	A15	IO52PB3F3	L16	IO79PB5F5	T6
IO23PB1F1	B14	IO54NB3F3	P16	IO81NB5F5	P5
IO26NB1F1	C15	IO54PB3F3	N16	IO81PB5F5	P6
IO26PB1F1	C14	IO55PB3F3	M16	IO83NB5F5	T3
IO27NB1F1	D13	IO56NB3F3	P15	IO83PB5F5	T4
IO27PB1F1	D12	IO56PB3F3	R16	IO85NB5F5	R3
Bank 2		IO58NB3F3	N15	IO85PB5F5	R4
IO29NB2F2	F13	IO58PB3F3	M15	IO88NB5F5	R1
IO29PB2F2	E13	IO59NB3F3	M13	IO88PB5F5	T2
IO30NB2F2	F14	IO59PB3F3	L13	IO89NB5F5	N4
IO30PB2F2	E14	IO61NB3F3	M14	IO89PB5F5	N5

FG256		FG256	
AX250 Function	Pin Number	AX250 Function	Pin Number
VCCA	L9	VCCIB4	M11
VCCA	N3	VCCIB4	M9
VCCA	P14	VCCIB5	M6
VCCPLA	C7	VCCIB5	M7
VCCPLB	D6	VCCIB5	M8
VCCPLC	A10	VCCIB6	J5
VCCPLD	D10	VCCIB6	K5
VCCPLE	P10	VCCIB6	L5
VCCPLF	N11	VCCIB7	F5
VCCPLG	T7	VCCIB7	G5
VCCPLH	N7	VCCIB7	H5
VCCDA	A11	VCOMPLA	A7
VCCDA	A2	VCOMPLB	D7
VCCDA	C13	VCOMPLC	B9
VCCDA	D9	VCOMPLD	D11
VCCDA	H1	VCOMPLE	T10
VCCDA	J15	VCOMPLF	N10
VCCDA	N14	VCOMPLG	R8
VCCDA	N8	VCOMPLH	N6
VCCDA	P4	VPUMP	A14
VCCDA	R11		
VCCDA	R5		
VCCIB0	E6		
VCCIB0	E7		
VCCIB0	E8		
VCCIB1	E10		
VCCIB1	E11		
VCCIB1	E9		
VCCIB2	F12		
VCCIB2	G12		
VCCIB2	H12		
VCCIB3	J12		
VCCIB3	K12		
VCCIB3	L12		
VCCIB4	M10		

FG324



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	T12	GND	W19	NC	AJ4
GND	T13	GND	Y11	NC	AK14
GND	T14	GND	Y20	NC	AK15
GND	T15	GND/LP	E4	NC	AK16
GND	T16	NC	A16	NC	AK17
GND	T17	NC	A26	NC	AK22
GND	T18	NC	A4	NC	AK4
GND	T19	NC	A6	NC	AK5
GND	T28	NC	AA30	NC	B16
GND	T3	NC	AB1	NC	B18
GND	U12	NC	AB30	NC	B21
GND	U13	NC	AC2	NC	B23
GND	U14	NC	AC29	NC	B26
GND	U15	NC	AD1	NC	B4
GND	U16	NC	AD2	NC	B6
GND	U17	NC	AD30	NC	B8
GND	U18	NC	AE1	NC	C27
GND	U19	NC	AE15	NC	D1
GND	V1	NC	AE16	NC	D2
GND	V12	NC	AE2	NC	D29
GND	V13	NC	AE30	NC	D30
GND	V14	NC	AF1	NC	E1
GND	V15	NC	AF2	NC	E2
GND	V16	NC	AF29	NC	E29
GND	V17	NC	AF30	NC	E30
GND	V18	NC	AG1	NC	F15
GND	V19	NC	AG2	NC	F16
GND	V30	NC	AG29	NC	F29
GND	W12	NC	AG30	NC	F30
GND	W13	NC	AH27	NC	G1
GND	W14	NC	AH4	NC	G29
GND	W15	NC	AJ14	NC	G30
GND	W16	NC	AJ15	NC	H29
GND	W17	NC	AJ16	NC	J1
GND	W18	NC	AJ27	NC	J30

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	N1	GND	U19	NC	A26
GND	N13	GND	U20	NC	AB2
GND	N22	GND	U21	NC	AB33
GND	N34	GND	U30	NC	AC34
GND	P14	GND	U5	NC	AD3
GND	P15	GND	V14	NC	AD34
GND	P16	GND	V15	NC	AE31
GND	P17	GND	V16	NC	AE33
GND	P18	GND	V17	NC	AE34
GND	P19	GND	V18	NC	AF1
GND	P20	GND	V19	NC	AF34
GND	P21	GND	V20	NC	AG2
GND	R14	GND	V21	NC	AG4
GND	R15	GND	V30	NC	AH1
GND	R16	GND	V5	NC	AH2
GND	R17	GND	W14	NC	AH31
GND	R18	GND	W15	NC	AH32
GND	R19	GND	W16	NC	AH34
GND	R20	GND	W17	NC	AJ1
GND	R21	GND	W18	NC	AJ2
GND	R3	GND	W19	NC	AJ3
GND	R32	GND	W20	NC	AJ31
GND	T14	GND	W21	NC	AJ32
GND	T15	GND	Y14	NC	AJ33
GND	T16	GND	Y15	NC	AJ34
GND	T17	GND	Y16	NC	AJ4
GND	T18	GND	Y17	NC	AL29
GND	T19	GND	Y18	NC	AM19
GND	T20	GND	Y19	NC	AM7
GND	T21	GND	Y20	NC	AN13
GND	U14	GND	Y21	NC	AN17
GND	U15	GND	Y3	NC	AN25
GND	U16	GND	Y32	NC	AN27
GND	U17	GND/LP	G6	NC	AN8
GND	U18	NC	A17	NC	AP17

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
VCCIB0	C5	VCCIB3	AA24	VCCIB6	AA11
VCCIB0	D5	VCCIB3	AB23	VCCIB6	AA12
VCCIB0	L12	VCCIB3	AB24	VCCIB6	AB11
VCCIB0	L13	VCCIB3	AC24	VCCIB6	AB12
VCCIB0	L14	VCCIB3	AK31	VCCIB6	AC11
VCCIB0	M13	VCCIB3	AK32	VCCIB6	AK1
VCCIB0	M14	VCCIB3	AK33	VCCIB6	AK2
VCCIB0	M15	VCCIB3	AK34	VCCIB6	AK3
VCCIB0	M16	VCCIB3	V23	VCCIB6	AK4
VCCIB0	M17	VCCIB3	W23	VCCIB6	V12
VCCIB1	A30	VCCIB3	Y23	VCCIB6	W12
VCCIB1	B30	VCCIB4	AC18	VCCIB6	Y12
VCCIB1	C30	VCCIB4	AC19	VCCIB7	E1
VCCIB1	D30	VCCIB4	AC20	VCCIB7	E2
VCCIB1	L21	VCCIB4	AC21	VCCIB7	E3
VCCIB1	L22	VCCIB4	AC22	VCCIB7	E4
VCCIB1	L23	VCCIB4	AD21	VCCIB7	M11
VCCIB1	M18	VCCIB4	AD22	VCCIB7	N11
VCCIB1	M19	VCCIB4	AD23	VCCIB7	N12
VCCIB1	M20	VCCIB4	AL30	VCCIB7	P11
VCCIB1	M21	VCCIB4	AM30	VCCIB7	P12
VCCIB1	M22	VCCIB4	AN30	VCCIB7	R12
VCCIB2	E31	VCCIB4	AP30	VCCIB7	T12
VCCIB2	E32	VCCIB5	AC13	VCCIB7	U12
VCCIB2	E33	VCCIB5	AC14	VCCPLA	J16
VCCIB2	E34	VCCIB5	AC15	VCCPLB	K17
VCCIB2	M24	VCCIB5	AC16	VCCPLC	J19
VCCIB2	N23	VCCIB5	AC17	VCCPLD	L18
VCCIB2	N24	VCCIB5	AD12	VCCPLE	AK19
VCCIB2	P23	VCCIB5	AD13	VCCPLF	AE18
VCCIB2	P24	VCCIB5	AD14	VCCPLG	AK16
VCCIB2	R23	VCCIB5	AL5	VCCPLH	AF17
VCCIB2	T23	VCCIB5	AM5	VCOMPLA	H16
VCCIB2	U23	VCCIB5	AN5	VCOMPLB	L17
VCCIB3	AA23	VCCIB5	AP5	VCOMPLC	H19

FG1152	
AX2000 Function	Pin Number
VCOMPLD	K18
VCOMPLE	AH19
VCOMPLF	AF18
VCOMPLG	AH16
VCOMPLH	AD17
VPUMP	J26

PQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	Pin Number
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX250 Function	Pin Number
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX250 Function	Pin Number
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282

CQ352	
AX250 Function	Pin Number
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224

CQ352	
AX250 Function	Pin Number
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

CQ352	
AX2000 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX2000 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	D7*
IO00PB0F0	E7*
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9*
IO13PB0F1	D8*
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11*
IO26PB0F2	B8*

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.