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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	729-BBGA
Supplier Device Package	729-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-2bg729i

The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).

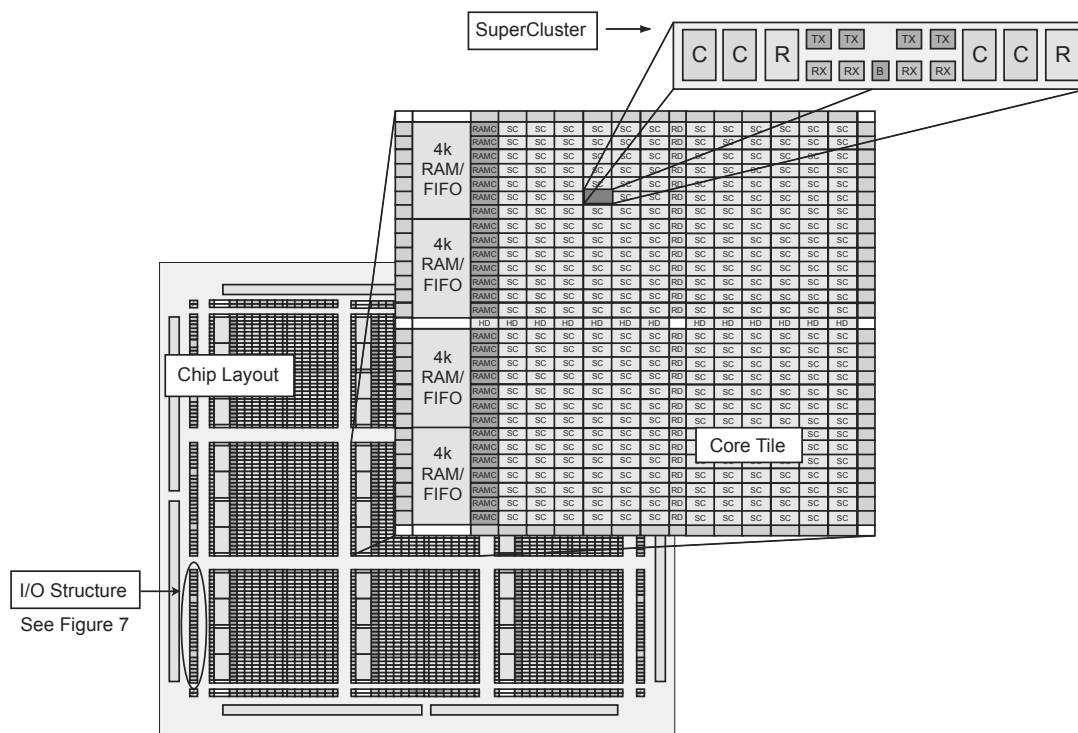


Figure 1-6 • AX Device Architecture (AX1000 shown)

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

Table 2-5 • Different Components Contributing to the Total Power Consumption in Axcelerator Devices

Component	Definition	Device Specific Value (in $\mu\text{W}/\text{MHz}$)				
		AX125	AX250	AX500	AX1000	AX2000
P1	Core tile HCLK power component	33	49	71	130	216
P2	R-cell power component	0.2	0.2	0.2	0.2	0.2
P3	HCLK signal power dissipation	4.5	4.5	9	13.5	18
P4	Core tile RCLK power component	33	49	71	130	216
P5	R-cell power component	0.3	0.3	0.3	0.3	0.3
P6	RCLK signal power dissipation	6.5	6.5	13	19.5	26
P7	Power dissipation due to the switching activity on the R-cell	1.6	1.6	1.6	1.6	1.6
P8	Power dissipation due to the switching activity on the C-cell	1.4	1.4	1.4	1.4	1.4
P9	Power component associated with the input voltage	10	10	10	10	10
P10	Power component associated with the output voltage	See table Per pin contribution				
P11	Power component associated with the read operation in the RAM block	25	25	25	25	25
P12	Power component associated with the write operation in the RAM block	30	30	30	30	30
P13	Core PLL power component	1.5	1.5	1.5	1.5	1.5

$$P_{total} = P_{dc} + P_{ac}$$

$$P_{dc} = ICCA * VCCA$$

$$P_{ac} = P_{HCLK} + P_{CLK} + P_{R-cells} + P_{C-cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$$

$$P_{HCLK} = (P1 + P2 * s + P3 * \sqrt{s}) * F_s$$

s = the number of R-cells clocked by this clock

F_s = the clock frequency

$$P_{CLK} = (P4 + P5 * s + P6 * \sqrt{s}) * F_s$$

s = the number of R-cells clocked by this clock

F_s = the clock frequency

$$P_{R-cells} = P7 * ms * F_s$$

ms = the number of R-cells switching at each F_s cycle

F_s = the clock frequency

$$P_{C-cells} = P8 * mc * F_s$$

mc = the number of C-cells switching at each F_s cycle

F_s = the clock frequency

$$P_{inputs} = P9 * pi * F_{pi}$$

pi = the number of inputs

F_{pi} = the average input frequency

User-Defined Supply Pins

VREF Supply Voltage

Reference voltage for I/O banks. VREF pins are configured by the user from regular I/O pins; VREF pins are not in fixed locations. There can be one or more VREF pins in an I/O bank.

Global Pins

HCLKA/B/C/D Dedicated (Hardwired) Clocks A, B, C and D

These pins are the clock inputs for sequential modules or north PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When the HCLK pins are unused, it is recommended that they are tied to ground.

CLKE/F/G/H Routed Clocks E, F, G, and H

These pins are clock inputs for clock distribution networks or south PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. The clock input is buffered prior to clocking the R-cells. When the CLK pins are unused, Microsemi recommends that they are tied to ground.

JTAG/Probe Pins

PRA/B/C/D Probe A, B, C and D

The Probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins' probe capabilities can be permanently disabled to protect programmed design confidentiality. The probe pins are of LVTTTL output levels.

TCK Test Clock

Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

TDI Test Data Input

Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal 10 k Ω pull-up resistor.

TDO Test Data Output

Serial output for JTAG boundary-scan testing.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, TRST). TMS is equipped with an internal 10 k Ω pull-up resistor.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a 10 k Ω pull-up resistor.

Special Functions

LP Low Power Pin

The LP pin controls the low power mode of Axcelerator devices. The device is placed in the low power mode by connecting the LP pin to logic high. To exit the low power mode, the LP pin must be set Low. Additionally, the LP pin must be set Low during chip powering-up or chip powering-down operations. See "Low Power Mode" on page 2-106 for more details.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

Note that the RAM blocks employ little-endian byte order for read and write operations.

Table 2-88 • RAM Signal Description

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus. The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to 15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

Table 2-101 • Eight FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		15.46		17.61		20.70	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		5.13		5.13		5.13	ns
t _{WCKP}	Minimum WCLK Period	5.88		5.88		5.88		ns
t _{RSU}	Read Setup		16.22		18.47		21.72	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		5.77		5.77		5.77	ns
t _{RCKP}	Minimum RCLK period	6.50		6.50		6.50		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		3.39		3.86		4.54	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		4.93		5.62		6.61	ns

Note: Timing data for these eight cascaded FIFO blocks uses a depth of 32,768. For all other combinations, use Microsemi's timing software.

throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is protected with highest level of security in the industry.



Figure 2-69 • FuseLock Logo

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to the *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (Figure 2-31 on page 2-58). Default setting is to clear all registers (GCLR = 0 and GPSET = 1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET = 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-108).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-7). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

BG729	
AX1000 Function	Pin Number
IO109NB3F10	V24
IO109PB3F10	V25
IO110NB3F10	T20
IO110PB3F10	T21
IO111NB3F10	W26
IO111PB3F10	W27
IO112NB3F10	U22
IO112PB3F10	U23
IO113NB3F10	Y26
IO113PB3F10	Y27
IO114NB3F10	U20
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	W25
IO116NB3F10	V22
IO116PB3F10	V23
IO117NB3F10	Y24
IO117PB3F10	Y25
IO118NB3F11	V20
IO118PB3F11	V21
IO119NB3F11	AA26
IO119PB3F11	AA27
IO120NB3F11	W22
IO120PB3F11	W23
IO121NB3F11	AA24
IO121PB3F11	AA25
IO122NB3F11	W20
IO122PB3F11	W21
IO123NB3F11	AB26
IO123PB3F11	AB27
IO124NB3F11	Y22
IO124PB3F11	Y23
IO125NB3F11	AB24
IO125PB3F11	AB25
IO126NB3F11	AA22
IO126PB3F11	AA23
IO127NB3F11	AC26

BG729	
AX1000 Function	Pin Number
IO127PB3F11	AC27
IO128NB3F11	Y20
IO128PB3F11	W19
Bank 4	
IO129NB4F12	AA20
IO129PB4F12	Y21
IO130NB4F12	AB22
IO130PB4F12	AB23
IO131NB4F12	AC22
IO131PB4F12	AC23
IO132NB4F12	AD23
IO132PB4F12	AD24
IO133NB4F12	AF23
IO133PB4F12	AE23
IO134NB4F12	AC21
IO134PB4F12	AB21
IO135NB4F12	AC20
IO135PB4F12	AB20
IO136NB4F12	AD21
IO136PB4F12	AD22
IO137NB4F12	Y19
IO137PB4F12	AA19
IO138NB4F12	AE21
IO138PB4F12	AE22
IO139NB4F13	AF21
IO139PB4F13	AF22
IO140NB4F13	AG22
IO140PB4F13	AG23
IO141NB4F13	Y18
IO141PB4F13	AA18
IO142NB4F13	AE20
IO142PB4F13	AD20
IO143NB4F13	AG20
IO143PB4F13	AG21
IO144NB4F13	AC19
IO144PB4F13	AB19
IO145NB4F13	AD18

BG729	
AX1000 Function	Pin Number
IO145PB4F13	AD19
IO146NB4F13	AC18
IO146PB4F13	AB18
IO147NB4F13	Y17
IO147PB4F13	AA17
IO148NB4F13	AF19
IO148PB4F13	AF20
IO149NB4F13	AC17
IO149PB4F13	AB17
IO150NB4F13	AE18
IO150PB4F13	AE19
IO151NB4F13	AA16
IO151PB4F13	Y16
IO152NB4F14	AG18
IO152PB4F14	AG19
IO153NB4F14	AC16
IO153PB4F14	AB16
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AB15
IO155PB4F14	AC15
IO156NB4F14	AE16
IO156PB4F14	AE17
IO157NB4F14	Y15
IO157PB4F14	AA15
IO158NB4F14	AG16
IO158PB4F14	AG17
IO159NB4F14/CLKEN	AF15
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AD14
IO160PB4F14/CLKFP	AD15
Bank 5	
IO161NB5F15/CLKGN	AE14
IO161PB5F15/CLKGP	AE15
IO162NB5F15/CLKHN	AC13
IO162PB5F15/CLKHP	AD13
IO163NB5F15	Y14

BG729	
AX1000 Function	Pin Number
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16

BG729	
AX1000 Function	Pin Number
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
IO52NB3F3	P18	IO69PB4F4	AA17	IO87NB5F5	Y4
IO52PB3F3	P19	IO70NB4F4	AB14	IO87PB5F5	Y5
IO53NB3F3	R20	IO70PB4F4	AB15	IO88NB5F5	V6
IO53PB3F3	P20	IO71NB4F4	Y14	IO88PB5F5	V7
IO54NB3F3	T21	IO71PB4F4	W14	IO89NB5F5	T7
IO54PB3F3	R21	IO72NB4F4	AA14	IO89PB5F5	T8
IO55NB3F3	R17	IO72PB4F4	AA15	Bank 6	
IO55PB3F3	P17	IO73NB4F4	AA13	IO90NB6F6	V4
IO56NB3F3	U20	IO73PB4F4	AB13	IO90PB6F6	W5
IO56PB3F3	T20	IO74NB4F4/CLKEN	V12	IO91NB6F6	P7
IO57NB3F3	T18	IO74PB4F4/CLKEP	V13	IO91PB6F6	R7
IO57PB3F3	R18	IO75NB4F4/CLKFN	W11	IO92NB6F6	U5
IO58NB3F3	U19	IO75PB4F4/CLKFP	W12	IO92PB6F6	T5
IO58PB3F3	T19	Bank 5		IO93NB6F6	P6
IO59NB3F3	R16	IO76NB5F5/CLKGN	U10	IO93PB6F6	R6
IO59PB3F3	P16	IO76PB5F5/CLKGP	U11	IO94NB6F6	T4
IO60NB3F3	W20	IO77NB5F5/CLKHN	V9	IO94PB6F6	U4
IO60PB3F3	V20	IO77PB5F5/CLKHP	V10	IO95NB6F6	P5
IO61NB3F3	U18	IO78NB5F5	AA9	IO95PB6F6	R5
IO61PB3F3	V19	IO78PB5F5	AA10	IO96NB6F6	T3
Bank 4		IO79NB5F5	AB9	IO96PB6F6	U3
IO62NB4F4	T15	IO79PB5F5	AB10	IO97NB6F6	P3
IO62PB4F4	T16	IO80NB5F5	AA7	IO97PB6F6	R3
IO63NB4F4	W17	IO80PB5F5	AA8	IO98NB6F6	R2
IO63PB4F4	V17	IO81NB5F5	W8	IO98PB6F6	T2
IO64NB4F4	V15	IO81PB5F5	W9	IO99NB6F6	P4
IO64PB4F4	V16	IO82NB5F5	AB5	IO99PB6F6	R4
IO65NB4F4	Y19	IO82PB5F5	AB6	IO100NB6F6	P1
IO65PB4F4	W18	IO83NB5F5	AA5	IO100PB6F6	R1
IO66NB4F4	AB18	IO83PB5F5	AA6	IO101NB6F6	M7
IO66PB4F4	AB19	IO84NB5F5	U8	IO101PB6F6	N7
IO67NB4F4	W15	IO84PB5F5	U9	IO102NB6F6	N2
IO67PB4F4	W16	IO85NB5F5	Y6	IO102PB6F6	P2
IO68NB4F4	U14	IO85PB5F5	Y7	IO103NB6F6	M6
IO68PB4F4	U15	IO86NB5F5	W6	IO103PB6F6	N6
IO69NB4F4	AA16	IO86PB5F5	W7	IO104NB6F6	M4

FG484	
AX500 Function	Pin Number
IO54PB2F5	H22
IO55NB2F5	L17
IO55PB2F5	K17
IO56NB2F5	K21
IO56PB2F5	K22
IO58NB2F5	L20
IO58PB2F5	K20
IO59NB2F5	L18
IO59PB2F5	K18
IO60NB2F5	M21
IO60PB2F5	L21
IO61NB2F5	L16
IO61PB2F5	K16
IO62NB2F5	M19
IO62PB2F5	L19
Bank 3	
IO63NB3F6	N16
IO63PB3F6	M16
IO64NB3F6	P22
IO64PB3F6	N22
IO65NB3F6	N20
IO65PB3F6	M20
IO66NB3F6	P21
IO66PB3F6	N21
IO67NB3F6	N18
IO67PB3F6	N19
IO68NB3F6	T22
IO68PB3F6	R22
IO69NB3F6	N17
IO69PB3F6	M17
IO70NB3F6	T21
IO70PB3F6	R21
IO71NB3F6	P18
IO71PB3F6	P19
IO72NB3F6	R20

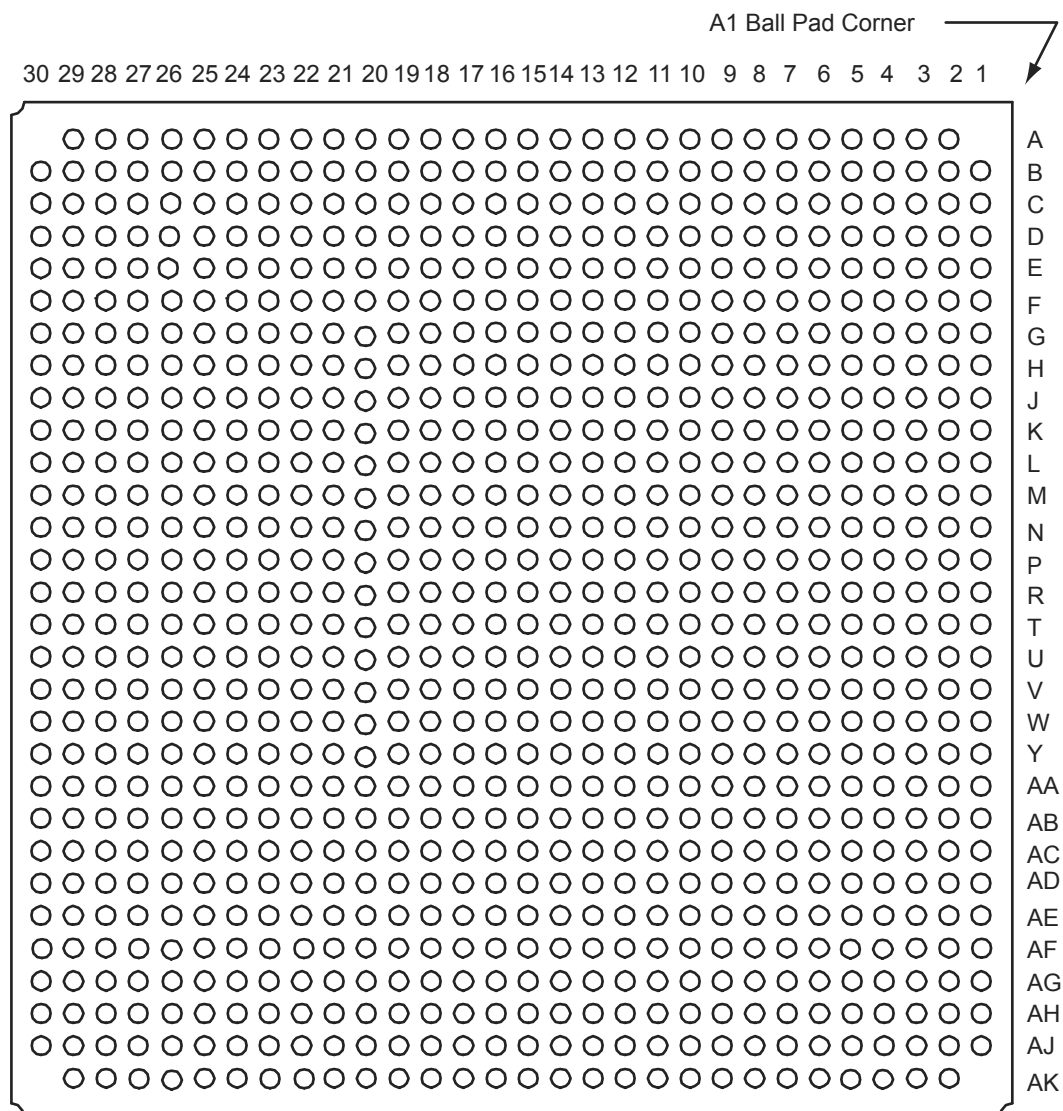
FG484	
AX500 Function	Pin Number
IO72PB3F6	P20
IO73PB3F6	R19
IO74NB3F7	V21
IO74PB3F7	U21
IO75NB3F7	V22
IO75PB3F7	U22
IO76NB3F7	U20
IO76PB3F7	T20
IO77NB3F7	R17
IO77PB3F7	P17
IO78NB3F7	W21
IO78PB3F7	W22
IO79NB3F7	T18
IO79PB3F7	R18
IO80NB3F7	W20
IO80PB3F7	V20
IO81NB3F7	U19
IO81PB3F7	T19
IO82NB3F7	U18
IO82PB3F7	V19
IO83NB3F7	R16
IO83PB3F7	P16
Bank 4	
IO84NB4F8	AB18
IO84PB4F8	AB19
IO85NB4F8	T15
IO85PB4F8	T16
IO86NB4F8	AA18
IO86PB4F8	AA19
IO87NB4F8	W17
IO87PB4F8	V17
IO88NB4F8	Y19
IO88PB4F8	W18
IO89NB4F8	U14
IO89PB4F8	U15

FG484	
AX500 Function	Pin Number
IO90NB4F8	Y17
IO90PB4F8	Y18
IO91NB4F8	V15
IO91PB4F8	V16
IO92PB4F8	AB17
IO93NB4F8	Y15
IO93PB4F8	Y16
IO94NB4F9	AA16
IO94PB4F9	AA17
IO95NB4F9	AB14
IO95PB4F9	AB15
IO96NB4F9	W15
IO96PB4F9	W16
IO97NB4F9	AA13
IO97PB4F9	AB13
IO98NB4F9	AA14
IO98PB4F9	AA15
IO100NB4F9	Y14
IO100PB4F9	W14
IO101NB4F9	Y12
IO101PB4F9	Y13
IO102NB4F9	AA11
IO102PB4F9	AA12
IO103NB4F9/CLKEN	V12
IO103PB4F9/CLKEP	V13
IO104NB4F9/CLKFN	W11
IO104PB4F9/CLKFP	W12
Bank 5	
IO105NB5F10/CLKGN	U10
IO105PB5F10/CLKGP	U11
IO106NB5F10/CLKHN	V9
IO106PB5F10/CLKHP	V10
IO107NB5F10	Y10
IO107PB5F10	Y11
IO108NB5F10	AA9

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO51PB1F4	E21	IO68PB2F6	K24	IO86NB2F8	N28
IO52NB1F4	F22	IO69NB2F6	F27	IO86PB2F8	N27
IO52PB1F4	E22	IO69PB2F6	E27	IO87NB2F8	P29
IO53NB1F4	B25	IO70NB2F6	J26	IO87PB2F8	P30
IO53PB1F4	B24	IO70PB2F6	J25	IO88NB2F8	P25
IO54NB1F5	D24	IO71NB2F6	H27	IO88PB2F8	P24
IO54PB1F5	D23	IO71PB2F6	G27	IO89NB2F8	P28
IO55NB1F5	F23	IO72NB2F6	J28	IO89PB2F8	P27
IO55PB1F5	E23	IO72PB2F6	H28	IO90NB2F8	P22
IO56NB1F5	H21	IO73NB2F6	G28	IO90PB2F8	P23
IO56PB1F5	G21	IO73PB2F6	F28	IO91NB2F8	R26
IO57NB1F5	D25	IO74NB2F7	L23	IO91PB2F8	P26
IO57PB1F5	C25	IO74PB2F7	L24	IO92NB2F8	R24
IO58NB1F5	F24	IO75NB2F7	L26	IO92PB2F8	R25
IO58PB1F5	E24	IO75PB2F7	K26	IO93NB2F8	R29
IO59NB1F5	D26	IO76NB2F7	M25	IO93PB2F8	R30
IO59PB1F5	C26	IO76PB2F7	L25	IO94NB2F8	R22
IO60NB1F5	G23	IO77NB2F7	K27	IO94PB2F8	R23
IO60PB1F5	G22	IO77PB2F7	J27	IO95NB2F8	T27
IO61NB1F5	B27	IO78NB2F7	M27	IO95PB2F8	R27
IO61PB1F5	A27	IO78PB2F7	L27	Bank 3	
IO62NB1F5	F25	IO79NB2F7	K30	IO96NB3F9	T29
IO62PB1F5	E25	IO79PB2F7	K29	IO96PB3F9	T30
IO63NB1F5	H23	IO80NB2F7	M23	IO97NB3F9	U29
IO63PB1F5	H22	IO80PB2F7	M24	IO97PB3F9	U30
Bank 2		IO81NB2F7	M28	IO98NB3F9	T22
IO64NB2F6	K23	IO81PB2F7	L28	IO98PB3F9	T23
IO64PB2F6	J23	IO82NB2F7	N26	IO99NB3F9	U26
IO65NB2F6	J24	IO82PB2F7	M26	IO99PB3F9	T26
IO65PB2F6	H24	IO83NB2F7	N25	IO100NB3F9	U24
IO66NB2F6	H26	IO83PB2F7	N24	IO100PB3F9	T24
IO66PB2F6	H25	IO84NB2F7	N22	IO101NB3F9	V28
IO67NB2F6	G26	IO84PB2F7	N23	IO101PB3F9	U28
IO67PB2F6	G25	IO85NB2F8	M29	IO102NB3F9	U23
IO68NB2F6	K25	IO85PB2F8	L29	IO102PB3F9	U22

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	T12	GND	W19	NC	AJ4
GND	T13	GND	Y11	NC	AK14
GND	T14	GND	Y20	NC	AK15
GND	T15	GND/LP	E4	NC	AK16
GND	T16	NC	A16	NC	AK17
GND	T17	NC	A26	NC	AK22
GND	T18	NC	A4	NC	AK4
GND	T19	NC	A6	NC	AK5
GND	T28	NC	AA30	NC	B16
GND	T3	NC	AB1	NC	B18
GND	U12	NC	AB30	NC	B21
GND	U13	NC	AC2	NC	B23
GND	U14	NC	AC29	NC	B26
GND	U15	NC	AD1	NC	B4
GND	U16	NC	AD2	NC	B6
GND	U17	NC	AD30	NC	B8
GND	U18	NC	AE1	NC	C27
GND	U19	NC	AE15	NC	D1
GND	V1	NC	AE16	NC	D2
GND	V12	NC	AE2	NC	D29
GND	V13	NC	AE30	NC	D30
GND	V14	NC	AF1	NC	E1
GND	V15	NC	AF2	NC	E2
GND	V16	NC	AF29	NC	E29
GND	V17	NC	AF30	NC	E30
GND	V18	NC	AG1	NC	F15
GND	V19	NC	AG2	NC	F16
GND	V30	NC	AG29	NC	F29
GND	W12	NC	AG30	NC	F30
GND	W13	NC	AH27	NC	G1
GND	W14	NC	AH4	NC	G29
GND	W15	NC	AJ14	NC	G30
GND	W16	NC	AJ15	NC	H29
GND	W17	NC	AJ16	NC	J1
GND	W18	NC	AJ27	NC	J30

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO259NB6F24	AF7	IO276PB6F25	AD2	IO294NB6F27	V10
IO259PB6F24	AG7	IO277NB6F25	AC4	IO294PB6F27	V11
IO260NB6F24	AH3	IO277PB6F25	AC3	IO295NB6F27	Y1
IO260PB6F24	AH4	IO278NB6F26	AA8	IO295PB6F27	Y2
IO261NB6F24	AH5	IO278PB6F26	AA9	IO296NB6F27	W1
IO261PB6F24	AJ5	IO279NB6F26	AB5	IO296PB6F27	W2
IO262NB6F24	AE6	IO279PB6F26	AB6	IO297NB6F27	V1
IO262PB6F24	AF6	IO280NB6F26	Y10	IO297PB6F27	V2
IO263NB6F24	AF5	IO280PB6F26	Y11	IO298NB6F27	V9
IO263PB6F24	AG5	IO281NB6F26	AB3	IO298PB6F27	V8
IO264NB6F24	AD8	IO281PB6F26	AB4	IO299NB6F27	U4
IO264PB6F24	AE8	IO282NB6F26	Y7	IO299PB6F27	V4
IO265NB6F24	AF3	IO282PB6F26	AA7	Bank 7	
IO265PB6F24	AG3	IO283NB6F26	AC2	IO300NB7F28	U10
IO266NB6F24	AC10	IO283PB6F26	AC1	IO300PB7F28	U11
IO266PB6F24	AD10	IO284NB6F26	Y9	IO301NB7F28	U2
IO267NB6F25	AD7	IO284PB6F26	Y8	IO301PB7F28	U1
IO267PB6F25	AE7	IO285NB6F26	AA5	IO302NB7F28	U6
IO268NB6F25	AD5	IO285PB6F26	AA6	IO302PB7F28	U7
IO268PB6F25	AE5	IO286NB6F26	W10	IO303NB7F28	T3
IO269NB6F25	AE4	IO286PB6F26	W11	IO303PB7F28	U3
IO269PB6F25	AF4	IO287NB6F26	AA3	IO304NB7F28	U9
IO270NB6F25	AB9	IO287PB6F26	AA4	IO304PB7F28	U8
IO270PB6F25	AC9	IO288NB6F26	W9	IO305NB7F28	R2
IO271NB6F25	AC6	IO288PB6F26	W8	IO305PB7F28	R1
IO271PB6F25	AD6	IO289NB6F27	AA1	IO306NB7F28	R4
IO272NB6F25	AB8	IO289PB6F27	AA2	IO306PB7F28	T4
IO272PB6F25	AC8	IO290NB6F27	W6	IO307NB7F28	R5
IO273NB6F25	AE1	IO290PB6F27	Y6	IO307PB7F28	T5
IO273PB6F25	AE2	IO291NB6F27	W5	IO308NB7F28	T11
IO274NB6F25	AA10	IO291PB6F27	Y5	IO308PB7F28	T10
IO274PB6F25	AB10	IO292NB6F27	V7	IO309NB7F28	T6
IO275NB6F25	AB7	IO292PB6F27	W7	IO309PB7F28	T7
IO275PB6F25	AC7	IO293NB6F27	W4	IO310NB7F29	T9
IO276NB6F25	AD1	IO293PB6F27	Y4	IO310PB7F29	T8

PQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	Pin Number
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX250 Function	Pin Number
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

CQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

CQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ256	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	248
IO01PB0F0	249
IO04NB0F0	246
IO04PB0F0	247
IO05NB0F0	242
IO05PB0F0	243
IO08NB0F0	240
IO08PB0F0	241
Bank 0	
IO37NB0F3	234
IO37PB0F3	235
IO41NB0F3/HCLKAN	232
IO41PB0F3/HCLKAP	233
IO42NB0F3/HCLKBN	228
IO42PB0F3/HCLKBP	229
Bank 1 -	
IO43NB1F4/HCLKCN	220
IO43PB1F4/HCLKCP	221
IO44NB1F4/HCLKDN	216
IO44PB1F4/HCLKDP	217
Bank 1	
IO65NB1F6	210
IO65PB1F6	211
IO69NB1F6	208
IO69PB1F6	209
IO70NB1F6	199
IO71NB1F6	204
IO71PB1F6	205
IO73NB1F6	202
IO73PB1F6	203
IO74NB1F6	197
IO74PB1F6	198
Bank 2	
IO87NB2F8	187

CQ256	
AX2000 Function	Pin Number
IO87PB2F8	188
IO89PB2F8	186
Bank 2	
IO107NB2F10	184
IO107PB2F10	185
IO110NB2F10	180
IO110PB2F10	181
IO111NB2F10	178
IO111PB2F10	179
IO112NB2F10	174
IO112PB2F10	175
IO113NB2F10	172
IO113PB2F10	173
IO114NB2F10	168
IO114PB2F10	169
IO115NB2F10	166
IO115PB2F10	167
IO117NB2F10	162
IO117PB2F10	163
Bank 3	
IO139NB3F13	158
IO139PB3F13	159
IO141NB3F13	154
IO141PB3F13	155
IO142NB3F13	152
IO142PB3F13	153
IO145NB3F13	148
IO145PB3F13	149
IO146NB3F13	146
IO146PB3F13	147
IO147NB3F13	140
IO147PB3F13	141
IO148NB3F13	142
IO148PB3F13	143
IO149NB3F13	136

CQ256	
AX2000 Function	Pin Number
IO149PB3F13	137
Bank 3	
IO165NB3F15	135
IO167NB3F15	133
IO167PB3F15	134
Bank 4	
IO181NB4F17	124
IO181PB4F17	125
IO182NB4F17	122
IO182PB4F17	123
IO183NB4F17	118
IO183PB4F17	119
IO184NB4F17	116
IO184PB4F17	117
IO190NB4F17	112
IO190PB4F17	113
IO192NB4F17	110
IO192PB4F17	111
Bank 4	
IO212NB4F19/CLKEN	104
IO212PB4F19/CLKEP	105
IO213NB4F19/CLKFN	100
IO213PB4F19/CLKFP	101
Bank 5	
IO214NB5F20/CLKGN	92
IO214PB5F20/CLKGP	93
IO215NB5F20/CLKHN	88
IO215PB5F20/CLKHP	89
Bank 5	
IO236NB5F22	82
IO236PB5F22	83
IO238NB5F22	80
IO238PB5F22	81
IO240NB5F22	76
IO240PB5F22	77

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15