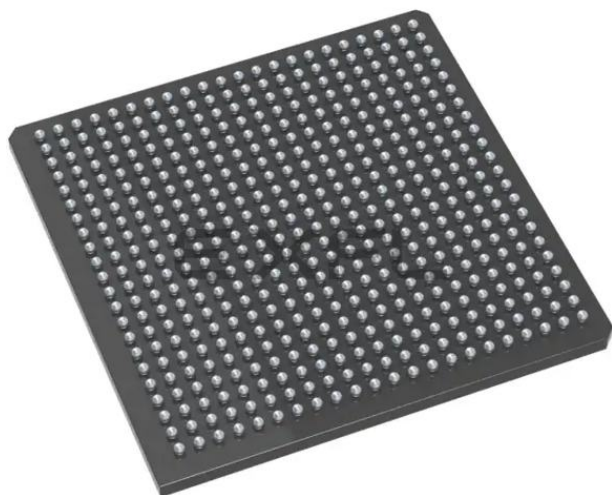




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-2fg484

Axcelerator Family Device Status

Axcelerator® Devices	Status
AX125	Production
AX250	Production
AX500	Production
AX1000	Production
AX2000	Production

Temperature Grade Offerings

Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	C, I, M	C, I, M	–	–
CQ208	–	M	M	–	–
CQ256	–	–	–	–	M
FG256	C, I	C, I, M	–	–	–
FG324	C, I	–	–	–	–
CQ352	–	M	M	M	M
FG484	–	C, I, M	C, I, M	C, I, M	–
CG624	–	–	–	M	M
FG676	–	–	C, I, M	C, I, M	–
BG729	–	–	–	C, I, M	–
FG896	–	–	–	C, I, M	C, I, M
FG1152	–	–	–	–	C, I, M

C = Commercial

I = Industrial

M = Military

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std	–1	–2
C	✓	✓	✓
I	✓	✓	✓
M	✓	✓	–

C = Commercial

I = Industrial

M = Military

1.8 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-26 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.2 VCCI	0.7 VCCI	3.6	0.2	VCCI - 0.2	8 mA	-8 mA

AC Loadings

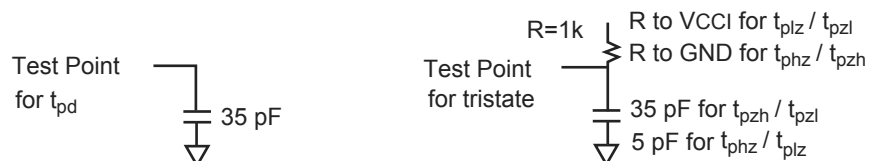


Figure 2-17 • AC Test Loads

Table 2-27 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	Cload (pF)
0	1.8	0.5 VCCI	N/A	35

Note: * Measuring Point = VTRIP

SSTL2

Stub Series Terminated Logic for 2.5 V is a general-purpose 2.5 V memory bus standard (JESD8-9). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-44 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF - 0.2	VREF + 0.2	3.6	VREF - 0.57	VREF + 0.57	7.6	-7.6

AC Loadings

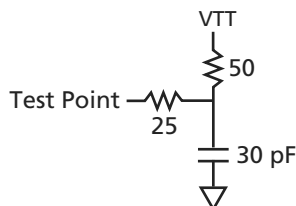


Figure 2-21 • AC Test Loads

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF - 0.75	VREF + 0.75	VREF	1.25	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-46 • 2.5 V SSTL2 Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		-2 Speed		-1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V SSTL2 Class I I/O Module Timing								
t _{DP}	Input Buffer		1.83		2.08		2.45	ns
t _{PY}	Output Buffer		2.39		2.72		3.20	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Model and Waveforms

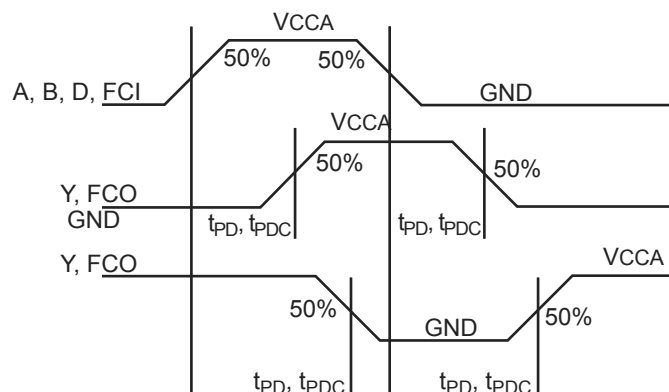


Figure 2-28 • C-Cell Timing Model and Waveforms

Timing Characteristics

Table 2-62 • C-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t _{PD}	Any input to output Y	0.74		0.84		0.99		ns
t _{PDC}	Any input to carry chain output (FCO)	0.57		0.64		0.76		ns
t _{PDB}	Any input through DB when one input is used	0.95		1.09		1.28		ns
t _{CCY}	Input to carry chain (FCI) to Y	0.61		0.69		0.82		ns
t _{CC}	Input to carry chain (FCI) to carry chain output (FCO)	0.08		0.09		0.11		ns

Table 2-72 • AX500 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.35		2.68		3.15	ns
t _{HCKH}	Input High to Low		2.44		2.79		3.27	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-73 • AX1000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-74 • AX2000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

PLLCLK and PLLHCLK

PLLCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 2-44).

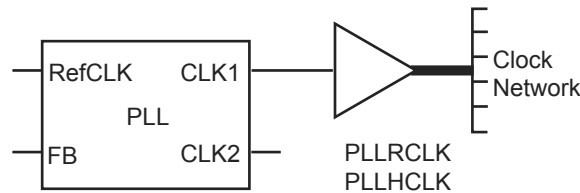


Figure 2-44 • PLLRCLK and PLLHCLK

Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc. (Figure 2-45).

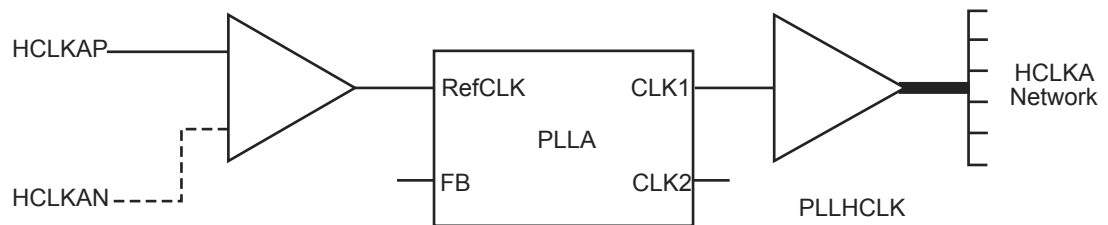


Figure 2-45 • Example of HCLKA Driven from a PLL with External Clock Source

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 2-46).

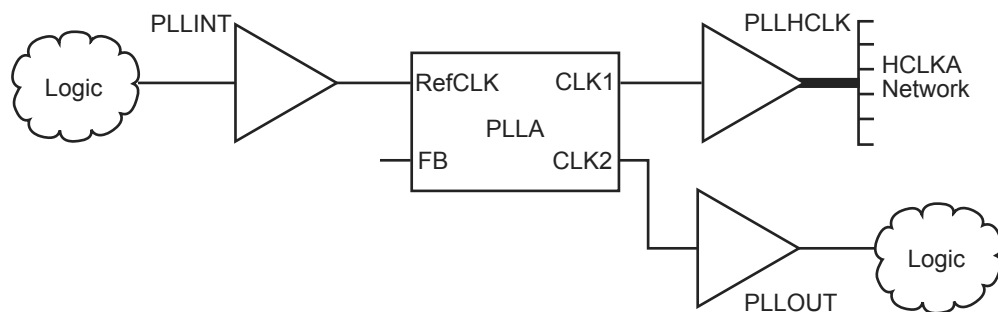


Figure 2-46 • Example of PLLINT and PLLOUT Usage

Table 2-102 • Sixteen FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		16.32		18.60		21.86	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		13.40		13.40		13.40	ns
t _{WCKP}	Minimum WCLK Period	14.15		14.15		14.15		ns
t _{RSU}	Read Setup		17.16		19.54		22.97	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		14.41		14.41		14.41	ns
t _{RCKP}	Minimum RCLK period	15.14		15.14		15.14		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		12.83		14.62		17.18	ns

Note: Timing data for these sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen Core Generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (refer to the *SmartGen*, *FlashROM*, *Analog System Builder*, and *Flash Memory System Builder* User's Guide for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Low Power Mode

Although designed for high performance, the AX architecture also allows the user to place the device into a low power mode. Each I/O bank in an Axcelerator device can be configured individually, when in low power mode, to tristate all outputs, disable inputs, or both. The low power mode is activated by asserting the LP pin, which is grounded in normal operation.

While in the low power mode, the device is still fully functional and all internal logic states are preserved. This allows a user to disable all but a few signals and operate the part in a low-frequency, watchdog

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0					
IO00NB0F0	E6	IO18NB0F1	C10	IO36NB1F3	H15
IO00PB0F0	F6	IO18PB0F1	C9	IO36PB1F3	G15
IO01NB0F0	G8	IO19NB0F1	E11	IO37NB1F3	C17
IO01PB0F0	G7	IO19PB0F1	F11	IO37PB1F3	C16
IO02NB0F0	D7	IO20NB0F1	G12	IO38NB1F3	B18
IO02PB0F0	E7	IO20PB0F1	H12	IO38PB1F3	B17
IO03NB0F0	D5	IO21NB0F1	D11	IO39NB1F3	A18
IO03PB0F0	E5	IO21PB0F1	D10	IO39PB1F3	A17
IO04NB0F0	G9	IO22NB0F2	A10	IO40NB1F3	H16
IO04PB0F0	H9	IO22PB0F2	A9	IO40PB1F3	G16
IO05NB0F0	E8	IO23NB0F2	B11	IO41NB1F4	B19
IO05PB0F0	F8	IO23PB0F2	B10	IO41PB1F4	A19
IO06NB0F0	C6	IO24NB0F2	G13	IO42NB1F4	C19
IO06PB0F0	D6	IO24PB0F2	H13	IO42PB1F4	C18
IO07NB0F0	B5	IO25NB0F2	C12	IO43NB1F4	D18
IO07PB0F0	C5	IO25PB0F2	C11	IO43PB1F4	D17
IO08NB0F0	A6	IO26NB0F2	E12	IO44NB1F4	H17
IO08PB0F0	A5	IO26PB0F2	D12	IO44PB1F4	G17
IO09NB0F0	E9	IO27NB0F2	E13	IO45NB1F4	F17
IO09PB0F0	F9	IO27PB0F2	F13	IO45PB1F4	E17
IO10NB0F0	G10	IO28NB0F2	G14	IO46NB1F4	B20
IO10PB0F0	H10	IO28PB0F2	H14	IO46PB1F4	A20
IO11NB0F0	B7	IO29NB0F2	A12	IO47NB1F4	C21
IO11PB0F0	B6	IO29PB0F2	B12	IO47PB1F4	C20
IO12NB0F1	C8	IO30NB0F2/HCLKAN	C13	IO48NB1F4	H18
IO12PB0F1	C7	IO30PB0F2/HCLKAP	D13	IO48PB1F4	G18
IO13NB0F1	E10	IO31NB0F2/HCLKBN	F14	IO49NB1F4	F18
IO13PB0F1	F10	IO31PB0F2/HCLKBP	E14	IO49PB1F4	E18
IO14NB0F1	G11	Bank 1		IO50NB1F4	D20
IO14PB0F1	H11	IO32NB1F3/HCLKCN	C14	IO50PB1F4	D19
IO15NB0F1	D9	IO32PB1F3/HCLKCP	B14	IO51NB1F4	A22
IO15PB0F1	D8	IO33NB1F3/HCLKDN	D16	IO51PB1F4	A21
IO16NB0F1	A8	IO33PB1F3/HCLKDP	D15	IO52NB1F4	B22
IO16PB0F1	A7	IO34NB1F3	B16	IO52PB1F4	B21
IO17NB0F1	B9	IO34PB1F3	A16	IO53NB1F4	F19
IO17PB0F1	B8	IO35NB1F3	E15	IO53PB1F4	E19
		IO35PB1F3	F15	IO54NB1F5	F20

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 6		IO81NB7F7	C2	GND	M12
IO60NB6F6	L4	IO81PB7F7	B1	GND	M5
IO60PB6F6	M4	IO82NB7F7	D2	GND	P13
IO61NB6F6	L3	IO82PB7F7	D3	GND	P3
IO61PB6F6	M3	IO83NB7F7	E3	GND	R15
IO63NB6F6	P2	IO83PB7F7	F3	GND	R2
IO63PB6F6	N2	Dedicated I/O		GND	T1
IO64NB6F6	J4	VCCDA	E4	GND	T16
IO64PB6F6	K4	GND	A1	GND/LP	D4
IO65NB6F6	N1	GND	A16	NC	A11
IO65PB6F6	P1	GND	B15	NC	R11
IO67NB6F6	L2	GND	B2	NC	R5
IO67PB6F6	M2	GND	D15	PRA	D8
IO69NB6F6	L1	GND	E12	PRB	C8
IO69PB6F6	M1	GND	E5	PRC	N9
IO70NB6F6	J3	GND	F11	PRD	P9
IO70PB6F6	K3	GND	F6	TCK	D5
IO71NB6F6	J2	GND	G10	TDI	C6
IO71PB6F6	K2	GND	G7	TDO	C4
Bank 7		GND	G8	TMS	C3
IO72NB7F7	J1	GND	G9	TRST	C5
IO72PB7F7	K1	GND	H10	VCCA	D14
IO73NB7F7	G2	GND	H7	VCCA	F10
IO73PB7F7	H2	GND	H8	VCCA	F4
IO74NB7F7	G3	GND	H9	VCCA	F7
IO74PB7F7	H3	GND	J10	VCCA	F8
IO75NB7F7	E1	GND	J7	VCCA	F9
IO75PB7F7	F1	GND	J8	VCCA	G11
IO76NB7F7	G1	GND	J9	VCCA	G6
IO77NB7F7	E2	GND	K10	VCCA	H11
IO77PB7F7	F2	GND	K7	VCCA	H6
IO78NB7F7	G4	GND	K8	VCCA	J11
IO78PB7F7	H4	GND	K9	VCCA	J6
IO79NB7F7	C1	GND	L11	VCCA	K11
IO79PB7F7	D1	GND	L6	VCCA	K6

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
Bank 0		IO17NB1F1	B14	IO34PB2F2	D22
IO00NB0F0	D7	IO17PB1F1	B13	IO35NB2F2	J18
IO00PB0F0	D6	IO18NB1F1	A14	IO35PB2F2	H18
IO01NB0F0	E7	IO18PB1F1	A13	IO36NB2F2	G21
IO01PB0F0	E6	IO19NB1F1	A16	IO36PB2F2	F21
IO02NB0F0	C5	IO19PB1F1	A15	IO37NB2F2	K19
IO02PB0F0	C4	IO20NB1F1	B16	IO37PB2F2	J19
IO03NB0F0	C7	IO20PB1F1	B15	IO38NB2F2	J20
IO03PB0F0	C6	IO21NB1F1	C17	IO38PB2F2	H20
IO04NB0F0	E9	IO21PB1F1	C16	IO39NB2F2	L16
IO04PB0F0	E8	IO22NB1F1	F15	IO39PB2F2	K16
IO05NB0F0	D9	IO22PB1F1	F14	IO40NB2F2	J21
IO05PB0F0	D8	IO23NB1F1	D16	IO40PB2F2	H21
IO06NB0F0	B7	IO23PB1F1	D15	IO41NB2F2	L17
IO06PB0F0	B6	IO24NB1F1	E16	IO41PB2F2	K17
IO07NB0F0	C9	IO24PB1F1	E15	IO42NB2F2	J22
IO07PB0F0	C8	IO25NB1F1	F18	IO42PB2F2	H22
IO08NB0F0	A7	IO25PB1F1	F17	IO43NB2F2	L18
IO08PB0F0	A6	IO26NB1F1	D18	IO43PB2F2	K18
IO09NB0F0	B9	IO26PB1F1	E17	IO44NB2F2	L20
IO09PB0F0	B8	IO27NB1F1	G16	IO44PB2F2	K20
IO10NB0F0	A9	IO27PB1F1	G15	Bank 3	
IO10PB0F0	A8	Bank 2		IO45NB3F3	M19
IO11NB0F0	B10	IO28NB2F2	F19	IO45PB3F3	L19
IO11PB0F0	A10	IO28PB2F2	E19	IO46NB3F3	M21
IO12NB0F0/HCLKAN	E11	IO29NB2F2	J16	IO46PB3F3	L21
IO12PB0F0/HCLKAP	E10	IO29PB2F2	H16	IO47NB3F3	N17
IO13NB0F0/HCLKBN	D12	IO30NB2F2	E20	IO47PB3F3	M17
IO13PB0F0/HCLKBP	D11	IO30PB2F2	D20	IO48NB3F3	N18
Bank 1		IO31NB2F2	J17	IO48PB3F3	N19
IO14NB1F1/HCLKCN	F13	IO31PB2F2	H17	IO49NB3F3	N16
IO14PB1F1/HCLKCP	F12	IO32NB2F2	G20	IO49PB3F3	M16
IO15NB1F1/HCLKDN	E14	IO32PB2F2	F20	IO50NB3F3	N20
IO15PB1F1/HCLKDP	E13	IO33NB2F2	H19	IO50PB3F3	M20
IO16NB1F1	C13	IO33PB2F2	G19	IO51NB3F3	P21
IO16PB1F1	C12	IO34NB2F2	E22	IO51PB3F3	N21

FG484	
AX1000 Function	Pin Number
Bank 0	
IO01NB0F0	E3
IO01PB0F0	D3
IO02NB0F0	E7
IO02PB0F0	E6
IO05NB0F0	D2
IO05PB0F0	E2
IO06NB0F0	C5
IO06PB0F0	C4
IO12NB0F1	D7
IO12PB0F1	D6
IO13NB0F1	B5
IO13PB0F1	B4
IO14NB0F1	E9
IO14PB0F1	E8
IO15NB0F1	C7
IO15PB0F1	C6
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	B7
IO17PB0F1	B6
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	C9
IO19PB0F1	C8
IO20NB0F1	D9
IO20PB0F1	D8
IO21NB0F1	B9
IO21PB0F1	B8
IO22NB0F2	A9
IO22PB0F2	A8
IO23NB0F2	B10
IO23PB0F2	A10
IO26NB0F2	A14
IO26PB0F2	A13

FG484	
AX1000 Function	Pin Number
IO29NB0F2	B12
IO29PB0F2	B11
IO30NB0F2/HCLKAN	E11
IO30PB0F2/HCLKAP	E10
IO31NB0F2/HCLKBN	D12
IO31PB0F2/HCLKBP	D11
Bank 1	
IO32NB1F3/HCLKCN	F13
IO32PB1F3/HCLKCP	F12
IO33NB1F3/HCLKDN	E14
IO33PB1F3/HCLKDP	E13
IO34NB1F3	C13
IO34PB1F3	C12
IO37NB1F3	B14
IO37PB1F3	B13
IO38NB1F3	A16
IO38PB1F3	A15
IO40NB1F3	C15
IO42NB1F4	A18
IO42PB1F4	A17
IO43NB1F4	B16
IO43PB1F4	B15
IO44NB1F4	B18
IO44PB1F4	B17
IO45NB1F4	B19
IO45PB1F4	A19
IO46NB1F4	C19
IO46PB1F4	C18
IO48NB1F4	F15
IO48PB1F4	F14
IO49NB1F4	D16
IO49PB1F4	D15
IO50NB1F4	C17
IO50PB1F4	C16
IO51NB1F4	E22

FG484	
AX1000 Function	Pin Number
IO51PB1F4	D22
IO52NB1F4	E16
IO52PB1F4	E15
IO57NB1F5	E21
IO57PB1F5	D21
IO60NB1F5	G16
IO60PB1F5	G15
IO61NB1F5	D18
IO61PB1F5	E17
IO63NB1F5	E20
IO63PB1F5	D20
Bank 2	
IO64NB2F6	F18
IO64PB2F6	F17
IO67NB2F6	F19
IO67PB2F6	E19
IO68NB2F6	J16
IO68PB2F6	H16
IO70NB2F6	J17
IO70PB2F6	H17
IO74NB2F7	J18
IO74PB2F7	H18
IO75NB2F7	G20
IO75PB2F7	F20
IO79NB2F7	H19
IO79PB2F7	G19
IO80NB2F7	L16
IO80PB2F7	K16
IO84NB2F7	L17
IO84PB2F7	K17
IO85NB2F8	G21
IO85PB2F8	F21
IO86NB2F8	G22
IO86PB2F8	F22
IO87NB2F8	J20

FG484	
AX1000 Function	Pin Number
IO167PB5F15	AA12
IO169NB5F15	AA9
IO169PB5F15	AA10
IO170NB5F15	AB9
IO170PB5F15	AB10
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	Y8
IO172PB5F16	Y9
IO173NB5F16	U8
IO173PB5F16	U9
IO174NB5F16	AA7
IO174PB5F16	AA8
IO175NB5F16	AB5
IO175PB5F16	AB6
IO176NB5F16	AA5
IO176PB5F16	AA6
IO177NB5F16	AA4
IO177PB5F16	AB4
IO178NB5F16	Y6
IO178PB5F16	Y7
IO179NB5F16	T7
IO179PB5F16	T8
IO180NB5F16	W6
IO180PB5F16	W7
IO181NB5F17	Y4
IO181PB5F17	Y5
IO184NB5F17	AB7
IO187NB5F17	V3
IO187PB5F17	W3
IO188NB5F17	V4
IO188PB5F17	W5
IO192NB5F17	V6
IO192PB5F17	V7
Bank 6	

FG484	
AX1000 Function	Pin Number
IO194NB6F18	V2
IO194PB6F18	W2
IO195NB6F18	U5
IO195PB6F18	T5
IO200NB6F18	T4
IO200PB6F18	U4
IO201NB6F18	P6
IO201PB6F18	R6
IO203NB6F19	U2
IO204NB6F19	T3
IO204PB6F19	U3
IO205NB6F19	P5
IO205PB6F19	R5
IO208NB6F19	V1
IO208PB6F19	W1
IO209NB6F19	P7
IO209PB6F19	R7
IO212NB6F19	P4
IO212PB6F19	R4
IO214NB6F20	P3
IO214PB6F20	R3
IO215NB6F20	M6
IO215PB6F20	N6
IO216NB6F20	R2
IO216PB6F20	T2
IO217NB6F20	T1
IO217PB6F20	U1
IO219NB6F20	M5
IO219PB6F20	N5
IO220NB6F20	P1
IO220PB6F20	R1
IO221NB6F20	N2
IO221PB6F20	P2
IO222NB6F20	M3
IO222PB6F20	N3

FG484	
AX1000 Function	Pin Number
IO223NB6F20	M7
IO223PB6F20	N7
IO224NB6F20	M4
IO224PB6F20	N4
Bank 7	
IO225NB7F21	M2
IO225PB7F21	N1
IO226NB7F21	K2
IO226PB7F21	K1
IO228NB7F21	L3
IO228PB7F21	L2
IO229NB7F21	K5
IO229PB7F21	L5
IO230NB7F21	H1
IO230PB7F21	J1
IO231NB7F21	H2
IO231PB7F21	J2
IO232NB7F21	K4
IO232PB7F21	K3
IO233NB7F21	K6
IO233PB7F21	L6
IO234NB7F21	F1
IO234PB7F21	G1
IO235NB7F21	F2
IO235PB7F21	G2
IO236NB7F22	H3
IO236PB7F22	J3
IO237NB7F22	K7
IO237PB7F22	L7
IO241NB7F22	H6
IO241PB7F22	J6
IO242NB7F22	H4
IO242PB7F22	J4
IO243NB7F22	H5
IO243PB7F22	J5

FG676	
AX500 Function	Pin Number
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8

FG676	
AX500 Function	Pin Number
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

FG676	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10

FG676	
AX1000 Function	Pin Number
IO21PB0F1	C10
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
Bank 1	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20

FG676	
AX1000 Function	Pin Number
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20
IO52PB1F4	C20
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
Bank 2	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

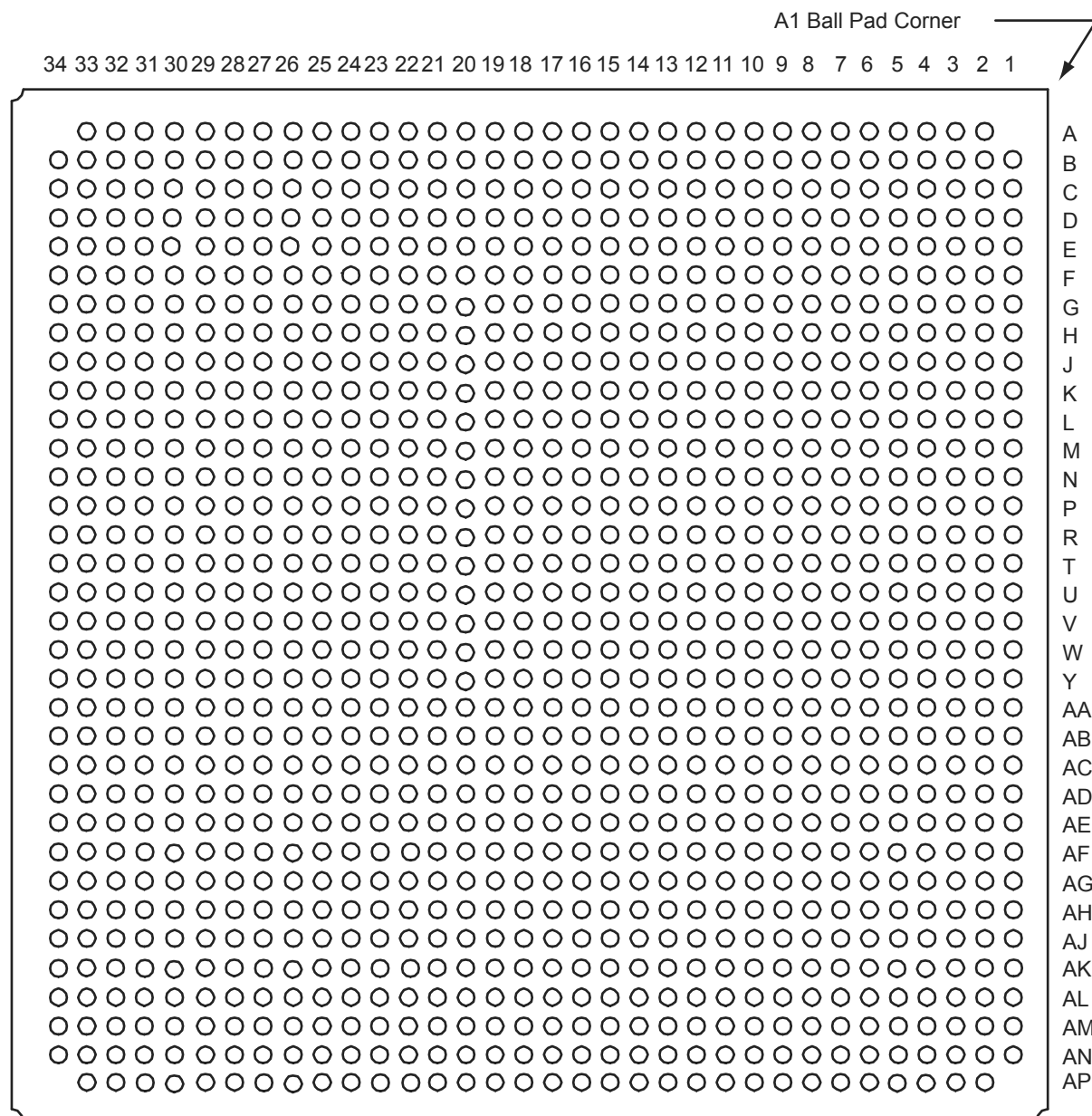
FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO51PB1F4	E21	IO68PB2F6	K24	IO86NB2F8	N28
IO52NB1F4	F22	IO69NB2F6	F27	IO86PB2F8	N27
IO52PB1F4	E22	IO69PB2F6	E27	IO87NB2F8	P29
IO53NB1F4	B25	IO70NB2F6	J26	IO87PB2F8	P30
IO53PB1F4	B24	IO70PB2F6	J25	IO88NB2F8	P25
IO54NB1F5	D24	IO71NB2F6	H27	IO88PB2F8	P24
IO54PB1F5	D23	IO71PB2F6	G27	IO89NB2F8	P28
IO55NB1F5	F23	IO72NB2F6	J28	IO89PB2F8	P27
IO55PB1F5	E23	IO72PB2F6	H28	IO90NB2F8	P22
IO56NB1F5	H21	IO73NB2F6	G28	IO90PB2F8	P23
IO56PB1F5	G21	IO73PB2F6	F28	IO91NB2F8	R26
IO57NB1F5	D25	IO74NB2F7	L23	IO91PB2F8	P26
IO57PB1F5	C25	IO74PB2F7	L24	IO92NB2F8	R24
IO58NB1F5	F24	IO75NB2F7	L26	IO92PB2F8	R25
IO58PB1F5	E24	IO75PB2F7	K26	IO93NB2F8	R29
IO59NB1F5	D26	IO76NB2F7	M25	IO93PB2F8	R30
IO59PB1F5	C26	IO76PB2F7	L25	IO94NB2F8	R22
IO60NB1F5	G23	IO77NB2F7	K27	IO94PB2F8	R23
IO60PB1F5	G22	IO77PB2F7	J27	IO95NB2F8	T27
IO61NB1F5	B27	IO78NB2F7	M27	IO95PB2F8	R27
IO61PB1F5	A27	IO78PB2F7	L27	Bank 3	
IO62NB1F5	F25	IO79NB2F7	K30	IO96NB3F9	T29
IO62PB1F5	E25	IO79PB2F7	K29	IO96PB3F9	T30
IO63NB1F5	H23	IO80NB2F7	M23	IO97NB3F9	U29
IO63PB1F5	H22	IO80PB2F7	M24	IO97PB3F9	U30
Bank 2		IO81NB2F7	M28	IO98NB3F9	T22
IO64NB2F6	K23	IO81PB2F7	L28	IO98PB3F9	T23
IO64PB2F6	J23	IO82NB2F7	N26	IO99NB3F9	U26
IO65NB2F6	J24	IO82PB2F7	M26	IO99PB3F9	T26
IO65PB2F6	H24	IO83NB2F7	N25	IO100NB3F9	U24
IO66NB2F6	H26	IO83PB2F7	N24	IO100PB3F9	T24
IO66PB2F6	H25	IO84NB2F7	N22	IO101NB3F9	V28
IO67NB2F6	G26	IO84PB2F7	N23	IO101PB3F9	U28
IO67PB2F6	G25	IO85NB2F8	M29	IO102NB3F9	U23
IO68NB2F6	K25	IO85PB2F8	L29	IO102PB3F9	U22

FG896	
AX2000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX2000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	Pin Number
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

FG1152



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO51PB1F4	J20	IO69NB1F6	C27	IO86NB2F8	J28
IO52NB1F4	B20	IO69PB1F6	C26	IO86PB2F8	J27
IO52PB1F4	A20	IO70NB1F6	H24	IO87NB2F8	M25
IO53NB1F4	F20	IO70PB1F6	G24	IO87PB2F8	L25
IO53PB1F4	E20	IO71NB1F6	H23	IO88NB2F8	L26
IO54NB1F5	B21	IO71PB1F6	G23	IO88PB2F8	K26
IO54PB1F5	A21	IO72NB1F6	B28	IO89NB2F8	G31
IO55NB1F5	K21	IO72PB1F6	A28	IO89PB2F8	F31
IO55PB1F5	J21	IO73NB1F6	E26	IO90NB2F8	H29
IO56NB1F5	D21	IO73PB1F6	E25	IO90PB2F8	G29
IO56PB1F5	C21	IO74NB1F6	F26	IO91NB2F8	K28
IO57NB1F5	G22	IO74PB1F6	F25	IO91PB2F8	K27
IO57PB1F5	G21	IO75NB1F6	K25	IO92NB2F8	J30
IO58NB1F5	E22	IO75PB1F6	K24	IO92PB2F8	H30
IO58PB1F5	E21	IO76NB1F7	D27	IO93NB2F8	L28
IO59NB1F5	D22	IO76PB1F7	D26	IO93PB2F8	L27
IO59PB1F5	C22	IO77NB1F7	B29	IO94NB2F8	K29
IO60NB1F5	B23	IO77PB1F7	A29	IO94PB2F8	J29
IO60PB1F5	A23	IO78NB1F7	D28	IO95NB2F8	K31
IO61NB1F5	H22	IO78PB1F7	C28	IO95PB2F8	J31
IO61PB1F5	H21	IO79NB1F7	H25	IO96NB2F9	J32
IO62NB1F5	C24	IO79PB1F7	G25	IO96PB2F9	H32
IO62PB1F5	C23	IO80NB1F7	F27	IO97NB2F9	M27
IO63NB1F5	F23	IO80PB1F7	E27	IO97PB2F9	M26
IO63PB1F5	F22	IO81NB1F7	J25	IO98NB2F9	L30
IO64NB1F6	B24	IO81PB1F7	J24	IO98PB2F9	K30
IO64PB1F6	A24	IO82NB1F7	D29	IO99NB2F9	N25
IO65NB1F6	J22	IO82PB1F7	C29	IO99PB2F9	N26
IO65PB1F6	K22	IO83NB1F7	H26	IO100NB2F9	M29
IO66NB1F6	B25	IO83PB1F7	G26	IO100PB2F9	L29
IO66PB1F6	A25	IO84NB1F7	F28	IO101NB2F9	L33
IO67NB1F6	K23	IO84PB1F7	E28	IO101PB2F9	L32
IO67PB1F6	J23	IO85NB1F7	H27	IO102NB2F9	K34
IO68NB1F6	F24	IO85PB1F7	G27	IO102PB2F9	K33
IO68PB1F6	E24	Bank 2		IO103NB2F9	N28

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 18 (March 2012)	Table 2-1 • Absolute Maximum Ratings was updated to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419).	2-1
	Values for tristate leakage current IOZ, and I _{IH} and I _{IL} were added to Table 2-3 • Standby Current (SARs 35774, 32021).	2-2
	Figure 2-2 • VCCPLX and VCOMPLX Power Supply Connect was updated to correct the units for the resistance from "W" to Ω (SAR 36415).	2-9
	In the Introduction to the "User I/Os" section, the following sentence was added to clarify the slew rate setting (SAR 34943): The slew rate setting is effective for both rising and falling edges.	2-11
	Figure 2-3 • Use of an External Resistor for 5 V Tolerance was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942).	2-13
	EQ 3 for 5 V tolerance was corrected to change V _{diode} from 0.6 V to 0.7 V (SAR 36786).	2-13
	Additional information was added to the "Using the Weak Pull-Up and Pull-Down Circuits" section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945).	2-17
	The description for the C _{INCLK} parameter in Table 2-18 • Input Capacitance was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944).	2-21
	Table 2-19 • I/O Input Rise Time and Fall Time* is new (SAR 34942).	2-21
	The minimum V _{IL} for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-29 • DC Input and Output Levels and Table 2-33 • DC Input and Output Levels (SAR 34358).	2-38, 2-40
	Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the <i>Antifuse Macro Library Guide</i> was added to the "R-Cell" section (SAR 26413).	2-58
Revision 17 (September 2011)	The enable signal in Figure 2-32 • R-Cell Delays was corrected to show it is active low rather than active high (SAR 34946).	2-59
	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Axcelerator Family Device Status" table indicates the status for each device in the device family.	iii
	The "Features" section, "Programmable Interconnect Element" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865).	i, 1-1, 2-108