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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-2fg484i

Figure 1-2 • Axcelerator Family Interconnect Elements

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

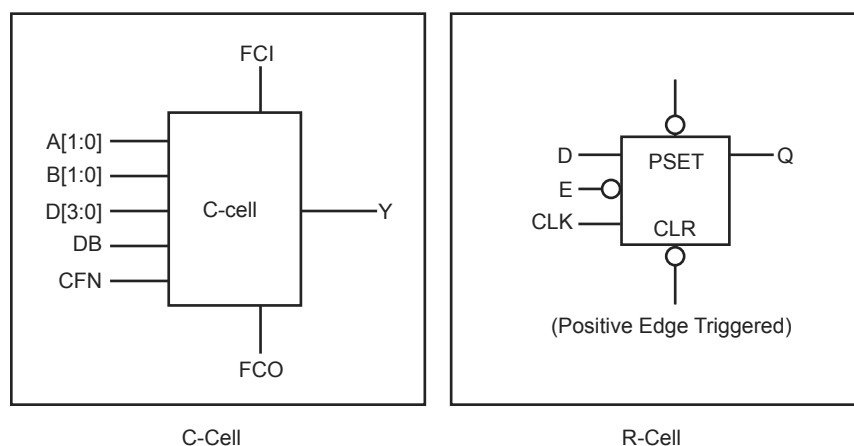


Figure 1-3 • AX C-Cell and R-Cell

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).

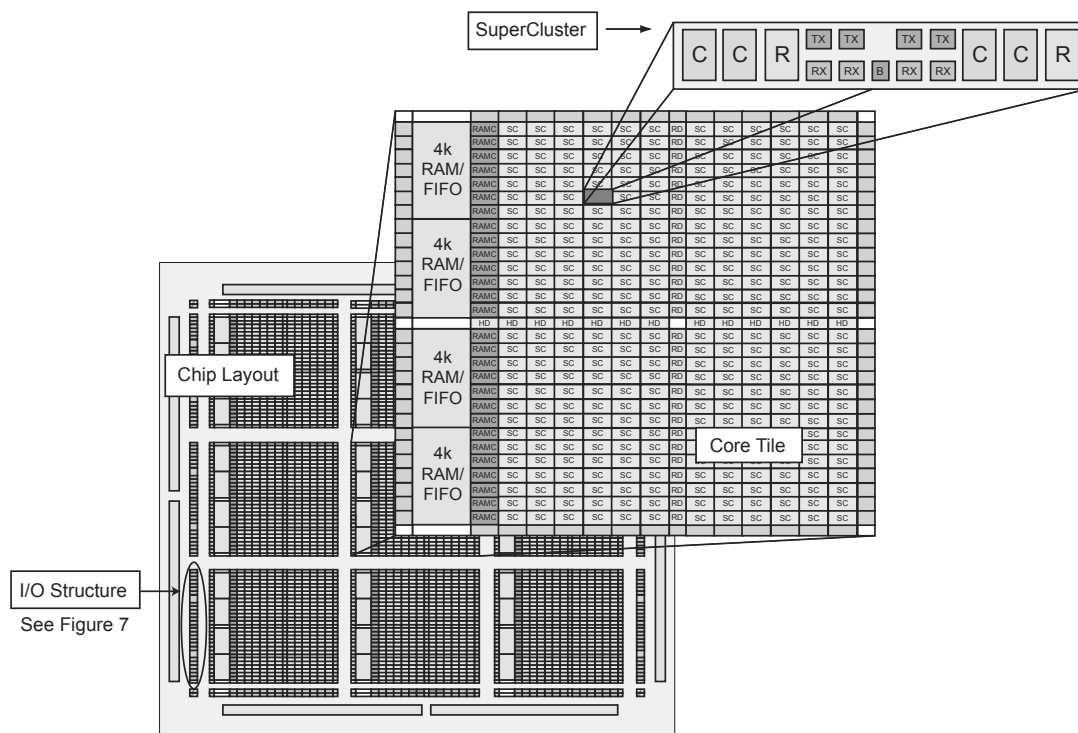


Figure 1-6 • AX Device Architecture (AX1000 shown)

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

Calculating Power Dissipation

Table 2-3 • Standby Current

Device	Temperature	ICCA	ICCD A	ICCBANK		ICCP LL	ICCCP ¹		IIH, IIL, IOZ ²	Units
		Standby Current (Core)	Standby Current, Differential I/O	Standby Current per I/O Bank		Standby Current per PLL	Standby Current, Charge Pump			
				2.5 V VCCI	3.3 V VCCI		Active	Bypassed Mode		
AX125	Typical at 25°C	1.5	1.5	0.2	0.3	0.2	0.3	0.01	±0.01	mA
	70°C	15	6	0.5	0.75	1	0.4	0.01	±0.01	mA
	85°C	25	6	0.6	0.8	1	0.4	0.2	±0.01	mA
	125°C	50	8	1	1.5	2	0.4	0.5	±0.01	mA
AX250	Typical at 25°C	1.5	1.4	0.25	0.4	0.2	0.3	0.01	±0.01	mA
	70°C	30	7	0.8	0.9	1	0.4	0.01	±0.01	mA
	85°C	40	7	0.8	1	1	0.4	0.2	±0.01	mA
	125°C	70	9	1.3	1.8	2	0.4	0.5	±0.01	mA
AX500	Typical at 25°C	5	1.4	0.4	0.75	0.2	0.3	0.01	±0.01	mA
	70°C	60	7	1	1.5	1	0.4	0.01	±0.01	mA
	85°C	80	7	1	1.9	1	0.4	0.2	±0.01	mA
	125°C	180	9	1.75	2.5	1.5	0.4	0.5	±0.01	mA
AX1000	Typical at 25°C	7.5	1.5	0.5	1.25	0.2	0.3	0.01	±0.01	mA
	70°C	80	8	1.5	3	1	0.4	0.01	±0.01	mA
	85°C	120	8	1.5	3.4	1	0.4	0.2	±0.01	mA
	125°C	200	10	3	4	1.5	0.4	0.5	±0.01	mA
AX2000	Typical at 25°C	20	1.6	0.7	1.5	0.2	0.3	0.01	±0.01	mA
	70°C	160	10	2	7	1	0.4	0.01	±0.01	mA
	85°C	200	10	3	8	1	0.4	0.2	±0.01	mA
	125°C	500	15	4	10	1.5	0.4	0.5	±0.01	mA

Notes:

1. ICCCP Active is the ICCDA or the Internal Charge Pump current. ICCCP Bypassed mode is the External Charge Pump current IIH (VPUMP pin).
2. IIH, IIL, or IOZ values are measured with inputs at the same level as VCCI for IIH and GND for IIL and IOZ.

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

Table 2-11 • Compatible I/O Standards for Different VREF Values

VREF	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5V and 3.3V Outputs)
0.75 V	HSTL (Class I)

Table 2-12 • Compatible I/O Standards for Different VCCI Values

VCCI ¹	Compatible Standards	VREF
3.3 V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVC MOS 2.5 V, GTL+ 2.5 V, LVDS ²	1.0
2.5 V	LVC MOS 2.5 V, SSTL 2 (Classes I and II), LVDS ²	1.25
1.8 V	LVC MOS 1.8 V	N/A
1.5 V	LVC MOS 1.5 V, HSTL Class I	0.75

Notes:

1. VCCI is used for both inputs and outputs
2. VCCI tolerance is $\pm 5\%$

Table 2-13 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank.

Table 2-13 • Legal I/O Usage Matrix

I/O Standard	LVTTTL 3.3 V	LVC MOS 2.5 V	LVC MOS 1.8 V	LVC MOS 1.5 V (JESD8-11)	3.3V PCI/PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	HSTL Class I (1.5V)	SSTL2 Class I & II (2.5 V)	SSTL3 Class I & II (3.3 V)	LVDS (2.5 V)	LVPECL (3.3 V)
LVTTTL 3.3 V (VREF=1.0 V)	✓	-	-	-	✓	✓	-	-	-	-	-	✓
LVTTTL 3.3 V (VREF=1.5 V)	✓	-	-	-	✓	-	-	-	-	✓	-	✓
LVC MOS 2.5 V (VREF=1.0 V)	-	✓	-	-	-	-	✓	-	-	-	✓	-
LVC MOS 2.5 V (VREF=1.25V)	-	✓	-	-	-	-	-	-	✓	-	✓	-
LVC MOS 1.8 V	-	-	✓	-	-	-	-	-	-	-	-	-
LVC MOS 1.5 V (VREF = 1.75 V) (JESD8-11)	-	-	-	✓	-	-	-	✓	-	-	-	-
3.3 V PCI/PCI-X (VREF = 1.0 V)	✓	-	-	-	✓	✓	-	-	-	-	-	✓
3.3 V PCI/PCI-X (VREF= 1.5 V)	✓	-	-	-	✓	-	-	-	-	✓	-	✓
GTL + (3.3 V)	✓	-	-	-	✓	✓	-	-	-	-	-	✓
GTL + (2.5 V)	-	✓	-	-	-	-	✓	-	-	-	-	-
HSTL Class I	-	-	-	✓	-	-	-	✓	-	-	-	-
SSTL2 Class I & II	-	✓	-	-	-	-	-	-	✓	-	✓	-
SSTL3 Class I & II	✓	-	-	-	✓	-	-	-	-	✓	-	✓
LVDS (VREF = 1.0 V)	-	✓	-	-	-	-	✓	-	-	-	✓	-
LVDS (VREF = 1.25 V)	-	✓	-	-	-	-	-	-	✓	-	✓	-
LVPECL (VREF = 1.0 V)	✓	-	-	-	✓	✓	-	-	-	-	-	✓
LVPECL (VREF = 1.5 V)	✓	-	-	-	✓	-	-	-	-	✓	-	✓

Notes:

1. Note that GTL+ 2.5 V is not supported across the full military temperature range.
2. A "✓" indicates whether standards can be used within a bank at the same time.

Examples:

- a) LVTTTL can be used with 3.3V PCI and GTL+ (3.3V), when $V_{REF} = 1.0V$ (GTL+ requirement).
- b) LVTTTL can be used with 3.3V PCI and SSTL3 Class I and II, when $V_{REF} = 1.5V$ (SSTL3 requirement).

Note that two I/O standards are compatible if:

- Their VCCI values are identical.
- Their VREF standards are identical (if applicable).

For example, if LVTTTL 3.3 V (VREF= 1.0 V) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTTL 3.3 V PCI/PCI-X, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank.

Timing Characteristics

Table 2-28 • 1.8V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.7 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS18 Output Module Timing								
t _{DP}	Input Buffer		3.26		3.71		4.37	ns
t _{PY}	Output Buffer		4.55		5.18		6.09	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.82		2.83		2.84	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.43		3.45		3.46	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.01		6.85		8.05	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.73		7.67		9.01	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t _{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t _{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t _{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t _{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t _{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t _{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t _{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t _{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t _{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t _{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t _{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t _{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t _{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t _{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t _{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t _{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t _{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t _{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-69 • AX2000 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.50	0.56	0.66	ns
t _{RD2}	Routing delay for FO2	0.59	0.67	0.79	ns
t _{RD3}	Routing delay for FO3	0.70	0.80	0.94	ns
t _{RD4}	Routing delay for FO4	0.76	0.87	1.02	ns
t _{RD5}	Routing delay for FO5	0.98	1.11	1.31	ns
t _{RD6}	Routing delay for FO6	1.48	1.68	1.97	ns
t _{RD7}	Routing delay for FO7	1.65	1.87	2.20	ns
t _{RD8}	Routing delay for FO8	1.73	1.96	2.31	ns
t _{RD16}	Routing delay for FO16	2.58	2.92	3.44	ns
t _{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-75 • AX125 Routed Array Clock Networks

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-76 • AX250 Routed Array Clock Networks

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t _{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO163PB5F15	AA14	IO182NB5F17	AF7	IO200NB6F18	AA4
IO164NB5F15	AE13	IO182PB5F17	AG7	IO200PB6F18	AA5
IO164PB5F15	AF13	IO183NB5F17	AD7	IO201NB6F18	W5
IO165NB5F15	AF12	IO183PB5F17	AE7	IO201PB6F18	W6
IO165PB5F15	AG12	IO184NB5F17	AC7	IO202NB6F18	AB1
IO166NB5F15	AD12	IO184PB5F17	AC8	IO202PB6F18	AC1
IO166PB5F15	AE12	IO185NB5F17	AF6	IO203NB6F19	Y3
IO167NB5F15	Y13	IO185PB5F17	AG6	IO203PB6F19	AA3
IO167PB5F15	AA13	IO186NB5F17	AB7	IO204NB6F19	AA2
IO168NB5F15	AD11	IO186PB5F17	AB8	IO204PB6F19	AB2
IO168PB5F15	AE11	IO187NB5F17	Y9	IO205NB6F19	U8
IO169NB5F15	AG11	IO187PB5F17	AA9	IO205PB6F19	V8
IO169PB5F15	AF11	IO188NB5F17	AD6	IO206NB6F19	V5
IO170NB5F15	AB11	IO188PB5F17	AE6	IO206PB6F19	V6
IO170PB5F15	AC11	IO189NB5F17	AB6	IO207NB6F19	Y1
IO171NB5F16	AF10	IO189PB5F17	AC6	IO207PB6F19	AA1
IO171PB5F16	AG10	IO190NB5F17	AF5	IO208NB6F19	W4
IO172NB5F16	AD10	IO190PB5F17	AG5	IO208PB6F19	Y4
IO172PB5F16	AE10	IO191NB5F17	AA6	IO209NB6F19	T7
IO173NB5F16	Y12	IO191PB5F17	AA7	IO209PB6F19	U7
IO173PB5F16	AA12	IO192NB5F17	Y8	IO210NB6F19	W2
IO174NB5F16	AB10	IO192PB5F17	AA8	IO210PB6F19	Y2
IO174PB5F16	AC10	Bank 6		IO211NB6F19	U5
IO175NB5F16	AF9	IO193NB6F18	W8	IO211PB6F19	U6
IO175PB5F16	AG9	IO193PB6F18	Y7	IO212NB6F19	V3
IO176NB5F16	AD9	IO194NB6F18	AB5	IO212PB6F19	W3
IO176PB5F16	AE9	IO194PB6F18	AC5	IO213NB6F19	R9
IO177NB5F16	Y11	IO195NB6F18	AC2	IO213PB6F19	T8
IO177PB5F16	AA11	IO195PB6F18	AC3	IO214NB6F20	U4
IO178NB5F16	AF8	IO196NB6F18	AC4	IO214PB6F20	V4
IO178PB5F16	AG8	IO196PB6F18	AD4	IO215NB6F20	T5
IO179NB5F16	AD8	IO197NB6F18	Y5	IO215PB6F20	T6
IO179PB5F16	AE8	IO197PB6F18	Y6	IO216NB6F20	V1
IO180NB5F16	AB9	IO198NB6F18	AB3	IO216PB6F20	W1
IO180PB5F16	AC9	IO198PB6F18	AB4	IO217NB6F20	R7
IO181NB5F17	Y10	IO199NB6F18	V7	IO217PB6F20	R8
IO181PB5F17	AA10	IO199PB6F18	W7	IO218NB6F20	U2

FG484		FG484		FG484	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO54PB2F5	H22	IO72PB3F6	P20	IO90NB4F8	Y17
IO55NB2F5	L17	IO73PB3F6	R19	IO90PB4F8	Y18
IO55PB2F5	K17	IO74NB3F7	V21	IO91NB4F8	V15
IO56NB2F5	K21	IO74PB3F7	U21	IO91PB4F8	V16
IO56PB2F5	K22	IO75NB3F7	V22	IO92PB4F8	AB17
IO58NB2F5	L20	IO75PB3F7	U22	IO93NB4F8	Y15
IO58PB2F5	K20	IO76NB3F7	U20	IO93PB4F8	Y16
IO59NB2F5	L18	IO76PB3F7	T20	IO94NB4F9	AA16
IO59PB2F5	K18	IO77NB3F7	R17	IO94PB4F9	AA17
IO60NB2F5	M21	IO77PB3F7	P17	IO95NB4F9	AB14
IO60PB2F5	L21	IO78NB3F7	W21	IO95PB4F9	AB15
IO61NB2F5	L16	IO78PB3F7	W22	IO96NB4F9	W15
IO61PB2F5	K16	IO79NB3F7	T18	IO96PB4F9	W16
IO62NB2F5	M19	IO79PB3F7	R18	IO97NB4F9	AA13
IO62PB2F5	L19	IO80NB3F7	W20	IO97PB4F9	AB13
Bank 3		IO80PB3F7	V20	IO98NB4F9	AA14
IO63NB3F6	N16	IO81NB3F7	U19	IO98PB4F9	AA15
IO63PB3F6	M16	IO81PB3F7	T19	IO100NB4F9	Y14
IO64NB3F6	P22	IO82NB3F7	U18	IO100PB4F9	W14
IO64PB3F6	N22	IO82PB3F7	V19	IO101NB4F9	Y12
IO65NB3F6	N20	IO83NB3F7	R16	IO101PB4F9	Y13
IO65PB3F6	M20	IO83PB3F7	P16	IO102NB4F9	AA11
IO66NB3F6	P21	Bank 4		IO102PB4F9	AA12
IO66PB3F6	N21	IO84NB4F8	AB18	IO103NB4F9/CLKEN	V12
IO67NB3F6	N18	IO84PB4F8	AB19	IO103PB4F9/CLKEP	V13
IO67PB3F6	N19	IO85NB4F8	T15	IO104NB4F9/CLKFN	W11
IO68NB3F6	T22	IO85PB4F8	T16	IO104PB4F9/CLKFP	W12
IO68PB3F6	R22	IO86NB4F8	AA18	Bank 5	
IO69NB3F6	N17	IO86PB4F8	AA19	IO105NB5F10/CLKGN	U10
IO69PB3F6	M17	IO87NB4F8	W17	IO105PB5F10/CLKGP	U11
IO70NB3F6	T21	IO87PB4F8	V17	IO106NB5F10/CLKHN	V9
IO70PB3F6	R21	IO88NB4F8	Y19	IO106PB5F10/CLKHP	V10
IO71NB3F6	P18	IO88PB4F8	W18	IO107NB5F10	Y10
IO71PB3F6	P19	IO89NB4F8	U14	IO107PB5F10	Y11
IO72NB3F6	R20	IO89PB4F8	U15	IO108NB5F10	AA9

FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
NC	J5	VCCA	J10	VCCDA	AD10
NC	J6	VCCA	J11	VCCDA	AD13
NC	P22	VCCA	J12	VCCDA	AD17
NC	R20	VCCA	J13	VCCDA	B1
NC	R21	VCCA	J14	VCCDA	B17
NC	R22	VCCA	J15	VCCDA	D24
NC	R4	VCCA	J16	VCCDA	E14
NC	R5	VCCA	J17	VCCDA	P2
NC	T22	VCCA	K18	VCCDA	P23
NC	T24	VCCA	K9	VCCIB0	G10
NC	U22	VCCA	L18	VCCIB0	G8
NC	U24	VCCA	L9	VCCIB0	G9
NC	V22	VCCA	M18	VCCIB0	H10
NC	V5	VCCA	M9	VCCIB0	H11
NC	W21	VCCA	N18	VCCIB0	H12
NC	W22	VCCA	N9	VCCIB0	H13
NC	W5	VCCA	P18	VCCIB0	H9
NC	W6	VCCA	P9	VCCIB1	G17
NC	Y21	VCCA	R18	VCCIB1	G18
NC	Y4	VCCA	R9	VCCIB1	G19
NC	Y5	VCCA	T18	VCCIB1	H14
NC	Y6	VCCA	T9	VCCIB1	H15
PRA	E13	VCCA	U18	VCCIB1	H16
PRB	B14	VCCA	U9	VCCIB1	H17
PRC	Y14	VCCA	V10	VCCIB1	H18
PRD	AD14	VCCA	V11	VCCIB2	H20
TCK	E5	VCCA	V12	VCCIB2	J19
TDI	B3	VCCA	V13	VCCIB2	J20
TDO	G6	VCCA	V14	VCCIB2	K19
TMS	D4	VCCA	V15	VCCIB2	K20
TRST	A2	VCCA	V16	VCCIB2	L19
VCCA	AB4	VCCA	V17	VCCIB2	M19
VCCA	AF24	VCCDA	A3	VCCIB2	N19
VCCA	C1	VCCDA	AB22	VCCIB3	P19
VCCA	C26	VCCDA	AB5	VCCIB3	R19

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO51PB1F4	E21	IO68PB2F6	K24	IO86NB2F8	N28
IO52NB1F4	F22	IO69NB2F6	F27	IO86PB2F8	N27
IO52PB1F4	E22	IO69PB2F6	E27	IO87NB2F8	P29
IO53NB1F4	B25	IO70NB2F6	J26	IO87PB2F8	P30
IO53PB1F4	B24	IO70PB2F6	J25	IO88NB2F8	P25
IO54NB1F5	D24	IO71NB2F6	H27	IO88PB2F8	P24
IO54PB1F5	D23	IO71PB2F6	G27	IO89NB2F8	P28
IO55NB1F5	F23	IO72NB2F6	J28	IO89PB2F8	P27
IO55PB1F5	E23	IO72PB2F6	H28	IO90NB2F8	P22
IO56NB1F5	H21	IO73NB2F6	G28	IO90PB2F8	P23
IO56PB1F5	G21	IO73PB2F6	F28	IO91NB2F8	R26
IO57NB1F5	D25	IO74NB2F7	L23	IO91PB2F8	P26
IO57PB1F5	C25	IO74PB2F7	L24	IO92NB2F8	R24
IO58NB1F5	F24	IO75NB2F7	L26	IO92PB2F8	R25
IO58PB1F5	E24	IO75PB2F7	K26	IO93NB2F8	R29
IO59NB1F5	D26	IO76NB2F7	M25	IO93PB2F8	R30
IO59PB1F5	C26	IO76PB2F7	L25	IO94NB2F8	R22
IO60NB1F5	G23	IO77NB2F7	K27	IO94PB2F8	R23
IO60PB1F5	G22	IO77PB2F7	J27	IO95NB2F8	T27
IO61NB1F5	B27	IO78NB2F7	M27	IO95PB2F8	R27
IO61PB1F5	A27	IO78PB2F7	L27	Bank 3	
IO62NB1F5	F25	IO79NB2F7	K30	IO96NB3F9	T29
IO62PB1F5	E25	IO79PB2F7	K29	IO96PB3F9	T30
IO63NB1F5	H23	IO80NB2F7	M23	IO97NB3F9	U29
IO63PB1F5	H22	IO80PB2F7	M24	IO97PB3F9	U30
Bank 2		IO81NB2F7	M28	IO98NB3F9	T22
IO64NB2F6	K23	IO81PB2F7	L28	IO98PB3F9	T23
IO64PB2F6	J23	IO82NB2F7	N26	IO99NB3F9	U26
IO65NB2F6	J24	IO82PB2F7	M26	IO99PB3F9	T26
IO65PB2F6	H24	IO83NB2F7	N25	IO100NB3F9	U24
IO66NB2F6	H26	IO83PB2F7	N24	IO100PB3F9	T24
IO66PB2F6	H25	IO84NB2F7	N22	IO101NB3F9	V28
IO67NB2F6	G26	IO84PB2F7	N23	IO101PB3F9	U28
IO67PB2F6	G25	IO85NB2F8	M29	IO102NB3F9	U23
IO68NB2F6	K25	IO85PB2F8	L29	IO102PB3F9	U22

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
NC	K1	VCCA	N20	VCCDA	AF19
NC	K2	VCCA	P11	VCCDA	C13
NC	L30	VCCA	P20	VCCDA	C5
NC	M30	VCCA	R11	VCCDA	D13
NC	N29	VCCA	R20	VCCDA	D19
NC	T1	VCCA	T11	VCCDA	D3
NC	U1	VCCA	T20	VCCDA	E18
NC	W30	VCCA	U11	VCCDA	F26
NC	Y1	VCCA	U20	VCCDA	G16
NC	Y2	VCCA	V11	VCCDA	T25
NC	Y30	VCCA	V20	VCCDA	T4
PRA	G15	VCCA	W11	VCCIB0	A3
PRB	D16	VCCA	W20	VCCIB0	B3
PRC	AB16	VCCA	Y12	VCCIB0	J10
PRD	AF16	VCCA	Y13	VCCIB0	J11
TCK	G7	VCCA	Y14	VCCIB0	J12
TDI	D5	VCCA	Y15	VCCIB0	K11
TDO	J8	VCCA	Y16	VCCIB0	K12
TMS	F6	VCCA	Y17	VCCIB0	K13
TRST	C4	VCCA	Y18	VCCIB0	K14
VCCA	AD6	VCCA	Y19	VCCIB0	K15
VCCA	AH26	VCCPLA	G14	VCCIB1	A28
VCCA	E28	VCCPLB	H15	VCCIB1	B28
VCCA	E3	VCCPLC	G17	VCCIB1	J19
VCCA	L12	VCCPLD	J16	VCCIB1	J20
VCCA	L13	VCCPLE	AH17	VCCIB1	J21
VCCA	L14	VCCPLF	AC16	VCCIB1	K16
VCCA	L15	VCCPLG	AH14	VCCIB1	K17
VCCA	L16	VCCPLH	AD15	VCCIB1	K18
VCCA	L17	VCCDA	AD24	VCCIB1	K19
VCCA	L18	VCCDA	AD7	VCCIB1	K20
VCCA	L19	VCCDA	AF12	VCCIB2	C29
VCCA	M11	VCCDA	AF13	VCCIB2	C30
VCCA	M20	VCCDA	AF15	VCCIB2	K22
VCCA	N11	VCCDA	AF18	VCCIB2	L21

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO103PB2F9	M28	IO121NB2F11	T27	IO138NB3F12	Y29
IO104NB2F9	M34	IO121PB2F11	T26	IO138PB3F12	W29
IO104PB2F9	L34	IO122NB2F11	T30	IO139NB3F13	Y27
IO105NB2F9	P27	IO122PB2F11	T29	IO139PB3F13	W27
IO105PB2F9	N27	IO123NB2F11	U28	IO140NB3F13	AA33
IO106NB2F9	M32	IO123PB2F11	T28	IO140PB3F13	Y33
IO106PB2F9	M31	IO124NB2F11	T31	IO141NB3F13	Y25
IO107NB2F10	P25	IO124PB2F11	T32	IO141PB3F13	Y24
IO107PB2F10	P26	IO125NB2F11	U24	IO142NB3F13	AA31
IO108NB2F10	N33	IO125PB2F11	U25	IO142PB3F13	Y31
IO108PB2F10	M33	IO126NB2F11	U33	IO143NB3F13	AA28
IO109NB2F10	P29	IO126PB2F11	U34	IO143PB3F13	Y28
IO109PB2F10	N29	IO127NB2F11	U26	IO144NB3F13	AA34
IO110NB2F10	P30	IO127PB2F11	U27	IO144PB3F13	Y34
IO110PB2F10	N30	IO128NB2F11	U31	IO145NB3F13	AA26
IO111NB2F10	R24	IO128PB2F11	U32	IO145PB3F13	Y26
IO111PB2F10	R25	Bank 3		IO146NB3F13	AA29
IO112NB2F10	P31	IO129NB3F12	V29	IO146PB3F13	AA30
IO112PB2F10	N31	IO129PB3F12	U29	IO147NB3F13	AB30
IO113NB2F10	R28	IO130NB3F12	V31	IO147PB3F13	AB29
IO113PB2F10	P28	IO130PB3F12	V32	IO148NB3F13	AB32
IO114NB2F10	P32	IO131NB3F12	V24	IO148PB3F13	AA32
IO114PB2F10	N32	IO131PB3F12	V25	IO149NB3F13	AB27
IO115NB2F10	R30	IO132NB3F12	W28	IO149PB3F13	AA27
IO115PB2F10	R29	IO132PB3F12	V28	IO150NB3F14	AC31
IO116NB2F10	P34	IO133NB3F12	W26	IO150PB3F14	AB31
IO116PB2F10	P33	IO133PB3F12	V26	IO151NB3F14	AD33
IO117NB2F10	R27	IO134NB3F12	W33	IO151PB3F14	AC33
IO117PB2F10	R26	IO134PB3F12	V33	IO152NB3F14	AC28
IO118NB2F11	R34	IO135NB3F12	W25	IO152PB3F14	AB28
IO118PB2F11	R33	IO135PB3F12	W24	IO153NB3F14	AB25
IO119NB2F11	T24	IO136NB3F12	W31	IO153PB3F14	AA25
IO119PB2F11	T25	IO136PB3F12	W32	IO154NB3F14	AD32
IO120NB2F11	T33	IO137NB3F12	Y30	IO154PB3F14	AC32
IO120PB2F11	T34	IO137PB3F12	W30	IO155NB3F14	AD29

CQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132

CQ208	
AX500 Function	Pin Number
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
Bank 4	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76

CQ208	
AX500 Function	Pin Number
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
GND	21	GND	240	TDI	348
GND	27	GND	246	TDO	347
GND	33	GND	252	TMS	350
GND	39	GND	258	TRST	351
GND	45	GND	264	VCCA	3
GND	51	GND	265	VCCA	14
GND	57	GND	274	VCCA	32
GND	63	GND	280	VCCA	56
GND	69	GND	286	VCCA	74
GND	75	GND	292	VCCA	87
GND	81	GND	298	VCCA	102
GND	88	GND	310	VCCA	114
GND	89	GND	322	VCCA	150
GND	97	GND	330	VCCA	162
GND	103	GND	334	VCCA	175
GND	109	GND	340	VCCA	191
GND	115	GND	345	VCCA	209
GND	121	GND/LP	352	VCCA	233
GND	133	NC	91	VCCA	251
GND	145	NC	117	VCCA	263
GND	151	NC	130	VCCA	279
GND	157	NC	131	VCCA	291
GND	163	NC	148	VCCA	329
GND	169	NC	174	VCCA	339
GND	176	NC	268	VCCDA	2
GND	177	NC	294	VCCDA	44
GND	186	NC	307	VCCDA	90
GND	192	NC	308	VCCDA	116
GND	198	NC	327	VCCDA	132
GND	204	NC	328	VCCDA	149
GND	210	PRA	312	VCCDA	178
GND	216	PRB	311	VCCDA	221
GND	222	PRC	135	VCCDA	266
GND	228	PRD	134	VCCDA	293
GND	234	TCK	349	VCCDA	309

CG624	
AX2000 Function	Pin Number
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22*
IO169PB3F15	W23*
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20*
IO171PB4F16	AC21*
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.