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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax1000-2fg896i

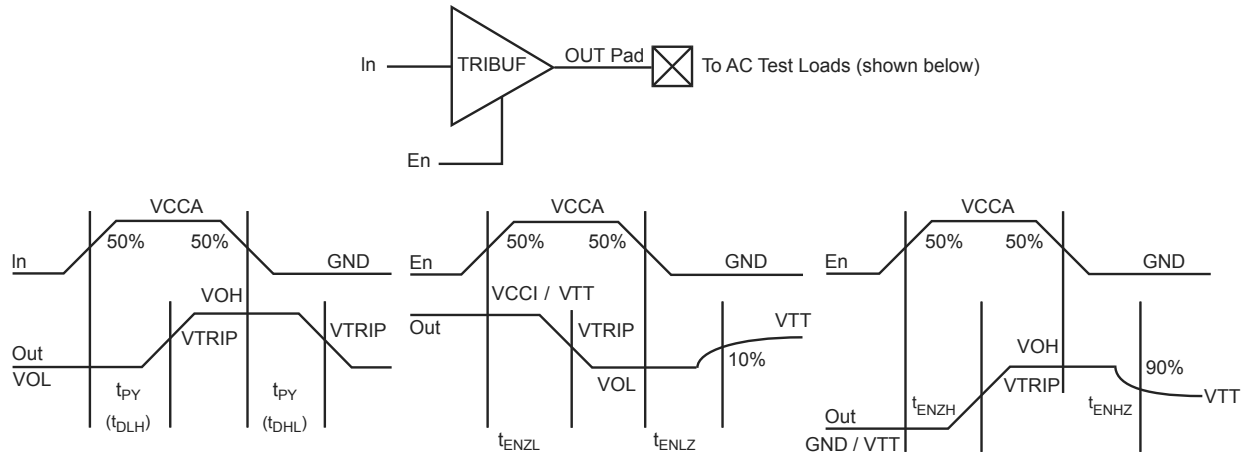


Figure 2-10 • Output Buffer Delays

I/O Module Timing Characteristics

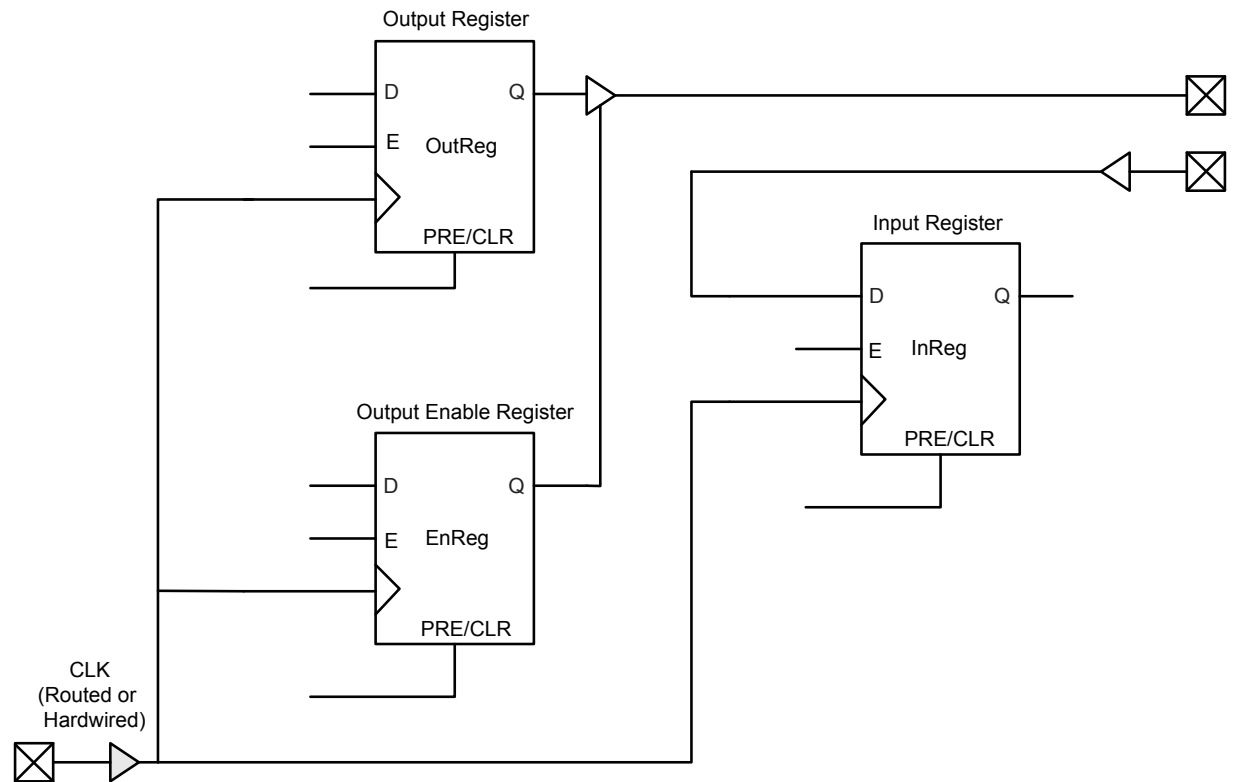


Figure 2-11 • Timing Model

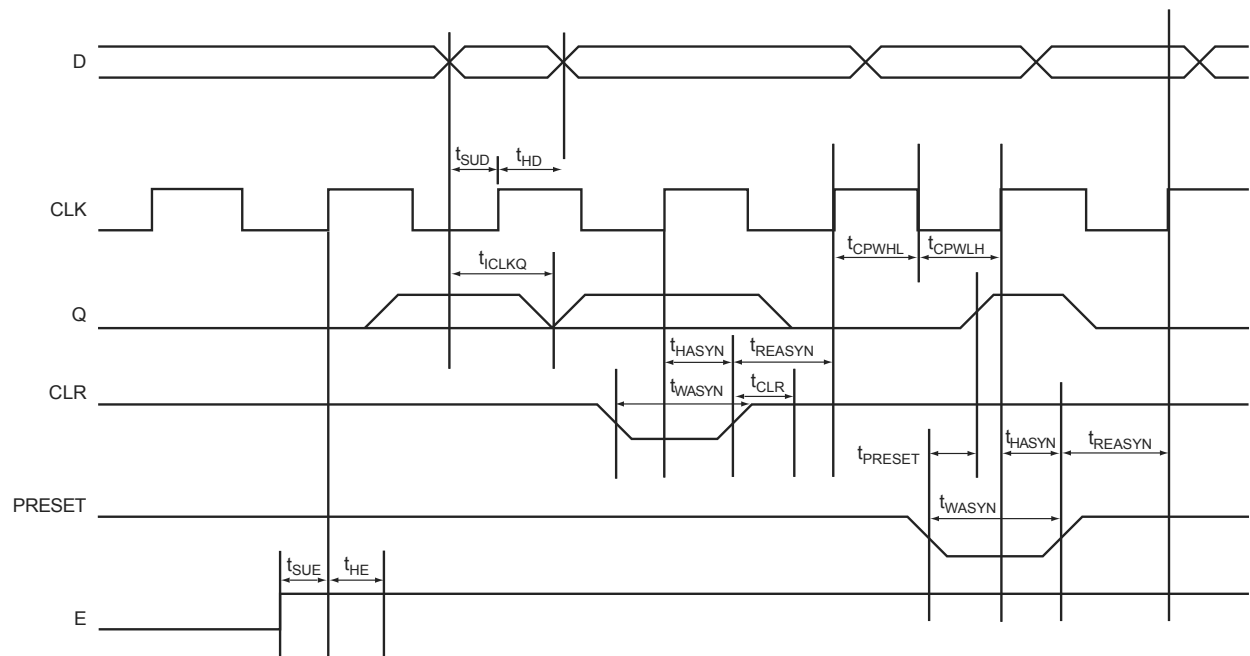


Figure 2-12 • Input Register Timing Characteristics

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 4 (24 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		10.45		11.90		13.99	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		10.61		12.08		14.21	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		10.47		11.93		14.02	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.92		1.94		1.94	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.57		2.58		2.59	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-25 • 2.5V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_j = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS25 I/O Module Timing								
t _{DP}	Input Buffer		1.95		2.22		2.61	ns
t _{PY}	Output Buffer		3.29		3.74		4.40	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.48		2.50		2.51	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.48		2.50		2.51	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		5.74		6.54		7.69	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.60		7.51		8.83	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Class II

Table 2-47 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	15.2	-15.2

AC Loadings

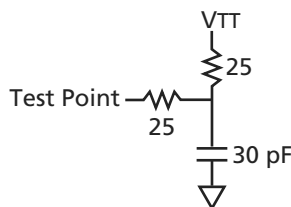


Figure 2-22 • AC Test Loads

Table 2-48 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 0.75	VREF + 0.75	VREF	1.25	30

Note: * Measuring Point = V_{trip}

Timing Characteristics

Table 2-49 • 2.5 V SSTL2 Class II I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V SSTL2 Class II I/O Module Timing								
t _{DP}	Input Buffer		1.89		2.16		2.53	ns
t _{PY}	Output Buffer		2.39		2.72		3.20	ns
t _{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-69 • AX2000 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.50	0.56	0.66	ns
t _{RD2}	Routing delay for FO2	0.59	0.67	0.79	ns
t _{RD3}	Routing delay for FO3	0.70	0.80	0.94	ns
t _{RD4}	Routing delay for FO4	0.76	0.87	1.02	ns
t _{RD5}	Routing delay for FO5	0.98	1.11	1.31	ns
t _{RD6}	Routing delay for FO6	1.48	1.68	1.97	ns
t _{RD7}	Routing delay for FO7	1.65	1.87	2.20	ns
t _{RD8}	Routing delay for FO8	1.73	1.96	2.31	ns
t _{RD16}	Routing delay for FO16	2.58	2.92	3.44	ns
t _{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Table 2-80 • PLL Interface Signals

Signal Name	Type	User Accessible	Allowable Values	Function
RefCLK	Input	Yes		Reference Clock for the PLL
FB	Input	Yes		Feedback port for the PLL
PowerDown	Input	Yes		PLL power down control
			0	PLL powered down
			1	PLL active
DIVI[5:0]	Input	Yes	1 to 64, in unsigned binary notation offset by -1	Sets value for feedback divider (multiplier)
DIVJ[5:0]	Input	Yes		Sets value for CLK1 divider
LowFreq	Input	Yes		Input frequency range selector
			0	50–200 MHz
			1	14–50 MHz
Osc[2:0]	Input	Yes		Output frequency range selector
			XX0	400–1000 MHZ
			001	200–400 MHZ
			011	100–200 MHZ
			101	50–100 MHZ
			111	20–50 MHZ
DelayLine[4:0]	Input	Yes	–15 to +15 (increments), in signed-and-magnitude binary representation	Clock Delay (positive/negative) in increments of 250 ps, with maximum value of ± 3.75 ns
FBMuxSel	Input	No		Selects the source for the feedback input
REFSEL	Input	No		Selects the source for the reference clock
OUTSEL	Input	No		Selects the source for the routed net output
PLLSEL	Input	No		ROOTSEL & PLLSEL are used to select the source of the global clock network
ROOTSEL	Input	No		
Lock	Output	Yes		High value indicates PLL has locked
CLK1	Output	Yes		PLL clock output
CLK2	Output	Yes		PLL clock output

Note: If the input RefClk is taken outside its operating range, the outputs Lock, CLK1 and CLK2 are indeterminate.

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

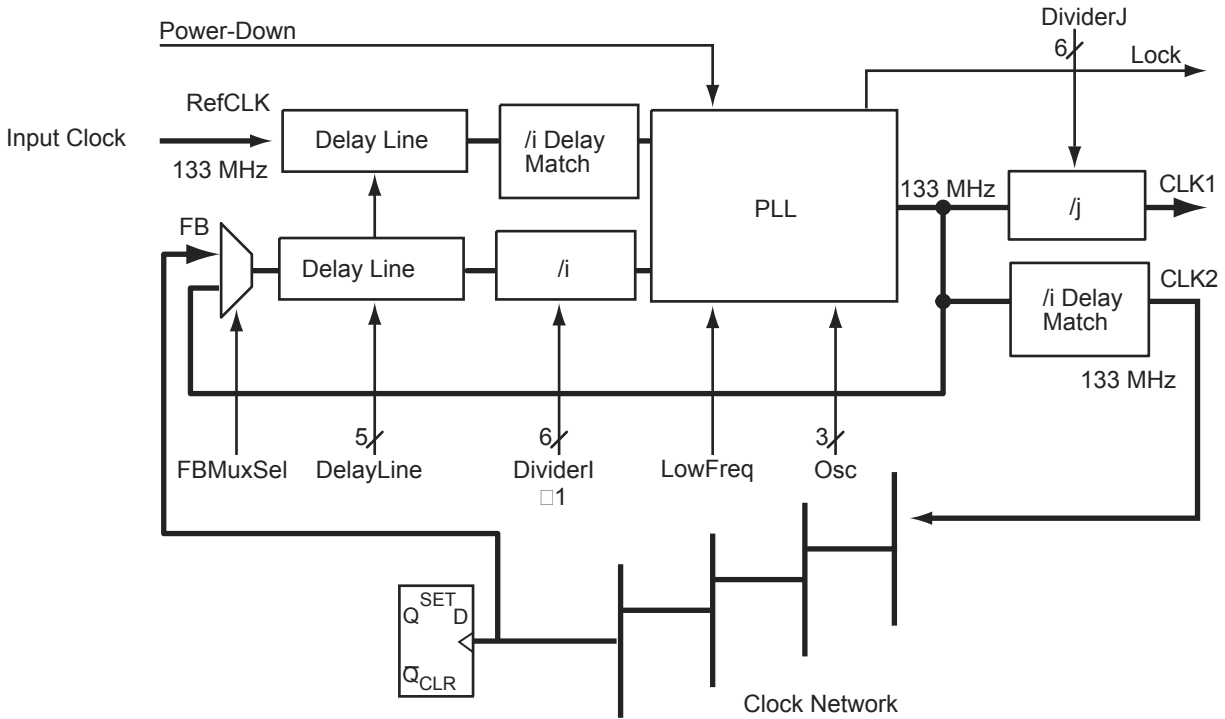


Figure 2-56 • Using the PLL for Clock Deskewing

Figure 2-63 illustrates flag generation.

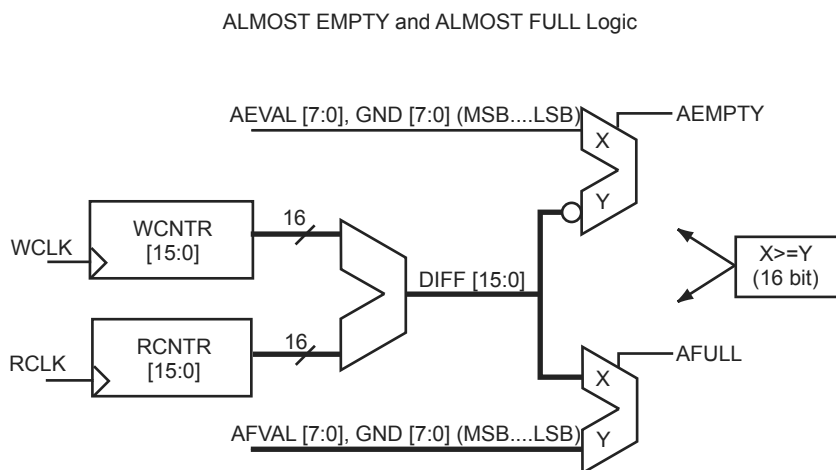


Figure 2-63 • ALMOST-EMPTY and ALMOST-FULL Logic

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0], 8'b00000000})?1:0;
assign AE = ({AEVAL[7:0], 8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-95).

Table 2-95 • Number of Available Configuration Bits

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-100.

FG324	
AX125 Function	Pin Number
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG484	
AX1000 Function	Pin Number
IO167PB5F15	AA12
IO169NB5F15	AA9
IO169PB5F15	AA10
IO170NB5F15	AB9
IO170PB5F15	AB10
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	Y8
IO172PB5F16	Y9
IO173NB5F16	U8
IO173PB5F16	U9
IO174NB5F16	AA7
IO174PB5F16	AA8
IO175NB5F16	AB5
IO175PB5F16	AB6
IO176NB5F16	AA5
IO176PB5F16	AA6
IO177NB5F16	AA4
IO177PB5F16	AB4
IO178NB5F16	Y6
IO178PB5F16	Y7
IO179NB5F16	T7
IO179PB5F16	T8
IO180NB5F16	W6
IO180PB5F16	W7
IO181NB5F17	Y4
IO181PB5F17	Y5
IO184NB5F17	AB7
IO187NB5F17	V3
IO187PB5F17	W3
IO188NB5F17	V4
IO188PB5F17	W5
IO192NB5F17	V6
IO192PB5F17	V7
Bank 6	

FG484	
AX1000 Function	Pin Number
IO194NB6F18	V2
IO194PB6F18	W2
IO195NB6F18	U5
IO195PB6F18	T5
IO200NB6F18	T4
IO200PB6F18	U4
IO201NB6F18	P6
IO201PB6F18	R6
IO203NB6F19	U2
IO204NB6F19	T3
IO204PB6F19	U3
IO205NB6F19	P5
IO205PB6F19	R5
IO208NB6F19	V1
IO208PB6F19	W1
IO209NB6F19	P7
IO209PB6F19	R7
IO212NB6F19	P4
IO212PB6F19	R4
IO214NB6F20	P3
IO214PB6F20	R3
IO215NB6F20	M6
IO215PB6F20	N6
IO216NB6F20	R2
IO216PB6F20	T2
IO217NB6F20	T1
IO217PB6F20	U1
IO219NB6F20	M5
IO219PB6F20	N5
IO220NB6F20	P1
IO220PB6F20	R1
IO221NB6F20	N2
IO221PB6F20	P2
IO222NB6F20	M3
IO222PB6F20	N3

FG484	
AX1000 Function	Pin Number
IO223NB6F20	M7
IO223PB6F20	N7
IO224NB6F20	M4
IO224PB6F20	N4
Bank 7	
IO225NB7F21	M2
IO225PB7F21	N1
IO226NB7F21	K2
IO226PB7F21	K1
IO228NB7F21	L3
IO228PB7F21	L2
IO229NB7F21	K5
IO229PB7F21	L5
IO230NB7F21	H1
IO230PB7F21	J1
IO231NB7F21	H2
IO231PB7F21	J2
IO232NB7F21	K4
IO232PB7F21	K3
IO233NB7F21	K6
IO233PB7F21	L6
IO234NB7F21	F1
IO234PB7F21	G1
IO235NB7F21	F2
IO235PB7F21	G2
IO236NB7F22	H3
IO236PB7F22	J3
IO237NB7F22	K7
IO237PB7F22	L7
IO241NB7F22	H6
IO241PB7F22	J6
IO242NB7F22	H4
IO242PB7F22	J4
IO243NB7F22	H5
IO243PB7F22	J5

FG676	
AX1000 Function	Pin Number
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26
IO73PB2F6	D26
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23

FG676	
AX1000 Function	Pin Number
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
Bank 3	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24
IO100NB3F9	R22
IO100PB3F9	P22
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25

FG676	
AX1000 Function	Pin Number
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
Bank 4	
IO129NB4F12	AB21

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	AK12	GND	AN34	GND	D1
GND	AK17	GND	AN4	GND	D11
GND	AK18	GND	AN9	GND	D2
GND	AK23	GND	AP13	GND	D24
GND	AK30	GND	AP2	GND	D3
GND	AK5	GND	AP22	GND	D31
GND	AL1	GND	AP27	GND	D32
GND	AL11	GND	AP3	GND	D33
GND	AL2	GND	AP31	GND	D34
GND	AL24	GND	AP32	GND	D4
GND	AL3	GND	AP33	GND	E12
GND	AL31	GND	AP4	GND	E17
GND	AL32	GND	AP8	GND	E18
GND	AL33	GND	B1	GND	E23
GND	AL34	GND	B2	GND	E30
GND	AL4	GND	B26	GND	E5
GND	AM1	GND	B3	GND	F29
GND	AM10	GND	B31	GND	F30
GND	AM15	GND	B32	GND	F6
GND	AM2	GND	B33	GND	G28
GND	AM20	GND	B34	GND	G7
GND	AM25	GND	B4	GND	H1
GND	AM3	GND	B9	GND	H34
GND	AM31	GND	C1	GND	J2
GND	AM32	GND	C10	GND	J33
GND	AM33	GND	C15	GND	K3
GND	AM34	GND	C2	GND	K32
GND	AM4	GND	C20	GND	L11
GND	AN1	GND	C25	GND	L24
GND	AN2	GND	C3	GND	L31
GND	AN26	GND	C31	GND	L4
GND	AN3	GND	C32	GND	M12
GND	AN31	GND	C33	GND	M23
GND	AN32	GND	C34	GND	M30
GND	AN33	GND	C4	GND	M5

CQ352	
AX250 Function	Pin Number
IO64PB4F4	167
IO65NB4F4	170
IO65PB4F4	171
IO66NB4F4	164
IO66PB4F4	165
IO67NB4F4	160
IO67PB4F4	161
IO68NB4F4	158
IO68PB4F4	159
IO70NB4F4	154
IO70PB4F4	155
IO72NB4F4	152
IO72PB4F4	153
IO73NB4F4	146
IO73PB4F4	147
IO74NB4F4/CLKEN	142
IO74PB4F4/CLKEP	143
IO75NB4F4/CLKFN	136
IO75PB4F4/CLKFP	137
Bank 5	
IO76NB5F5/CLKGN	128
IO76PB5F5/CLKGP	129
IO77NB5F5/CLKHN	122
IO77PB5F5/CLKHP	123
IO78NB5F5	112
IO78PB5F5	113
IO79NB5F5	118
IO79PB5F5	119
IO80NB5F5	110
IO80PB5F5	111
IO82NB5F5	106
IO82PB5F5	107
IO84NB5F5	100
IO84PB5F5	101
IO85NB5F5	104

CQ352	
AX250 Function	Pin Number
IO85PB5F5	105
IO86NB5F5	98
IO86PB5F5	99
IO87NB5F5	94
IO87PB5F5	95
IO89NB5F5	92
IO89PB5F5	93
Bank 6	
IO90PB6F6	86
IO91NB6F6	84
IO91PB6F6	85
IO92NB6F6	78
IO92PB6F6	79
IO93NB6F6	82
IO93PB6F6	83
IO95NB6F6	76
IO95PB6F6	77
IO96NB6F6	72
IO96PB6F6	73
IO97NB6F6	70
IO97PB6F6	71
IO98NB6F6	66
IO98PB6F6	67
IO99NB6F6	64
IO99PB6F6	65
IO100NB6F6	60
IO100PB6F6	61
IO101NB6F6	58
IO101PB6F6	59
IO103NB6F6	54
IO103PB6F6	55
IO104NB6F6	52
IO104PB6F6	53
IO105NB6F6	48
IO105PB6F6	49

CQ352	
AX250 Function	Pin Number
IO106NB6F6	46
IO106PB6F6	47
Bank 7	
IO107NB7F7	40
IO107PB7F7	41
IO108NB7F7	42
IO108PB7F7	43
IO109NB7F7	36
IO109PB7F7	37
IO110NB7F7	34
IO110PB7F7	35
IO111NB7F7	30
IO111PB7F7	31
IO113NB7F7	28
IO113PB7F7	29
IO114NB7F7	24
IO114PB7F7	25
IO115NB7F7	22
IO115PB7F7	23
IO116NB7F7	18
IO116PB7F7	19
IO117NB7F7	16
IO117PB7F7	17
IO118NB7F7	12
IO118PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121NB7F7	6
IO121PB7F7	7
IO123NB7F7	4
IO123PB7F7	5
Dedicated I/O	
GND	1
GND	9
GND	15

CQ352		CQ352		CQ352	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	21	GND	240	VCCA	150
GND	27	GND	246	VCCA	162
GND	33	GND	252	VCCA	175
GND	39	GND	258	VCCA	191
GND	45	GND	264	VCCA	209
GND	51	GND	265	VCCA	233
GND	57	GND	274	VCCA	251
GND	63	GND	280	VCCA	263
GND	69	GND	286	VCCA	279
GND	75	GND	292	VCCA	291
GND	81	GND	298	VCCA	329
GND	88	GND	310	VCCA	339
GND	89	GND	322	VCCDA	2
GND	97	GND	330	VCCDA	44
GND	103	GND	334	VCCDA	90
GND	109	GND	340	VCCDA	91
GND	115	GND	345	VCCDA	116
GND	121	GND	352	VCCDA	117
GND	133	PRA	312	VCCDA	130
GND	145	PRB	311	VCCDA	131
GND	151	PRC	135	VCCDA	132
GND	157	PRD	134	VCCDA	148
GND	163	TCK	349	VCCDA	149
GND	169	TDI	348	VCCDA	174
GND	176	TDO	347	VCCDA	178
GND	177	TMS	350	VCCDA	221
GND	186	TRST	351	VCCDA	266
GND	192	VCCA	3	VCCDA	268
GND	198	VCCA	14	VCCDA	293
GND	204	VCCA	32	VCCDA	294
GND	210	VCCA	56	VCCDA	307
GND	216	VCCA	74	VCCDA	308
GND	222	VCCA	87	VCCDA	309
GND	228	VCCA	102	VCCDA	327
GND	234	VCCA	114	VCCDA	328

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO131NB4F12	V19	IO153NB4F14	Y15	IO173PB5F16	Y11
IO131PB4F12	W19	IO153PB4F14	Y16	IO174NB5F16	AB10
IO133NB4F12	Y18	IO155NB4F14	V15	IO174PB5F16	AB11
IO133PB4F12	Y19	IO155PB4F14	V16	IO175NB5F16	AC9
IO135NB4F12	W18	IO156NB4F14	AB14	IO175PB5F16	AE9
IO135PB4F12	V18	IO156PB4F14	AB15	IO177NB5F16	AA8
IO137NB4F12	Y17	IO157NB4F14	AE14	IO177PB5F16	Y8
IO137PB4F12	AA17	IO157PB4F14	AC18	IO178NB5F16	Y6
IO138NB4F12	AB19	IO158NB4F14	AC15	IO178PB5F16	W6
IO138PB4F12	AB18	IO158PB4F14	AC19	IO179NB5F16	Y10
IO139NB4F13	AA19	IO159NB4F14/CLKEN	W14	IO179PB5F16	W10
IO139PB4F13	U18	IO159PB4F14/CLKEP	W15	IO180NB5F16	Y7
IO140NB4F13	AC20	IO160NB4F14/CLKFN	AC13	IO180PB5F16	W7
IO140PB4F13	AC21	IO160PB4F14/CLKFP	AD13	IO181NB5F17	AD9
IO141NB4F13	AD17	Bank 5		IO181PB5F17	AD10
IO141PB4F13	AD18	IO161NB5F15/CLKGN	W13	IO182NB5F17	AE10
IO142NB4F13	AD21	IO161PB5F15/CLKGP	Y13	IO182PB5F17	AE11
IO142PB4F13	AD22	IO162NB5F15/CLKHN	AC12	IO183NB5F17	AD7
IO143NB4F13	AB17	IO162PB5F15/CLKHP	AD12	IO183PB5F17	AD8
IO143PB4F13	AC17	IO163NB5F15	V9	IO184NB5F17	AB9
IO144PB4F13	AE22	IO163PB5F15	V10	IO185NB5F17	AE6
IO145NB4F13	AE15	IO164NB5F15	V11	IO185PB5F17	AE7
IO145PB4F13	AE16	IO164PB5F15	T13	IO186NB5F17	AE4
IO146NB4F13	AD19	IO165NB5F15	U13	IO186PB5F17	AE5
IO146PB4F13	AD20	IO165PB5F15	V13	IO187NB5F17	AA9
IO147NB4F13	AD15	IO167NB5F15	W11	IO187PB5F17	Y9
IO147PB4F13	AD16	IO167PB5F15	W12	IO188NB5F17	U8
IO148PB4F13	AE21	IO168NB5F15	AB6	IO189NB5F17	AD5
IO149NB4F13	AD14	IO168PB5F15	AA6	IO189PB5F17	AD6
IO149PB4F13	AC14	IO169NB5F15	V8	IO191NB5F17	AC5
IO150NB4F13	AE19	IO169PB5F15	V7	IO191PB5F17	AC6
IO150PB4F13	AE20	IO171NB5F16	W8	IO192NB5F17	AB7
IO151NB4F13	V17	IO171PB5F16	W9	IO192PB5F17	AC7
IO151PB4F13	W17	IO172NB5F16	AB8	Bank 6	
IO152NB4F14	AB16	IO172PB5F16	AC8	IO193NB6F18	U6
IO152PB4F14	W16	IO173NB5F16	AA11	IO193PB6F18	U5

CG624	
AX2000 Function	Pin Number
IO310NB7F29	N10
IO310PB7F29	N9
IO311NB7F29	K1
IO311PB7F29	L1
IO313NB7F29	M5
IO316NB7F29	L6
IO316PB7F29	L5
IO317NB7F29	K2
IO317PB7F29	L2
IO318NB7F29	K4
IO318PB7F29	L4
IO320NB7F29	J3
IO321NB7F30	J2
IO321PB7F30	J1
IO323NB7F30	L7
IO323PB7F30	M7
IO324NB7F30	M9
IO324PB7F30	M8
IO327NB7F30	F1
IO327PB7F30	G1
IO328NB7F30	K7
IO328PB7F30	K6
IO329NB7F30	D1
IO329PB7F30	E1
IO331PB7F30	G2
IO332NB7F31	H3
IO332PB7F31	H2
IO333NB7F31	E2
IO333PB7F31	F2
IO334NB7F31	H4
IO334PB7F31	J4
IO335NB7F31	H5

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO335PB7F31	H6
IO337NB7F31	D2
IO338NB7F31	J6
IO338PB7F31	J5
IO339NB7F31	F3
IO339PB7F31	E3
IO340NB7F31	G4*
IO340PB7F31	G3*
IO341NB7F31	K8
IO341PB7F31	L8
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5
GND	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

Revision	Changes	Page
Revision 17 (continued)	The C180 package was removed from product tables and the "Package Pin Assignments" section (PDN 0909).	3-1
	Package names used in the "Axcelerator Family Product Profile" and "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	i, 3-1
	The "Introduction" section for "User I/Os" was updated as follows: "The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os" (SARs 24181, 24309).	2-11
	Power values in Table 2-4 • Default CLOAD/VCCI were updated to reflect those of SmartPower (SAR 33945).	2-3
	Two parameter names were corrected in Figure 2-10 • Output Buffer Delays. One occurrence of t_{ENLZ} was changed to t_{ENZL} and one occurrence of t_{ENHZ} was changed to t_{ENZH} (SAR 33890).	2-22
	The "Timing Model" section was updated with new timing values. Timing tables in the "I/O Specifications" section were updated to include enable paths. Values in the timing tables in the "Voltage-Referenced I/O Standards" section and "Differential Standards" section were updated. Table 2-63 • R-Cell was updated (SAR 33945).	2-8, 2-26 to 2-53
	Figure 2-11 • Timing Model was replaced (SAR 33043).	2-23
	The timing tables for "RAM" and "FIFO" were updated (SAR 33945).	2-90 to 2-106
	"Data Registers (DRs)" values were modified for IDCODE and USERCODE (SARs 18257, 26406).	2-108
Revision 16 (v2.8, Oct. 2009)	The package diagram for the "CQ208" package was incorrect and has been replaced with the correct diagram (SARs 23865, 26345).	3-89
	The datasheet was updated to include AX2000-CQ2526 information.	N/A
	MIL-STD-883 Class B is no longer supported by Axcelerator FPGAs and as a result was removed.	N/A
Revision 15 (v2.7, Nov. 2008)	A footnote was added to the "Introduction" in the "Axcelerator Clock Management System" section.	2-75
	RoHS-compliant information was added to the "Ordering Information".	ii
Revision 14 (v2.6)	ACTgen was changed to SmartGen because ACTgen is obsolete.	N/A
	In Table 2-4, the units for the P_{LOAD} , P_{10} , and $P_{I/O}$ were updated from mW/MHz to mW/MHz.	2-3
	In the "Pin Descriptions" section, the HCLK and CLK descriptions were updated to include tie-off information.	2-9
	The "Global Resource Distribution" section was updated.	2-70
Revision 13 (v2.5)	The "CG624" table was updated.	3-116
	A note was added to Table 2-2.	2-1
Revision 12 (v2.4)	In the "Package Thermal Characteristics", the temperature was changed from 150°C to 125°C.	2-6