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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

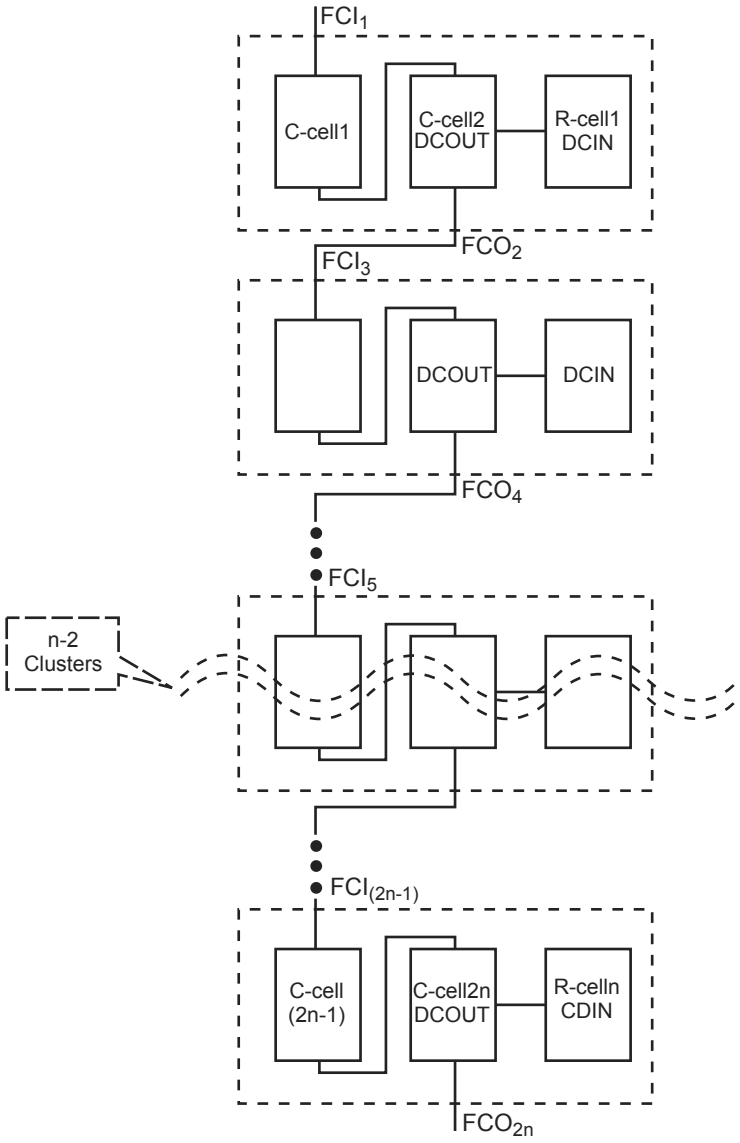
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 18144 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 165888 |
| Number of I/O | 317 |
| Number of Gates | 1000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ax1000-2fgg484 |

***Table 2-36* • 3.3 V PCI-X I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **3.3 V PCI-X Output Module Timing** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.57 | | 1.79 | | 2.10 | ns |
| $t_{PY}$ | Output Buffer | | 2.10 | | 2.40 | | 2.82 | ns |
| $t_{ENZL}$ | Enable to Pad Delay through the Output Buffer—Z to Low | | 1.61 | | 1.62 | | 1.63 | ns |
| $t_{ENZH}$ | Enable to Pad Delay through the Output Buffer—Z to High | | 1.59 | | 1.60 | | 1.61 | ns |
| $t_{ENLZ}$ | Enable to Pad Delay through the Output Buffer—Low to Z | | 2.65 | | 3.02 | | 3.55 | ns |
| $t_{ENHZ}$ | Enable to Pad Delay through the Output Buffer—High to Z | | 3.11 | | 3.55 | | 4.17 | ns |
| $t_{IOCLKQ}$ | Sequential Clock-to-Q for the I/O Input Register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{IOCLKY}$ | Clock-to-output Y for the I/O Output Register and the I/O Enable Register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |




*Note: The carry-chain sequence can end on either C-cell.*

***Figure 2-30 •*** **Carry-Chain Sequencing of C-Cells**

## *Timing Characteristics*

Refer to Table 2-62 on page 2-55 for more information on carry-chain timing.

## Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

### *Timing Characteristics*

***Table 2-75 •*** **AX125 Routed Array Clock Networks**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Routed Array Clock Networks** | | | | | | | | |
| $t_{RCKL}$ | Input Low to High | | 3.08 | | 3.50 | | 4.12 | ns |
| $t_{RCKH}$ | Input High to Low | | 3.13 | | 3.56 | | 4.19 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 0.57 | | 0.64 | | 0.75 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 0.52 | | 0.59 | | 0.69 | | ns |
| $t_{RCKSW}$ | Maximum Skew | | 0.35 | | 0.39 | | 0.46 | ns |
| $t_{RP}$ | Minimum Period | 1.15 | | 1.31 | | 1.54 | | ns |
| $t_{RMAX}$ | Maximum Frequency | | 870 | | 763 | | 649 | MHz |

***Table 2-76 •*** **AX250 Routed Array Clock Networks**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Routed Array Clock Networks** | | | | | | | | |
| $t_{RCKL}$ | Input Low to High | | 2.52 | | 2.87 | | 3.37 | ns |
| $t_{RCKH}$ | Input High to Low | | 2.59 | | 2.95 | | 3.47 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 0.57 | | 0.64 | | 0.75 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 0.52 | | 0.59 | | 0.69 | | ns |
| $t_{RCKSW}$ | Maximum Skew | | 0.35 | | 0.39 | | 0.46 | ns |
| $t_{RP}$ | Minimum Period | 1.15 | | 1.31 | | 1.54 | | ns |
| $t_{RMAX}$ | Maximum Frequency | | 870 | | 763 | | 649 | MHz |

The HM and CM modules can select between:

- The HCLK or CLK source respectively
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module respectively
- A local signal routed on generic routing resources

The AX architecture is capable of supporting a large number of local clocks—24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Microsemi's Designer software's place-and-route takes advantage of the segmented clock structure found in Axcelerator devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption.

## Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s), an internal net, or the output of a PLL. These connections can be made by using one of three types of macros: CLKBUF, CLKINT, and PLLCLK.

### *CLKBUF and HCLKBUF*

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF_LVCMOS25, HCLKBUF_LVDS, etc.) (Figure 2-42).

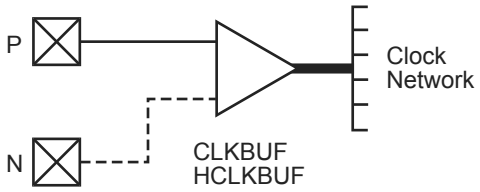



***Figure 2-42 •*** **CLKBUF and HCLKBUF**

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

### *CLKINT and HCLKINT*

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 2-43).

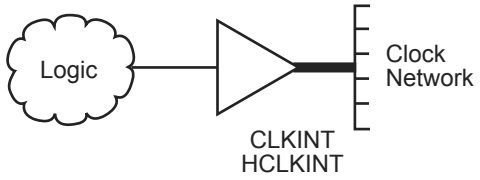



***Figure 2-43 •*** **CLKINT and HCLKINT**

***Table 2-80* • PLL Interface Signals**

| Signal Name | Type | User Accessible | Allowable Values | Function |
|---|---|---|---|---|
| RefCLK | Input | Yes | | Reference Clock for the PLL |
| FB | Input | Yes | | Feedback port for the PLL |
| PowerDown | Input | Yes | | PLL power down control |
| | | | 0 | PLL powered down |
| | | | 1 | PLL active |
| | | | | |
| DIVI[5:0] | Input | Yes | 1 to 64, in unsigned binary notation offset by -1 | Sets value for feedback divider (multiplier) |
| DIVJ[5:0] | Input | Yes | | Sets value for CLK1 divider |
| LowFreq | Input | Yes | | Input frequency range selector |
| | | | 0 | 50–200 MHz |
| | | | 1 | 14–50 MHz |
| Osc[2:0] | Input | Yes | | Output frequency range selector |
| | | | XX0 | 400–1000 MHZ |
| | | | 001 | 200–400 MHZ |
| | | | 011 | 100–200 MHZ |
| | | | 101 | 50–100 MHZ |
| | | | 111 | 20–50 MHZ |
| DelayLine[4:0] | Input | Yes | –15 to +15 (increments), in signed-and-magnitude binary representation | Clock Delay (positive/negative) in increments of 250 ps, with maximum value of ± 3.75 ns |
| FBMuxSel | Input | No | | Selects the source for the feedback input |
| REFSEL | Input | No | | Selects the source for the reference clock |
| OUTSEL | Input | No | | Selects the source for the routed net output |
| PLLSEL | Input | No | | ROOTSEL & PLLSEL are used to select the source of the global clock network |
| ROOTSEL | Input | No | | |
| Lock | Output | Yes | | High value indicates PLL has locked |
| CLK1 | Output | Yes | | PLL clock output |
| CLK2 | Output | Yes | | PLL clock output |

*Note: If the input RefClk is taken outside its operating range, the outputs Lock, CLK1 and CLK2 are indeterminate.*

Note that the RAM blocks employ little-endian byte order for read and write operations.

***Table 2-88* • RAM Signal Description**

| Signal | Direction | Description |
|---|---|---|
| WCLK | Input | Write clock (can be active on either edge). |
| WA[J:0] | Input | Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15. |
| WD[M-1:0] | Input | Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36. |
| RCLK | Input | Read clock (can be active on either edge). |
| RA[K:0] | Input | Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15. |
| RD[N-1:0] | Output | Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36. |
| REN | Input | Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD. |
| WEN | Input | Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA. |
| RW[2:0] | Input | Width of the read operation dataword. |
| WW[2:0] | Input | Width of the write operation dataword. |
| Pipe | Input | Sets the pipe option to be on or off. |

## Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

***Table 2-91* • Four RAM Blocks Cascaded**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Write Mode** | | | | | | | | |
| $t_{WDASU}$ | Write Data Setup vs. WCLK | | 2.37 | | 2.70 | | 3.17 | ns |
| $t_{WDAHD}$ | Write Data Hold vs. WCLK | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{WADSU}$ | Write Address Setup vs. WCLK | | 2.37 | | 2.70 | | 3.17 | ns |
| $t_{WADHD}$ | Write Address Hold vs. WCLK | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{WENSU}$ | Write Enable Setup vs. WCLK | | 2.37 | | 2.70 | | 3.17 | ns |
| $t_{WENHD}$ | Write Enable Hold vs. WCLK | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{WCKH}$ | WCLK Minimum High Pulse Width | 0.75 | | 0.75 | | 0.75 | | ns |
| $t_{WCLK}$ | WCLK Minimum Low Pulse Width | 2.51 | | 2.51 | | 2.51 | | ns |
| $t_{WCKP}$ | WCLK Minimum Period | 3.26 | | 3.26 | | 3.26 | | ns |
| **Read Mode** | | | | | | | | |
| $t_{RADSU}$ | Read Address Setup vs. RCLK | | 3.08 | | 3.51 | | 4.13 | ns |
| $t_{RADHD}$ | Read Address Hold vs. RCLK | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{RENSU}$ | Read Enable Setup vs. RCLK | | 3.08 | | 3.51 | | 4.13 | ns |
| $t_{RENHD}$ | Read Enable Hold vs. RCLK | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{RCK2RD1}$ | RCLK-To-OUT (Pipelined) | | 2.36 | | 2.69 | | 3.16 | ns |
| $t_{RCK2RD2}$ | RCLK-To-OUT (Non-Pipelined) | | 2.83 | | 3.23 | | 3.79 | ns |
| $t_{RCLKH}$ | RCLK Minimum High Pulse Width | 0.73 | | 0.73 | | 0.73 | | ns |
| $t_{RCLKL}$ | RCLK Minimum Low Pulse Width | 2.96 | | 2.96 | | 2.96 | | ns |
| $t_{RCKP}$ | RCLK Minimum Period | 3.69 | | 3.69 | | 3.69 | | ns |

*Note: Timing data for these four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.*

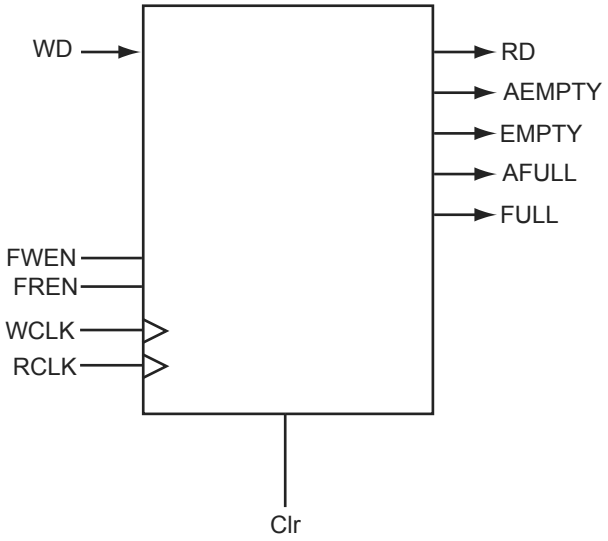



***Figure 2-66 •*** **FIFO Model**

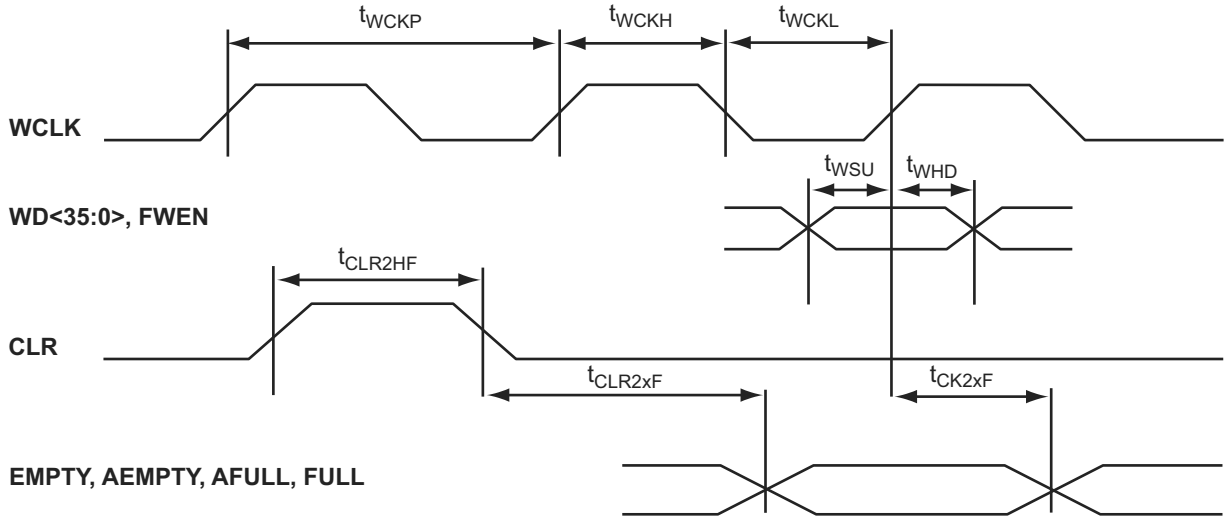



***Figure 2-67 •*** **FIFO Write Timing**

throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is protected with highest level of security in the industry.


***Figure 2-69 •*** **FuseLock Logo**

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to the *Implementation of Security in Actel Antifuse FPGAs* application note.

### *Global Set Fuse*

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (Figure 2-31 on page 2-58). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

## Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-108).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-7). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| **Bank 0** | |
| IO00NB0F0 | E6 |
| IO00PB0F0 | F6 |
| IO01NB0F0 | G8 |
| IO01PB0F0 | G7 |
| IO02NB0F0 | D7 |
| IO02PB0F0 | E7 |
| IO03NB0F0 | D5 |
| IO03PB0F0 | E5 |
| IO04NB0F0 | G9 |
| IO04PB0F0 | H9 |
| IO05NB0F0 | E8 |
| IO05PB0F0 | F8 |
| IO06NB0F0 | C6 |
| IO06PB0F0 | D6 |
| IO07NB0F0 | B5 |
| IO07PB0F0 | C5 |
| IO08NB0F0 | A6 |
| IO08PB0F0 | A5 |
| IO09NB0F0 | E9 |
| IO09PB0F0 | F9 |
| IO10NB0F0 | G10 |
| IO10PB0F0 | H10 |
| IO11NB0F0 | B7 |
| IO11PB0F0 | B6 |
| IO12NB0F1 | C8 |
| IO12PB0F1 | C7 |
| IO13NB0F1 | E10 |
| IO13PB0F1 | F10 |
| IO14NB0F1 | G11 |
| IO14PB0F1 | H11 |
| IO15NB0F1 | D9 |
| IO15PB0F1 | D8 |
| IO16NB0F1 | A8 |
| IO16PB0F1 | A7 |
| IO17NB0F1 | B9 |
| IO17PB0F1 | B8 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO18NB0F1 | C10 |
| IO18PB0F1 | C9 |
| IO19NB0F1 | E11 |
| IO19PB0F1 | F11 |
| IO20NB0F1 | G12 |
| IO20PB0F1 | H12 |
| IO21NB0F1 | D11 |
| IO21PB0F1 | D10 |
| IO22NB0F2 | A10 |
| IO22PB0F2 | A9 |
| IO23NB0F2 | B11 |
| IO23PB0F2 | B10 |
| IO24NB0F2 | G13 |
| IO24PB0F2 | H13 |
| IO25NB0F2 | C12 |
| IO25PB0F2 | C11 |
| IO26NB0F2 | E12 |
| IO26PB0F2 | D12 |
| IO27NB0F2 | E13 |
| IO27PB0F2 | F13 |
| IO28NB0F2 | G14 |
| IO28PB0F2 | H14 |
| IO29NB0F2 | A12 |
| IO29PB0F2 | B12 |
| IO30NB0F2/HCLKAN | C13 |
| IO30PB0F2/HCLKAP | D13 |
| IO31NB0F2/HCLKBN | F14 |
| IO31PB0F2/HCLKBP | E14 |
| **Bank 1** | |
| IO32NB1F3/HCLKCN | C14 |
| IO32PB1F3/HCLKCP | B14 |
| IO33NB1F3/HCLKDN | D16 |
| IO33PB1F3/HCLKDP | D15 |
| IO34NB1F3 | B16 |
| IO34PB1F3 | A16 |
| IO35NB1F3 | E15 |
| IO35PB1F3 | F15 |

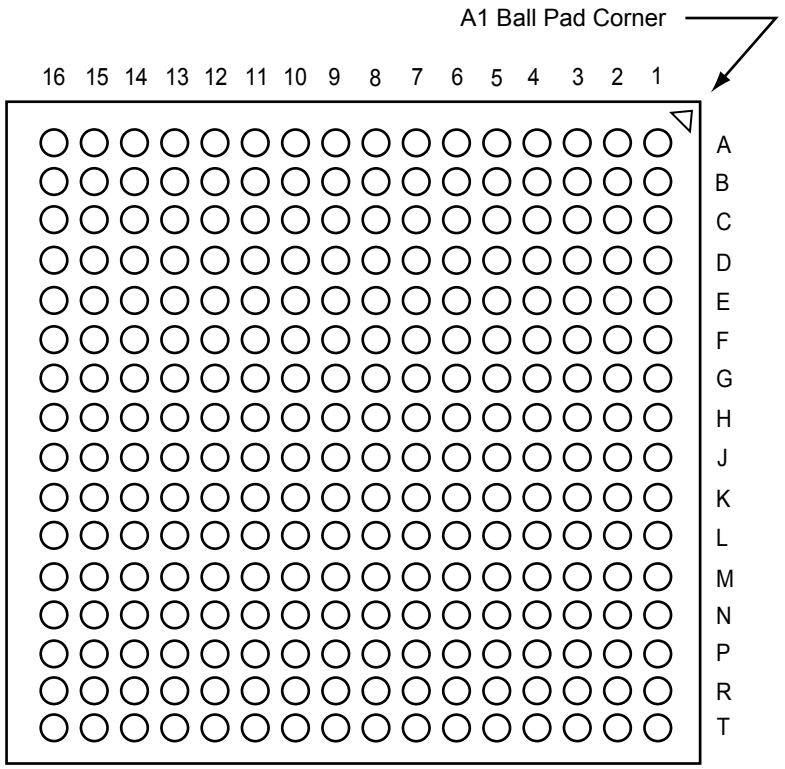
| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO36NB1F3 | H15 |
| IO36PB1F3 | G15 |
| IO37NB1F3 | C17 |
| IO37PB1F3 | C16 |
| IO38NB1F3 | B18 |
| IO38PB1F3 | B17 |
| IO39NB1F3 | A18 |
| IO39PB1F3 | A17 |
| IO40NB1F3 | H16 |
| IO40PB1F3 | G16 |
| IO41NB1F4 | B19 |
| IO41PB1F4 | A19 |
| IO42NB1F4 | C19 |
| IO42PB1F4 | C18 |
| IO43NB1F4 | D18 |
| IO43PB1F4 | D17 |
| IO44NB1F4 | H17 |
| IO44PB1F4 | G17 |
| IO45NB1F4 | F17 |
| IO45PB1F4 | E17 |
| IO46NB1F4 | B20 |
| IO46PB1F4 | A20 |
| IO47NB1F4 | C21 |
| IO47PB1F4 | C20 |
| IO48NB1F4 | H18 |
| IO48PB1F4 | G18 |
| IO49NB1F4 | F18 |
| IO49PB1F4 | E18 |
| IO50NB1F4 | D20 |
| IO50PB1F4 | D19 |
| IO51NB1F4 | A22 |
| IO51PB1F4 | A21 |
| IO52NB1F4 | B22 |
| IO52PB1F4 | B21 |
| IO53NB1F4 | F19 |
| IO53PB1F4 | E19 |
| IO54NB1F5 | F20 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO54PB1F5 | E20 |
| IO55NB1F5 | E21 |
| IO55PB1F5 | D21 |
| IO56NB1F5 | H19 |
| IO56PB1F5 | G19 |
| IO57NB1F5 | D22 |
| IO57PB1F5 | C22 |
| IO58NB1F5 | B23 |
| IO58PB1F5 | A23 |
| IO59NB1F5 | D23 |
| IO59PB1F5 | C23 |
| IO60NB1F5 | G21 |
| IO60PB1F5 | G20 |
| IO61NB1F5 | E23 |
| IO61PB1F5 | E22 |
| IO62NB1F5 | F22 |
| IO62PB1F5 | F21 |
| IO63NB1F5 | H20 |
| IO63PB1F5 | J19 |
| **Bank 2** | |
| IO64NB2F6 | J21 |
| IO64PB2F6 | H21 |
| IO65NB2F6 | F24 |
| IO65PB2F6 | F23 |
| IO66NB2F6 | F26 |
| IO66PB2F6 | F25 |
| IO67NB2F6 | E26 |
| IO67PB2F6 | E25 |
| IO68NB2F6 | J22 |
| IO68PB2F6 | H22 |
| IO69NB2F6 | G24 |
| IO69PB2F6 | G23 |
| IO70NB2F6 | K20 |
| IO70PB2F6 | J20 |
| IO71NB2F6 | G26 |
| IO71PB2F6 | G25 |
| IO72NB2F6 | J24 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO72PB2F6 | J23 |
| IO73NB2F6 | H24 |
| IO73PB2F6 | H23 |
| IO74NB2F7 | L21 |
| IO74PB2F7 | K21 |
| IO75NB2F7 | G27 |
| IO75PB2F7 | F27 |
| IO76NB2F7 | K23 |
| IO76PB2F7 | K22 |
| IO77NB2F7 | H26 |
| IO77PB2F7 | H25 |
| IO78NB2F7 | K25 |
| IO78PB2F7 | K24 |
| IO79NB2F7 | J26 |
| IO79PB2F7 | J25 |
| IO80NB2F7 | M20 |
| IO80PB2F7 | L20 |
| IO81NB2F7 | J27 |
| IO81PB2F7 | H27 |
| IO82NB2F7 | L23 |
| IO82PB2F7 | L22 |
| IO83NB2F7 | L25 |
| IO83PB2F7 | L24 |
| IO84NB2F7 | N21 |
| IO84PB2F7 | M21 |
| IO85NB2F8 | K27 |
| IO85PB2F8 | K26 |
| IO86NB2F8 | M23 |
| IO86PB2F8 | M22 |
| IO87NB2F8 | M25 |
| IO87PB2F8 | M24 |
| IO88NB2F8 | L27 |
| IO88PB2F8 | L26 |
| IO89NB2F8 | M27 |
| IO89PB2F8 | M26 |
| IO90NB2F8 | N23 |
| IO90PB2F8 | N22 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO91NB2F8 | N25 |
| IO91PB2F8 | N24 |
| IO92NB2F8 | N27 |
| IO92PB2F8 | N26 |
| IO93NB2F8 | P26 |
| IO93PB2F8 | P27 |
| IO94NB2F8 | N19 |
| IO94PB2F8 | N20 |
| IO95NB2F8 | P23 |
| IO95PB2F8 | P22 |
| **Bank 3** | |
| IO96NB3F9 | P25 |
| IO96PB3F9 | P24 |
| IO97NB3F9 | R26 |
| IO97PB3F9 | R27 |
| IO98NB3F9 | P21 |
| IO98PB3F9 | P20 |
| IO99NB3F9 | R24 |
| IO99PB3F9 | R25 |
| IO100NB3F9 | T26 |
| IO100PB3F9 | T27 |
| IO101NB3F9 | T24 |
| IO101PB3F9 | T25 |
| IO102NB3F9 | R20 |
| IO102PB3F9 | R21 |
| IO103NB3F9 | R23 |
| IO103PB3F9 | R22 |
| IO104NB3F9 | U26 |
| IO104PB3F9 | U27 |
| IO105NB3F9 | U24 |
| IO105PB3F9 | U25 |
| IO106NB3F9 | R19 |
| IO106PB3F9 | P19 |
| IO107NB3F10 | V26 |
| IO107PB3F10 | V27 |
| IO108NB3F10 | T23 |
| IO108PB3F10 | T22 |

# FG256




## *Note*

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| IO155NB4F14 | AC17 |
| IO155PB4F14 | AB17 |
| IO156NB4F14 | AK19 |
| IO156PB4F14 | AJ19 |
| IO157NB4F14 | AE17 |
| IO157PB4F14 | AD17 |
| IO158NB4F14 | AJ17 |
| IO158PB4F14 | AJ18 |
| IO159NB4F14/CLKEN | AG18 |
| IO159PB4F14/CLKEP | AH18 |
| IO160NB4F14/CLKFN | AG16 |
| IO160PB4F14/CLKFP | AG17 |
| **Bank 5** | |
| IO161NB5F15/CLKGN | AG14 |
| IO161PB5F15/CLKGP | AG15 |
| IO162NB5F15/CLKHN | AG13 |
| IO162PB5F15/CLKHP | AH13 |
| IO163NB5F15 | AE14 |
| IO163PB5F15 | AD14 |
| IO164NB5F15 | AJ12 |
| IO164PB5F15 | AJ13 |
| IO165NB5F15 | AB14 |
| IO165PB5F15 | AC15 |
| IO166NB5F15 | AK11 |
| IO166PB5F15 | AK12 |
| IO167NB5F15 | AB13 |
| IO167PB5F15 | AC14 |
| IO168NB5F15 | AH11 |
| IO168PB5F15 | AH12 |
| IO169NB5F15 | AD13 |
| IO169PB5F15 | AC13 |
| IO170NB5F15 | AJ10 |
| IO170PB5F15 | AJ11 |
| IO171NB5F16 | AG11 |
| IO171PB5F16 | AG12 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| IO172NB5F16 | AK9 |
| IO172PB5F16 | AK10 |
| IO173NB5F16 | AE12 |
| IO173PB5F16 | AE13 |
| IO174NB5F16 | AG9 |
| IO174PB5F16 | AG10 |
| IO175NB5F16 | AE11 |
| IO175PB5F16 | AF11 |
| IO176NB5F16 | AH8 |
| IO176PB5F16 | AH9 |
| IO177NB5F16 | AC12 |
| IO177PB5F16 | AD12 |
| IO178NB5F16 | AJ7 |
| IO178PB5F16 | AJ8 |
| IO179NB5F16 | AF9 |
| IO179PB5F16 | AF10 |
| IO180NB5F16 | AE9 |
| IO180PB5F16 | AE10 |
| IO181NB5F17 | AC11 |
| IO181PB5F17 | AD11 |
| IO182NB5F17 | AK6 |
| IO182PB5F17 | AK7 |
| IO183NB5F17 | AF8 |
| IO183PB5F17 | AG8 |
| IO184NB5F17 | AG7 |
| IO184PB5F17 | AH7 |
| IO185NB5F17 | AC10 |
| IO185PB5F17 | AD10 |
| IO186NB5F17 | AJ5 |
| IO186PB5F17 | AJ6 |
| IO187NB5F17 | AE7 |
| IO187PB5F17 | AE8 |
| IO188NB5F17 | AF6 |
| IO188PB5F17 | AF7 |
| IO189NB5F17 | AD8 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| IO189PB5F17 | AD9 |
| IO190NB5F17 | AH6 |
| IO190PB5F17 | AG6 |
| IO191NB5F17 | AG5 |
| IO191PB5F17 | AH5 |
| IO192NB5F17 | AC8 |
| IO192PB5F17 | AC9 |
| **Bank 6** | |
| IO193NB6F18 | AB7 |
| IO193PB6F18 | AC7 |
| IO194NB6F18 | AD5 |
| IO194PB6F18 | AE5 |
| IO195NB6F18 | AB6 |
| IO195PB6F18 | AC6 |
| IO196NB6F18 | AE4 |
| IO196PB6F18 | AF4 |
| IO197NB6F18 | AA8 |
| IO197PB6F18 | AB8 |
| IO198NB6F18 | AF3 |
| IO198PB6F18 | AG3 |
| IO199NB6F18 | AC4 |
| IO199PB6F18 | AD4 |
| IO200NB6F18 | AB5 |
| IO200PB6F18 | AC5 |
| IO201NB6F18 | Y7 |
| IO201PB6F18 | AA7 |
| IO202NB6F18 | AD3 |
| IO202PB6F18 | AE3 |
| IO203NB6F19 | Y6 |
| IO203PB6F19 | AA6 |
| IO204NB6F19 | Y5 |
| IO204PB6F19 | AA5 |
| IO205NB6F19 | W8 |
| IO205PB6F19 | Y8 |
| IO206NB6F19 | AA4 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO65PB1F6 | H20 |
| IO66NB1F6 | B23 |
| IO66PB1F6 | B21 |
| IO67NB1F6 | H21 |
| IO67PB1F6 | G21 |
| IO68NB1F6 | D22 |
| IO68PB1F6 | C22 |
| IO69NB1F6 | A25 |
| IO69PB1F6 | A24 |
| IO70NB1F6 | F22 |
| IO70PB1F6 | E22 |
| IO71NB1F6 | F21 |
| IO71PB1F6 | E21 |
| IO73NB1F6 | C24 |
| IO73PB1F6 | C23 |
| IO74NB1F6 | D24 |
| IO74PB1F6 | D23 |
| IO75NB1F6 | H23 |
| IO75PB1F6 | H22 |
| IO76NB1F7 | B25 |
| IO76PB1F7 | B24 |
| IO78NB1F7 | B26 |
| IO78PB1F7 | A26 |
| IO79NB1F7 | F23 |
| IO79PB1F7 | E23 |
| IO80NB1F7 | D25 |
| IO80PB1F7 | C25 |
| IO81NB1F7 | G23 |
| IO81PB1F7 | G22 |
| IO82NB1F7 | B27 |
| IO82PB1F7 | A27 |
| IO83NB1F7 | F24 |
| IO83PB1F7 | E24 |
| IO84NB1F7 | D26 |
| IO84PB1F7 | C26 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO85NB1F7 | F25 |
| IO85PB1F7 | E25 |
| **Bank 2** | |
| IO86NB2F8 | G26 |
| IO86PB2F8 | G25 |
| IO87NB2F8 | K23 |
| IO87PB2F8 | J23 |
| IO88NB2F8 | J24 |
| IO88PB2F8 | H24 |
| IO89NB2F8 | E29 |
| IO89PB2F8 | D29 |
| IO90NB2F8 | F27 |
| IO90PB2F8 | E27 |
| IO91NB2F8 | H26 |
| IO91PB2F8 | H25 |
| IO92NB2F8 | G28 |
| IO92PB2F8 | F28 |
| IO93NB2F8 | J26 |
| IO93PB2F8 | J25 |
| IO94NB2F8 | H27 |
| IO94PB2F8 | G27 |
| IO95NB2F8 | H29 |
| IO95PB2F8 | G29 |
| IO96NB2F9 | G30 |
| IO96PB2F9 | F30 |
| IO97NB2F9 | K25 |
| IO97PB2F9 | K24 |
| IO98NB2F9 | J28 |
| IO98PB2F9 | H28 |
| IO99NB2F9 | L23 |
| IO99PB2F9 | L24 |
| IO100NB2F9 | K27 |
| IO100PB2F9 | J27 |
| IO101PB2F9 | J30 |
| IO102NB2F9 | E30 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO102PB2F9 | D30 |
| IO103NB2F9 | L26 |
| IO103PB2F9 | K26 |
| IO104NB2F9 | F29 |
| IO105NB2F9 | M25 |
| IO105PB2F9 | L25 |
| IO106NB2F9 | K30 |
| IO106PB2F9 | K29 |
| IO107NB2F10 | M23 |
| IO107PB2F10 | M24 |
| IO109NB2F10 | M27 |
| IO109PB2F10 | L27 |
| IO110NB2F10 | M28 |
| IO110PB2F10 | L28 |
| IO111NB2F10 | N22 |
| IO111PB2F10 | N23 |
| IO112NB2F10 | M29 |
| IO112PB2F10 | L29 |
| IO113NB2F10 | N26 |
| IO113PB2F10 | M26 |
| IO114NB2F10 | M30 |
| IO114PB2F10 | L30 |
| IO115NB2F10 | N28 |
| IO115PB2F10 | N27 |
| IO117NB2F10 | N25 |
| IO117PB2F10 | N24 |
| IO118NB2F11 | N29 |
| IO119NB2F11 | P22 |
| IO119PB2F11 | P23 |
| IO121NB2F11 | P25 |
| IO121PB2F11 | P24 |
| IO122NB2F11 | P28 |
| IO122PB2F11 | P27 |
| IO123NB2F11 | R26 |
| IO123PB2F11 | P26 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO180PB4F16 | AG24 |
| IO181NB4F17 | AK24 |
| IO181PB4F17 | AK25 |
| IO182NB4F17 | AD22 |
| IO182PB4F17 | AC22 |
| IO183NB4F17 | AF22 |
| IO183PB4F17 | AF23 |
| IO184NB4F17 | AE21 |
| IO184PB4F17 | AE22 |
| IO185NB4F17 | AJ23 |
| IO185PB4F17 | AJ24 |
| IO187NB4F17 | AH22 |
| IO187PB4F17 | AH23 |
| IO188NB4F17 | AD21 |
| IO188PB4F17 | AC21 |
| IO189PB4F17 | AK22 |
| IO190NB4F17 | AF20 |
| IO190PB4F17 | AF21 |
| IO191NB4F17 | AG21 |
| IO191PB4F17 | AG22 |
| IO192NB4F17 | AE19 |
| IO192PB4F17 | AE20 |
| IO195NB4F18 | AK21 |
| IO195PB4F18 | AJ21 |
| IO196NB4F18 | AD19 |
| IO196PB4F18 | AD20 |
| IO197NB4F18 | AJ20 |
| IO197PB4F18 | AK20 |
| IO198NB4F18 | AC19 |
| IO198PB4F18 | AC20 |
| IO199NB4F18 | AG19 |
| IO199PB4F18 | AG20 |
| IO200NB4F18 | AH19 |
| IO200PB4F18 | AH20 |
| IO201NB4F18 | AK19 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO201PB4F18 | AJ19 |
| IO202NB4F18 | AC18 |
| IO202PB4F18 | AB18 |
| IO206NB4F19 | AE18 |
| IO206PB4F19 | AD18 |
| IO207NB4F19 | AJ17 |
| IO207PB4F19 | AJ18 |
| IO208NB4F19 | AE17 |
| IO208PB4F19 | AD17 |
| IO209NB4F19 | AK17 |
| IO210NB4F19 | AC17 |
| IO210PB4F19 | AB17 |
| IO211NB4F19 | AJ16 |
| IO211PB4F19 | AK16 |
| IO212NB4F19/CLKEN | AG18 |
| IO212PB4F19/CLKEP | AH18 |
| IO213NB4F19/CLKFN | AG16 |
| IO213PB4F19/CLKFP | AG17 |
| **Bank 5** | |
| IO214NB5F20/CLKGN | AG14 |
| IO214PB5F20/CLKGP | AG15 |
| IO215NB5F20/CLKHN | AG13 |
| IO215PB5F20/CLKHP | AH13 |
| IO216NB5F20 | AB14 |
| IO216PB5F20 | AC15 |
| IO217NB5F20 | AK15 |
| IO217PB5F20 | AJ15 |
| IO218NB5F20 | AE14 |
| IO218PB5F20 | AD14 |
| IO219NB5F20 | AK14 |
| IO219PB5F20 | AJ14 |
| IO222NB5F20 | AB13 |
| IO222PB5F20 | AC14 |
| IO223NB5F21 | AJ12 |
| IO223PB5F21 | AJ13 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO225NB5F21 | AH11 |
| IO225PB5F21 | AH12 |
| IO226NB5F21 | AC13 |
| IO226PB5F21 | AD13 |
| IO227NB5F21 | AE12 |
| IO227PB5F21 | AE13 |
| IO228NB5F21 | AG11 |
| IO228PB5F21 | AG12 |
| IO229NB5F21 | AK11 |
| IO229PB5F21 | AK12 |
| IO230NB5F21 | AC12 |
| IO230PB5F21 | AD12 |
| IO232NB5F21 | AE11 |
| IO232PB5F21 | AF11 |
| IO233NB5F21 | AJ10 |
| IO233PB5F21 | AJ11 |
| IO234NB5F21 | AC11 |
| IO234PB5F21 | AD11 |
| IO236NB5F22 | AK9 |
| IO236PB5F22 | AK10 |
| IO237NB5F22 | AG9 |
| IO237PB5F22 | AG10 |
| IO238NB5F22 | AF9 |
| IO238PB5F22 | AF10 |
| IO239NB5F22 | AH8 |
| IO239PB5F22 | AH9 |
| IO240NB5F22 | AC10 |
| IO240PB5F22 | AD10 |
| IO242NB5F22 | AE9 |
| IO242PB5F22 | AE10 |
| IO243NB5F22 | AJ7 |
| IO243PB5F22 | AJ8 |
| IO244NB5F22 | AK6 |
| IO244PB5F22 | AK7 |
| IO245NB5F23 | AF8 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | AK18 |
| GND | AK2 |
| GND | AK23 |
| GND | AK29 |
| GND | AK8 |
| GND | B1 |
| GND | B2 |
| GND | B22 |
| GND | B29 |
| GND | B30 |
| GND | B9 |
| GND | C10 |
| GND | C15 |
| GND | C16 |
| GND | C21 |
| GND | C28 |
| GND | C3 |
| GND | D27 |
| GND | D28 |
| GND | D4 |
| GND | E26 |
| GND | E5 |
| GND | H1 |
| GND | H30 |
| GND | J2 |
| GND | J22 |
| GND | J29 |
| GND | J9 |
| GND | K10 |
| GND | K21 |
| GND | K28 |
| GND | K3 |
| GND | L11 |
| GND | L20 |
| GND | M12 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | M13 |
| GND | M14 |
| GND | M15 |
| GND | M16 |
| GND | M17 |
| GND | M18 |
| GND | M19 |
| GND | N1 |
| GND | N12 |
| GND | N13 |
| GND | N14 |
| GND | N15 |
| GND | N16 |
| GND | N17 |
| GND | N18 |
| GND | N19 |
| GND | N30 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | P15 |
| GND | P16 |
| GND | P17 |
| GND | P18 |
| GND | P19 |
| GND | R12 |
| GND | R13 |
| GND | R14 |
| GND | R15 |
| GND | R16 |
| GND | R17 |
| GND | R18 |
| GND | R19 |
| GND | R28 |
| GND | R3 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | T12 |
| GND | T13 |
| GND | T14 |
| GND | T15 |
| GND | T16 |
| GND | T17 |
| GND | T18 |
| GND | T19 |
| GND | T28 |
| GND | T3 |
| GND | U12 |
| GND | U13 |
| GND | U14 |
| GND | U15 |
| GND | U16 |
| GND | U17 |
| GND | U18 |
| GND | U19 |
| GND | V1 |
| GND | V12 |
| GND | V13 |
| GND | V14 |
| GND | V15 |
| GND | V16 |
| GND | V17 |
| GND | V18 |
| GND | V19 |
| GND | V30 |
| GND | W12 |
| GND | W13 |
| GND | W14 |
| GND | W15 |
| GND | W16 |
| GND | W17 |
| GND | W18 |

| CQ208 | |
|---|---|
| AX250 Function | Pin Number |
| **Bank 0** | |
| IO02NB0F0 | 197 |
| IO03NB0F0 | 198 |
| IO03PB0F0 | 199 |
| IO12NB0F0/HCLKAN | 191 |
| IO12PB0F0/HCLKAP | 192 |
| IO13NB0F0/HCLKBN | 185 |
| IO13PB0F0/HCLKBP | 186 |
| **Bank 1** | |
| IO14NB1F1/HCLKCN | 180 |
| IO14PB1F1/HCLKCP | 181 |
| IO15NB1F1/HCLKDN | 174 |
| IO15PB1F1/HCLKDP | 175 |
| IO16NB1F1 | 170 |
| IO16PB1F1 | 171 |
| IO24NB1F1 | 165 |
| IO24PB1F1 | 166 |
| IO26NB1F1 | 161 |
| IO26PB1F1 | 162 |
| IO27NB1F1 | 159 |
| IO27PB1F1 | 160 |
| **Bank 2** | |
| IO29NB2F2 | 151 |
| IO29PB2F2 | 153 |
| IO30NB2F2 | 152 |
| IO30PB2F2 | 154 |
| IO31PB2F2 | 148 |
| IO32NB2F2 | 146 |
| IO32PB2F2 | 147 |
| IO34NB2F2 | 144 |
| IO34PB2F2 | 145 |
| IO39NB2F2 | 139 |
| IO39PB2F2 | 140 |
| IO40PB2F2 | 141 |
| IO41NB2F2 | 137 |
| IO41PB2F2 | 138 |
| IO43NB2F2 | 132 |

| CQ208 | |
|---|---|
| AX250 Function | Pin Number |
| IO43PB2F2 | 134 |
| IO44NB2F2 | 131 |
| IO44PB2F2 | 133 |
| **Bank 3** | |
| IO45NB3F3 | 127 |
| IO45PB3F3 | 129 |
| IO46NB3F3 | 126 |
| IO46PB3F3 | 128 |
| IO48NB3F3 | 122 |
| IO48PB3F3 | 123 |
| IO50NB3F3 | 120 |
| IO50PB3F3 | 121 |
| IO55NB3F3 | 116 |
| IO55PB3F3 | 117 |
| IO57NB3F3 | 114 |
| IO57PB3F3 | 115 |
| IO59NB3F3 | 110 |
| IO59PB3F3 | 111 |
| IO60NB3F3 | 108 |
| IO60PB3F3 | 109 |
| IO61NB3F3 | 106 |
| IO61PB3F3 | 107 |
| **Bank 4** | |
| IO62NB4F4 | 100 |
| IO62PB4F4 | 103 |
| IO63NB4F4 | 101 |
| IO63PB4F4 | 102 |
| IO64NB4F4 | 96 |
| IO64PB4F4 | 97 |
| IO72NB4F4 | 91 |
| IO72PB4F4 | 92 |
| IO74NB4F4/CLKEN | 87 |
| IO74PB4F4/CLKEP | 88 |
| IO75NB4F4/CLKFN | 81 |
| IO75PB4F4/CLKFP | 82 |
| **Bank 5** | |
| IO76NB5F5/CLKGN | 76 |

| CQ208 | |
|---|---|
| AX250 Function | Pin Number |
| IO76PB5F5/CLKGP | 77 |
| IO77NB5F5/CLKHN | 70 |
| IO77PB5F5/CLKHP | 71 |
| IO78NB5F5 | 66 |
| IO78PB5F5 | 67 |
| IO86NB5F5 | 62 |
| IO87NB5F5 | 60 |
| IO87PB5F5 | 61 |
| IO88NB5F5 | 56 |
| IO88PB5F5 | 57 |
| IO89NB5F5 | 54 |
| IO89PB5F5 | 55 |
| **Bank 6** | |
| IO91NB6F6 | 47 |
| IO91PB6F6 | 49 |
| IO92NB6F6 | 48 |
| IO92PB6F6 | 50 |
| IO93NB6F6 | 42 |
| IO93PB6F6 | 43 |
| IO94PB6F6 | 44 |
| IO96NB6F6 | 40 |
| IO96PB6F6 | 41 |
| IO101NB6F6 | 35 |
| IO101PB6F6 | 36 |
| IO102PB6F6 | 37 |
| IO103NB6F6 | 33 |
| IO103PB6F6 | 34 |
| IO105NB6F6 | 28 |
| IO105PB6F6 | 30 |
| IO106NB6F6 | 27 |
| IO106PB6F6 | 29 |
| **Bank 7** | |
| IO107NB7F7 | 23 |
| IO107PB7F7 | 25 |
| IO108NB7F7 | 22 |
| IO108PB7F7 | 24 |
| IO110NB7F7 | 18 |

| CQ352 | |
|---|---|
| AX250 Function | Pin Number |
| IO64PB4F4 | 167 |
| IO65NB4F4 | 170 |
| IO65PB4F4 | 171 |
| IO66NB4F4 | 164 |
| IO66PB4F4 | 165 |
| IO67NB4F4 | 160 |
| IO67PB4F4 | 161 |
| IO68NB4F4 | 158 |
| IO68PB4F4 | 159 |
| IO70NB4F4 | 154 |
| IO70PB4F4 | 155 |
| IO72NB4F4 | 152 |
| IO72PB4F4 | 153 |
| IO73NB4F4 | 146 |
| IO73PB4F4 | 147 |
| IO74NB4F4/CLKEN | 142 |
| IO74PB4F4/CLKEP | 143 |
| IO75NB4F4/CLKFN | 136 |
| IO75PB4F4/CLKFP | 137 |
| **Bank 5** | |
| IO76NB5F5/CLKGN | 128 |
| IO76PB5F5/CLKGP | 129 |
| IO77NB5F5/CLKHN | 122 |
| IO77PB5F5/CLKHP | 123 |
| IO78NB5F5 | 112 |
| IO78PB5F5 | 113 |
| IO79NB5F5 | 118 |
| IO79PB5F5 | 119 |
| IO80NB5F5 | 110 |
| IO80PB5F5 | 111 |
| IO82NB5F5 | 106 |
| IO82PB5F5 | 107 |
| IO84NB5F5 | 100 |
| IO84PB5F5 | 101 |
| IO85NB5F5 | 104 |

| CQ352 | |
|---|---|
| AX250 Function | Pin Number |
| IO85PB5F5 | 105 |
| IO86NB5F5 | 98 |
| IO86PB5F5 | 99 |
| IO87NB5F5 | 94 |
| IO87PB5F5 | 95 |
| IO89NB5F5 | 92 |
| IO89PB5F5 | 93 |
| **Bank 6** | |
| IO90PB6F6 | 86 |
| IO91NB6F6 | 84 |
| IO91PB6F6 | 85 |
| IO92NB6F6 | 78 |
| IO92PB6F6 | 79 |
| IO93NB6F6 | 82 |
| IO93PB6F6 | 83 |
| IO95NB6F6 | 76 |
| IO95PB6F6 | 77 |
| IO96NB6F6 | 72 |
| IO96PB6F6 | 73 |
| IO97NB6F6 | 70 |
| IO97PB6F6 | 71 |
| IO98NB6F6 | 66 |
| IO98PB6F6 | 67 |
| IO99NB6F6 | 64 |
| IO99PB6F6 | 65 |
| IO100NB6F6 | 60 |
| IO100PB6F6 | 61 |
| IO101NB6F6 | 58 |
| IO101PB6F6 | 59 |
| IO103NB6F6 | 54 |
| IO103PB6F6 | 55 |
| IO104NB6F6 | 52 |
| IO104PB6F6 | 53 |
| IO105NB6F6 | 48 |
| IO105PB6F6 | 49 |

| CQ352 | |
|---|---|
| AX250 Function | Pin Number |
| IO106NB6F6 | 46 |
| IO106PB6F6 | 47 |
| Bank 7 | |
| IO107NB7F7 | 40 |
| IO107PB7F7 | 41 |
| IO108NB7F7 | 42 |
| IO108PB7F7 | 43 |
| IO109NB7F7 | 36 |
| IO109PB7F7 | 37 |
| IO110NB7F7 | 34 |
| IO110PB7F7 | 35 |
| IO111NB7F7 | 30 |
| IO111PB7F7 | 31 |
| IO113NB7F7 | 28 |
| IO113PB7F7 | 29 |
| IO114NB7F7 | 24 |
| IO114PB7F7 | 25 |
| IO115NB7F7 | 22 |
| IO115PB7F7 | 23 |
| IO116NB7F7 | 18 |
| IO116PB7F7 | 19 |
| IO117NB7F7 | 16 |
| IO117PB7F7 | 17 |
| IO118NB7F7 | 12 |
| IO118PB7F7 | 13 |
| IO119NB7F7 | 10 |
| IO119PB7F7 | 11 |
| IO121NB7F7 | 6 |
| IO121PB7F7 | 7 |
| IO123NB7F7 | 4 |
| IO123PB7F7 | 5 |
| **Dedicated I/O** | |
| GND | 1 |
| GND | 9 |
| GND | 15 |

| CQ352 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| VCCDA | 346 |
| VCCIB0 | 321 |
| VCCIB0 | 333 |
| VCCIB0 | 344 |
| VCCIB1 | 273 |
| VCCIB1 | 285 |
| VCCIB1 | 297 |
| VCCIB2 | 227 |
| VCCIB2 | 239 |
| VCCIB2 | 245 |
| VCCIB2 | 257 |
| VCCIB3 | 185 |
| VCCIB3 | 197 |
| VCCIB3 | 203 |
| VCCIB3 | 215 |
| VCCIB4 | 144 |
| VCCIB4 | 156 |
| VCCIB4 | 168 |
| VCCIB5 | 96 |
| VCCIB5 | 108 |
| VCCIB5 | 120 |
| VCCIB6 | 50 |
| VCCIB6 | 62 |
| VCCIB6 | 68 |
| VCCIB6 | 80 |
| VCCIB7 | 8 |
| VCCIB7 | 20 |
| VCCIB7 | 26 |
| VCCIB7 | 38 |
| VCCPLA | 317 |
| VCCPLB | 315 |
| VCCPLC | 303 |
| VCCPLD | 301 |
| VCCPLE | 140 |
| VCCPLF | 138 |

| CQ352 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| VCCPLG | 126 |
| VCCPLH | 124 |
| VCOMPLA | 318 |
| VCOMPLB | 316 |
| VCOMPLC | 304 |
| VCOMPLD | 302 |
| VCOMPLE | 141 |
| VCOMPLF | 139 |
| VCOMPLG | 127 |
| VCOMPLH | 125 |
| VPUMP | 267 |

| CG624 | |
|---|---|
| AX1000 Function | Pin Number |
| GND | A8 |
| GND | AA10 |
| GND | AA16 |
| GND | AA18 |
| GND | AA21 |
| GND | AA5 |
| GND | AB22 |
| GND | AB4 |
| GND | AC10 |
| GND | AC16 |
| GND | AC23 |
| GND | AC3 |
| GND | AD1 |
| GND | AD2 |
| GND | AD24 |
| GND | AD25 |
| GND | AE1 |
| GND | AE18 |
| GND | AE2 |
| GND | AE24 |
| GND | AE25 |
| GND | AE8 |
| GND | B1 |
| GND | B2 |
| GND | B24 |
| GND | B25 |
| GND | C10 |
| GND | C16 |
| GND | C23 |
| GND | C3 |
| GND | D22 |
| GND | D4 |
| GND | E10 |
| GND | E16 |
| GND | E21 |
| GND | E5 |

| CG624 | |
|---|---|
| AX1000 Function | Pin Number |
| GND/LP | E8 |
| GND | H1 |
| GND | H21 |
| GND | H25 |
| GND | K21 |
| GND | K23 |
| GND | K3 |
| GND | L11 |
| GND | L12 |
| GND | L13 |
| GND | L14 |
| GND | L15 |
| GND | M11 |
| GND | M12 |
| GND | M13 |
| GND | M14 |
| GND | M15 |
| GND | N11 |
| GND | N12 |
| GND | N13 |
| GND | N14 |
| GND | N15 |
| GND | P11 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | P15 |
| GND | R11 |
| GND | R12 |
| GND | R13 |
| GND | R14 |
| GND | R15 |
| GND | T21 |
| GND | T23 |
| GND | T3 |
| GND | T5 |

| CG624 | |
|---|---|
| AX1000 Function | Pin Number |
| GND | V1 |
| GND | V25 |
| GND | V5 |
| NC | A14 |
| NC | AA20 |
| NC | AB13 |
| NC | AD4 |
| NC | AE12 |
| NC | F21 |
| NC | G10 |
| PRA | F13 |
| PRB | A13 |
| PRC | AB12 |
| PRD | AE13 |
| TCK | F5 |
| TDI | C5 |
| TDO | F6 |
| TMS | D6 |
| TRST | E6 |
| VCCA | AB20 |
| VCCA | F22 |
| VCCA | F4 |
| VCCA | J17 |
| VCCA | J9 |
| VCCA | K10 |
| VCCA | K11 |
| VCCA | K15 |
| VCCA | K16 |
| VCCA | L10 |
| VCCA | L16 |
| VCCA | R10 |
| VCCA | R16 |
| VCCA | T10 |
| VCCA | T11 |
| VCCA | T15 |
| VCCA | T16 |